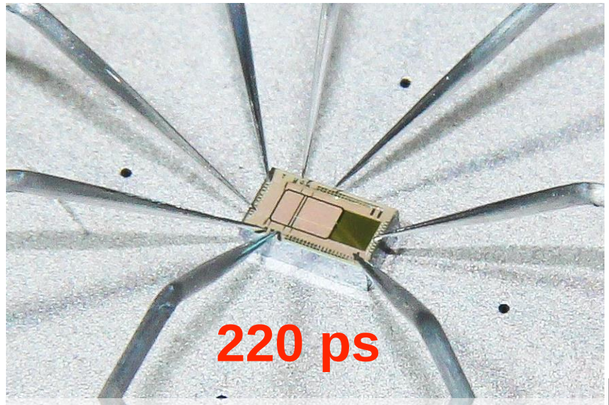
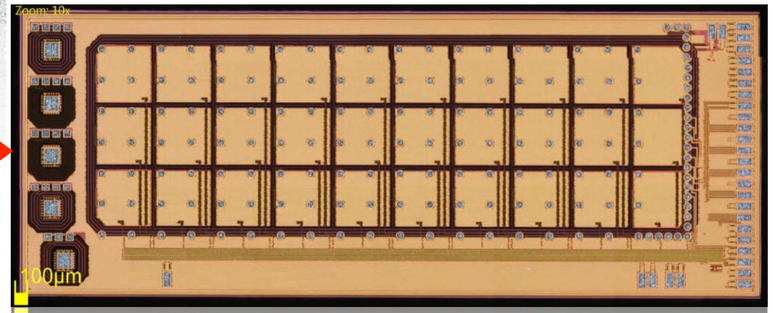
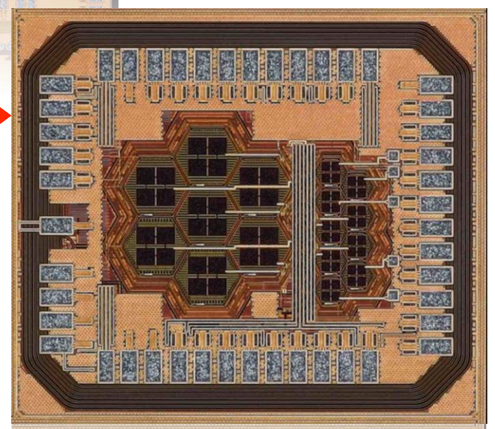
50 ps timing with SiGe Bi-CMOS monolithic pixel sensors



(2017)



(2018) 110 ps



(2019) 50 ps

Lorenzo Paolozzi
Université de Genève

VERTEX 2019
October 16, 2019

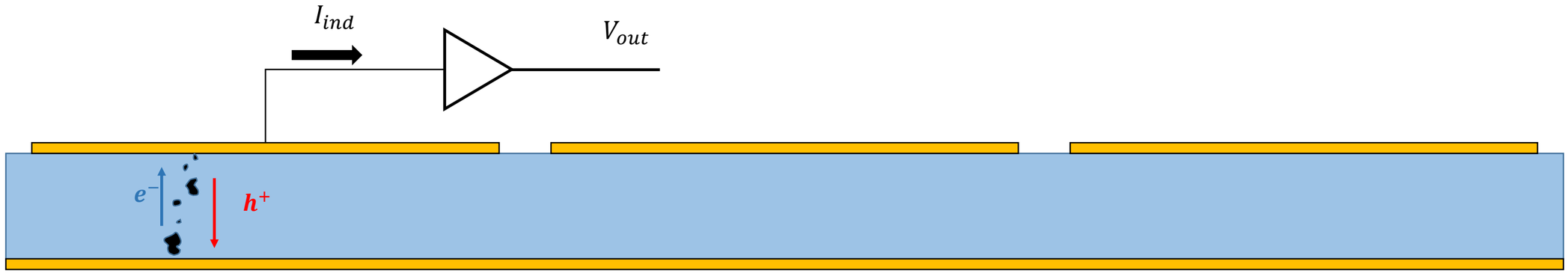
Timing with silicon detectors

Time resolution of silicon pixel detectors

(Recommended reading W. Riegler and G. Aglieri Rinella, Time resolution of silicon pixel sensors, JINST 12 (2017) P11017)

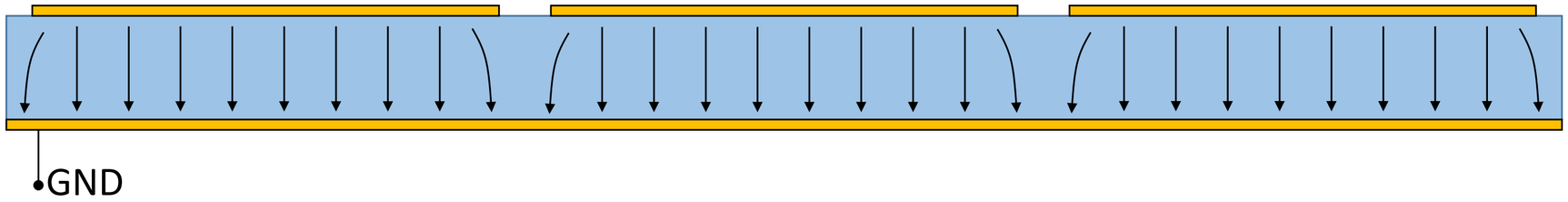
What are the main parameters that control the time resolution of semiconductor detectors?

1. Geometry & fields
2. Charge collection (or Landau) noise
3. Electronics noise



1. Geometry and fields

Sensor optimization for time measurement means:
sensor time response **independent** from the particle trajectory



$\Longrightarrow$ **"Parallel plate"** read out: wide pixel w.r.t. depletion depth

Induced current for
a parallel plate readout
from Shockley-Ramo's theorem:

$$I_{ind} = \sum_i q_i \bar{v}_{drift,i} \cdot \bar{E}_{w,i} \cong v_{drift} \frac{1}{D} \sum_i q_i$$

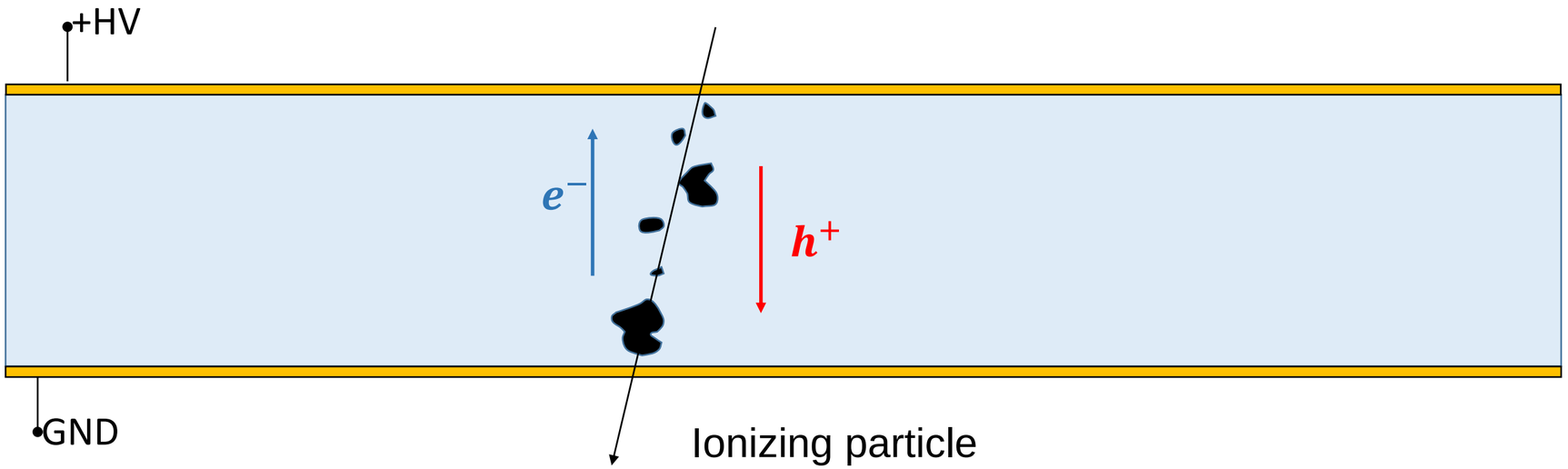
Scalar, saturated

Scalar, uniform

Desired features:

- **Uniform** Ramo field (signal induction)
- **Uniform** electric field (charge transport)
- **Saturated** charge drift velocity

2. Charge-collection (or Landau) noise

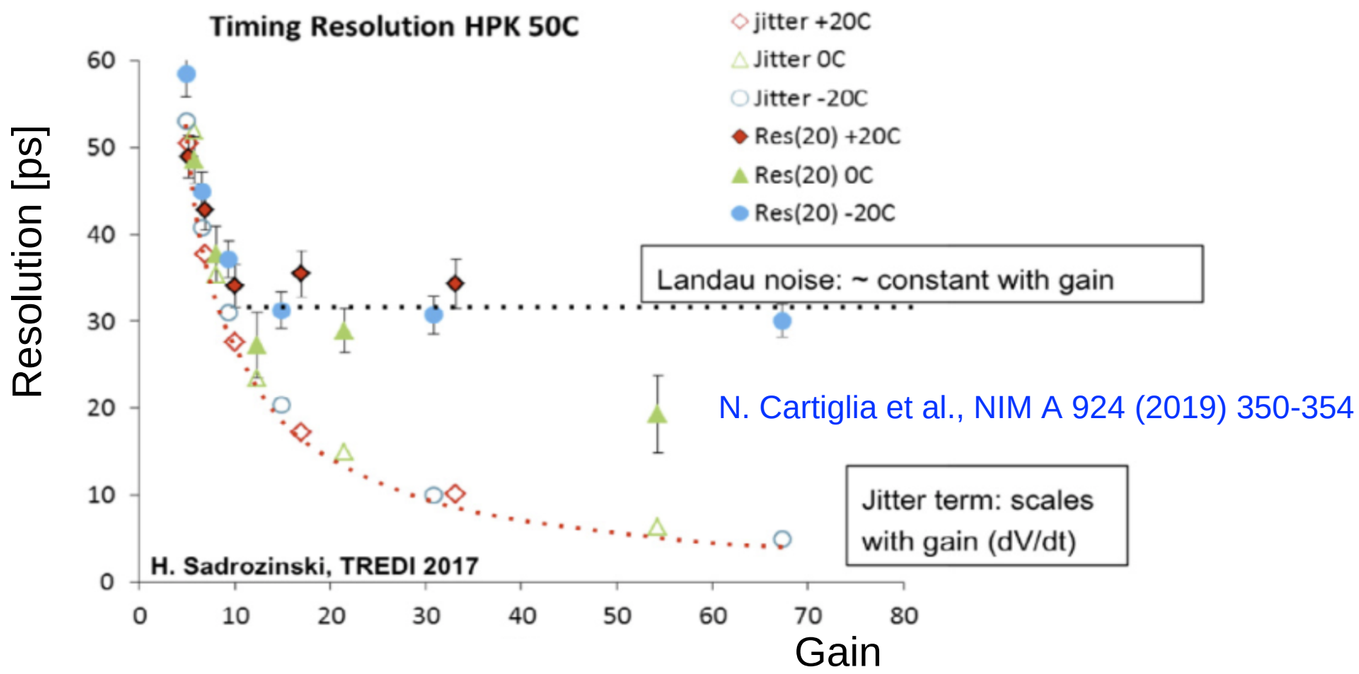


is produced by the **non uniformity of the charge deposition** in the sensor:

$$I_{ind} \cong v_{drift} \frac{1}{D} \sum_i q_i$$

When **large clusters** are absorbed at the electrodes, their contribution is removed from the induced current. The **statistical origin** of this variability of I_{ind} makes this effect irreducible in PN-junction sensors.

2. Charge-collection (or Landau) noise



N. Cartiglia et al., NIM A 924 (2019) 350-354

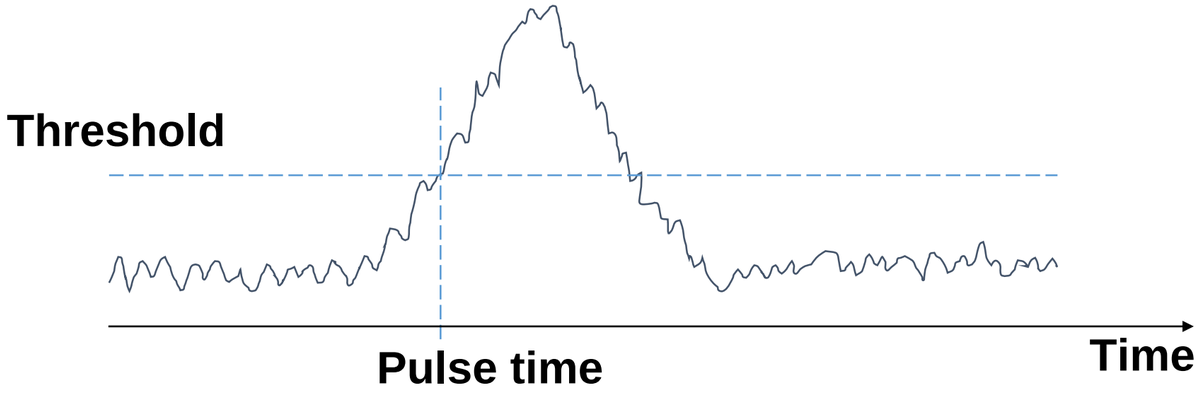
Charge collection noise represents an intrinsic limit to the time resolution for a semiconductor PN-junction detector.

~30 ps reached by present LGAD sensors.

Lower contribution from sensors without internal gain

3. Electronics noise

Once the geometry has been fixed, the time resolution depends mostly on the amplifier performance.



$$\sigma_t = \frac{\sigma_V}{\frac{dV}{dt}} \cong \frac{ENC}{I_{ind}}$$

Need an ultra-fast, low noise, low power-consumption electronics with fast rise time and small capacitance. Our solution:

High f_t, single transistor preamplifier ⟶ **SiGe HBT** technology.

Equivalent Noise Charge

For a fast charge integrator in BJT technology, the ENC series noise is:

$$ENC_{\text{series noise}} \propto \sqrt{k_1 \cdot \frac{C_{tot}^2}{\beta} + k_2 \cdot R_b C_{tot}^2}$$

Goal: maximize the current gain β at high frequencies while keeping a low base resistance R_b

For a NPN BJT, the amplifier current gain β can be expressed as:

$$\beta = \frac{i_C}{i_B} = \frac{\tau_p}{\tau_t}$$

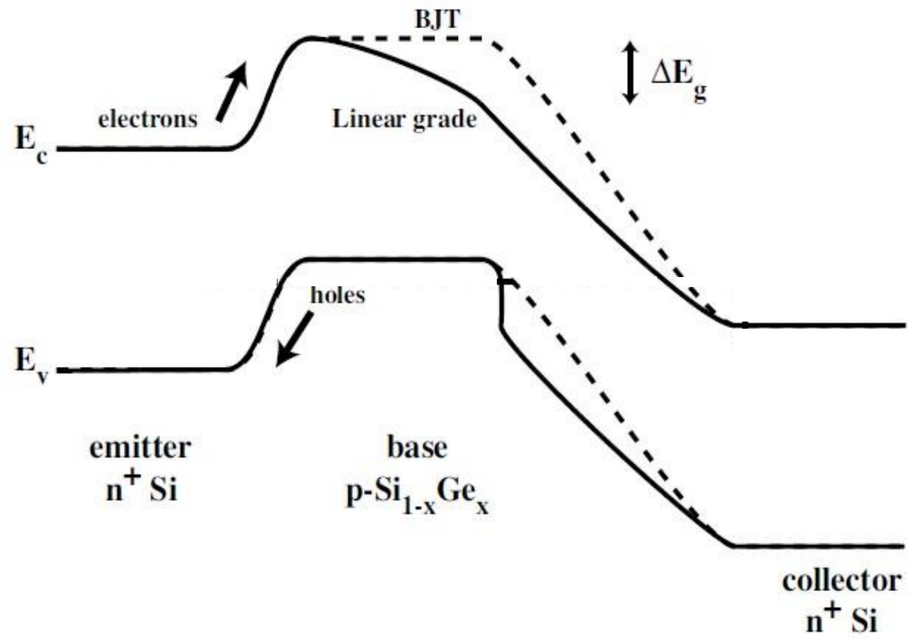
τ_p = hole recombination time in Base

τ_t = electron transit time (Emitter to Collector)

Large $\beta \Longrightarrow$ Minimize the electron transit time

SiGe HBT technology for low-noise, fast amplifiers

In SiGe Heterojunction Bipolar Transistors (HBT) the **grading** of the bandgap in the Base changes the **charge-transport mechanism** in the Base from **diffusion** to **drift**:



Grading of germanium in the base:

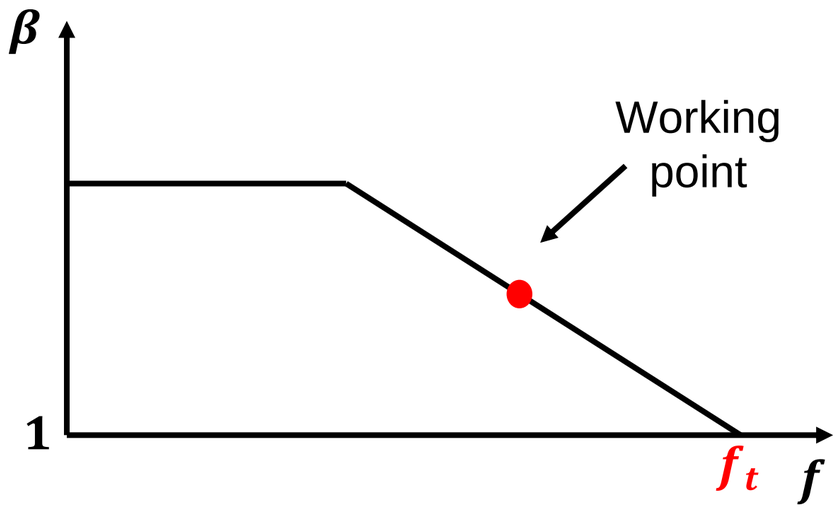
field-assisted charge transport in the Base,
equivalent to introducing an electric field in the Base

$\Longrightarrow$ short e^- transit time in Base $\Longrightarrow$ very high β

$\Longrightarrow$ smaller size $\Longrightarrow$ reduction of R_b and very high f_t

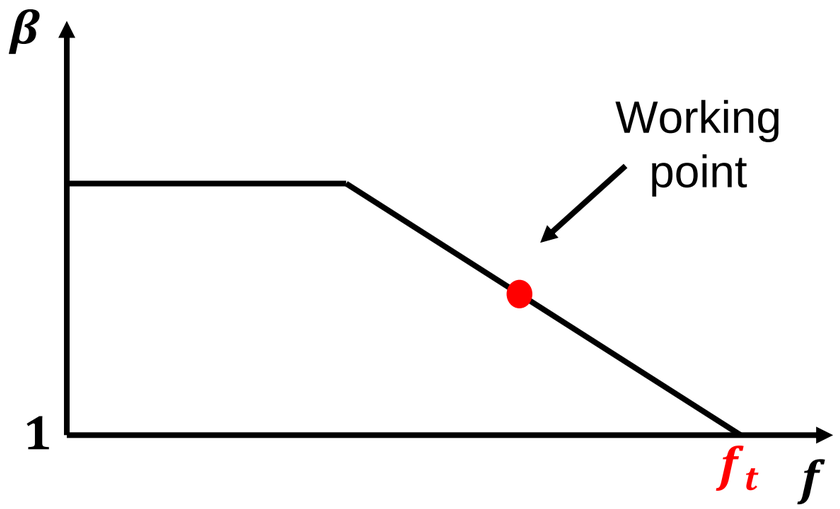
Hundreds of GHz

Current gain and power consumption: f_t is the key



	$f_t = 10\ GHz$	$f_t = 50\ GHz$	$f_t = 100\ GHz$
$\beta_{max}\ at\ 200\ MHz$	50	250	500
$\beta_{max}\ at\ 1\ GHz$	10	50	100
$\beta_{max}\ at\ 5\ GHz$	2	10	20

Current gain and power consumption: f_t is the key



	$f_t = 10\ GHz$	$f_t = 50\ GHz$	$f_t = 100\ GHz$
$\beta_{max}\ at\ 200\ MHz$	50	250	500
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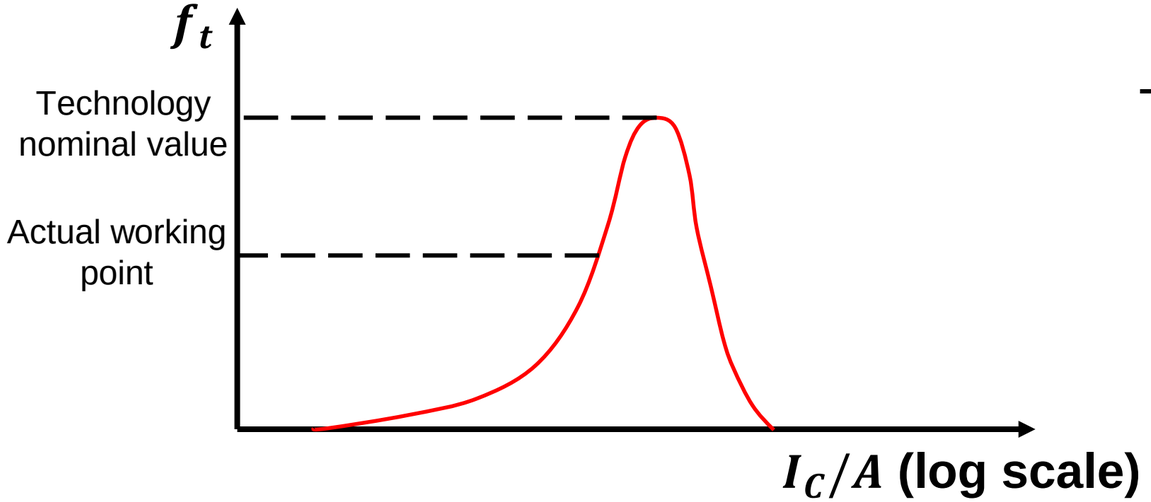
$\beta_{max}\ at\ 5\ GHz$	2	10	20



Trade-off: **ENC** ⟺ **Power Consumption**

$f_t > 100\ GHz$ technologies are necessary for a fast amplification of silicon pixel signals.

Technology choice

Exploit the properties of state-of-the-art SiGe Bi-CMOS transistors to produce an **ultra-fast, low-noise, low-power consumption amplifier**

Leading-edge technology: **IHP SG13G2**

130 nm process featuring **SiGe HBT** with

- Transistor transition frequency: $f_t = 0.3\,THz$
- DC Current gain: $\beta = 900$

Time digitisation:

- 4 ps inverter; delay precision ~100 fs
- > 40GHz oscillation frequency achievable with purely digital schematics

We were able to design a TDCs with a time binning down to 4ps and power consumption of **few tens mW/ch** with simple architecture

Why SiGe BiCMOS for signal amplification

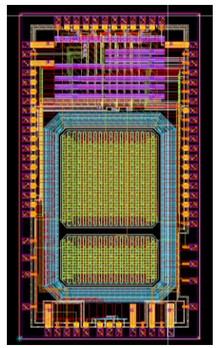
- High f_T and high β SiGe HBT allows for amplifiers with:
  - ➞Intrinsically **low series noise**
  - ➞**fast pulse integration**
  - ➞**High gain**
  - ➞**very low-power consumption**
- Moreover, it is a **fast growing technology**
  - ➞**f_t = 700 GHz** transistor under development
- **Commercial** VLSI CMOS foundry processes available

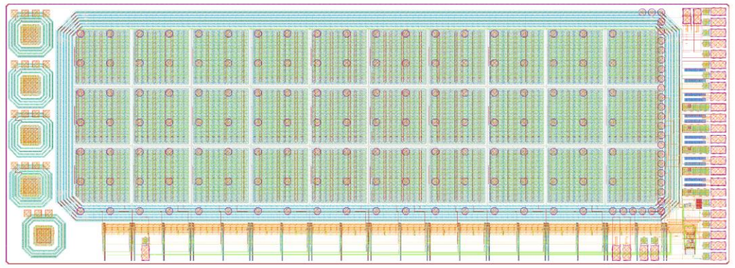
source: https://towerjazz.com/technology/rf-and-hpa/sige-bicmos-platform/

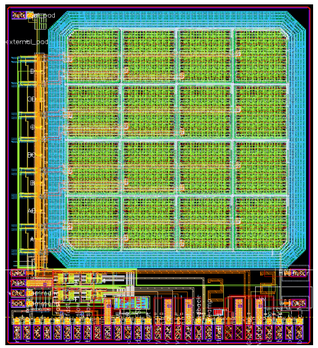
Experimental results

The prototype chips

Design submitted: **2016** **2017** **2019**



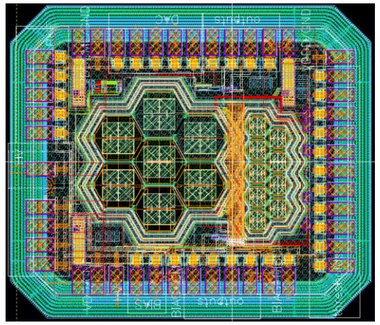


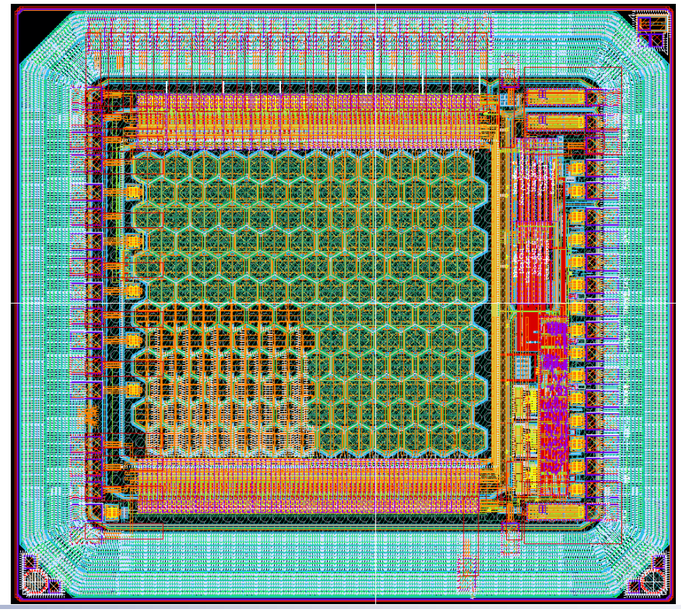


TT-PET

For a silicon TOF-PET Project

Design submitted: **2018** **2019**

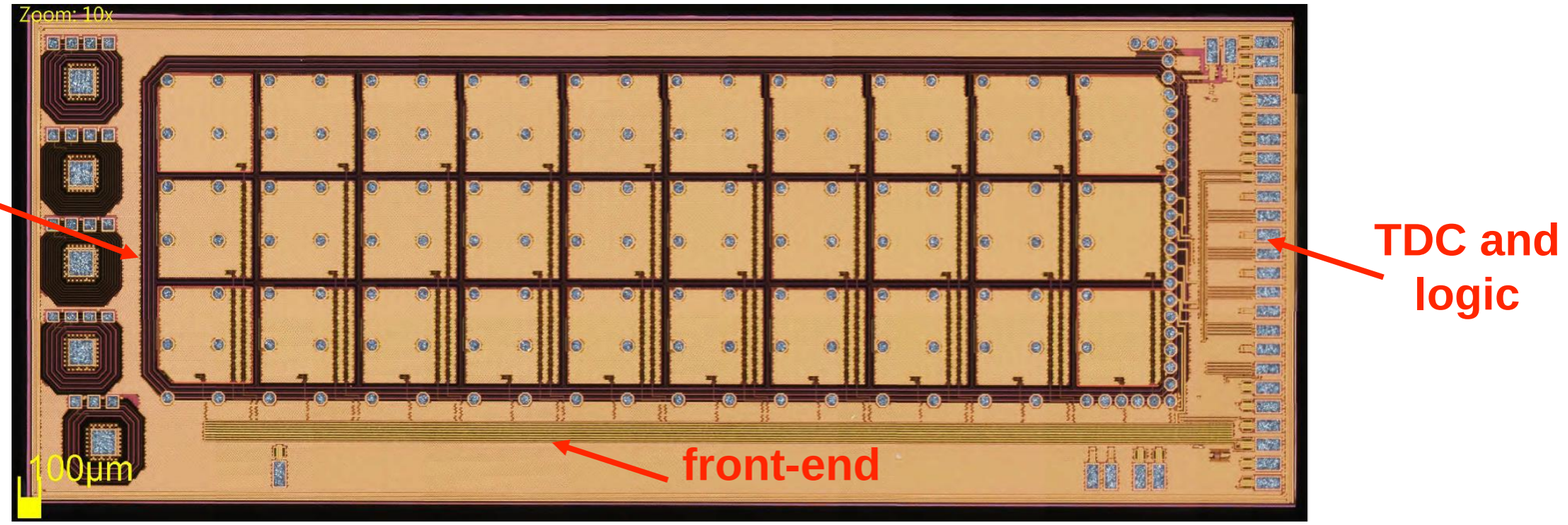




For generic timing R&D

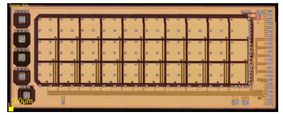
The TT-PET “demonstrator” chip

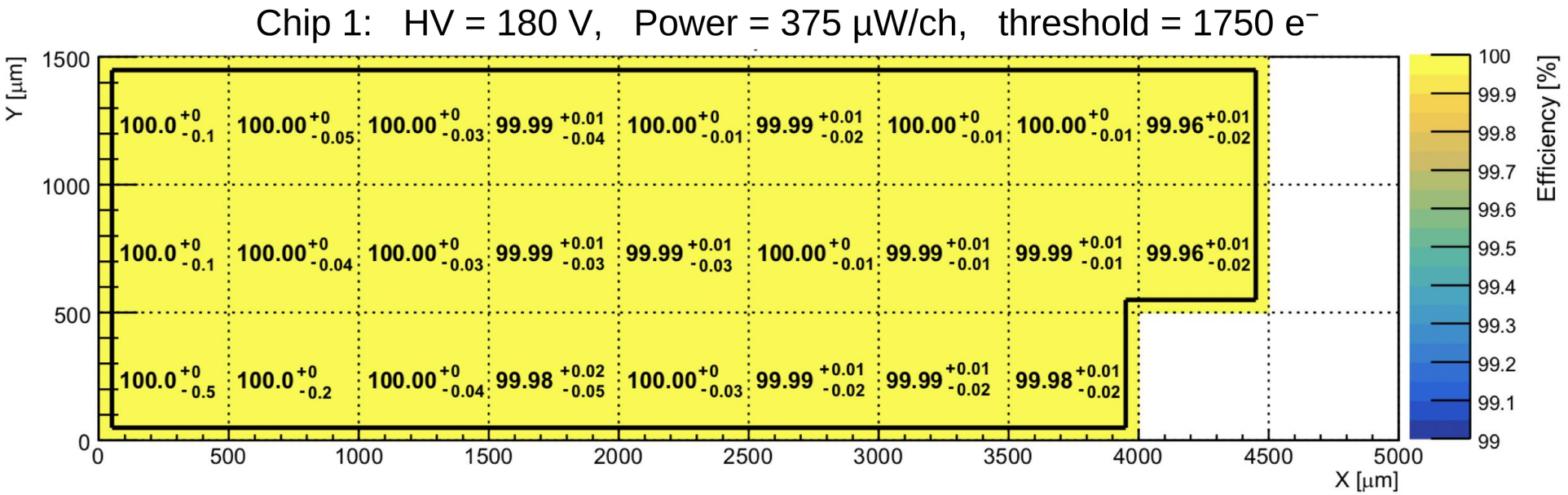
Matrix of **3×10** n-on-p pixels, of **470×470 µm²** (C_{tot} = 750 fF) spaced by **30 µm**.



- SiGe HBT **preamplifier**
- CMOS-based open-loop tri-stage **discriminator** (adjustable threshold with an 8-bit DAC), that preserves the **TOA** and the **TOT** of the pixel
- Discriminator output sent to **fast-OR chain**
- **50ps binning TDC**, R/O logic, serializer

Test beam results: efficiency

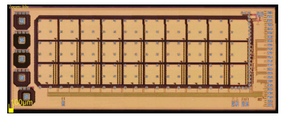




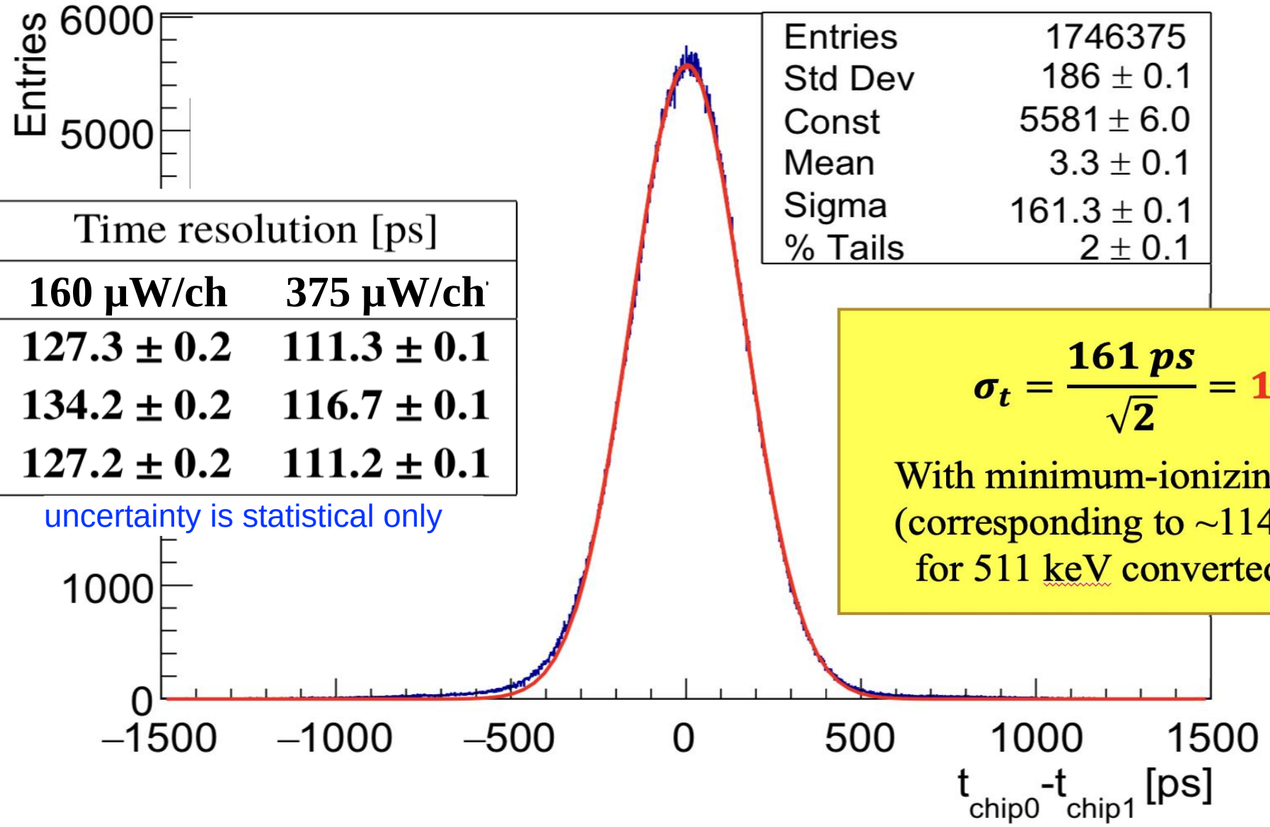
Full efficiency, even in the inter-pixel region.

L. Paolozzi *et al.*, 2019 JINST **14** P02009, https://doi.org/10.1088/1748-0221/14/02/P02009
P. Valerio *et al.*, 2019 JINST **14** P07013, https://doi.org/10.1088/1748-0221/14/07/P07013

Test beam results: time resolution



Chip 1: HV = 180 V, Power = 375 µW/ch, threshold = 1750 e^-



	Time resolution [ps]	
	160 µW/ch	**375 µW/ch**
$\sigma_{t,\ chip\ 0}$	**127.3 ± 0.2**	**111.3 ± 0.1**
$\sigma_{t,\ chip\ 1}$	**134.2 ± 0.2**	**116.7 ± 0.1**
$\sigma_{t,\ chip\ 2}$	**127.2 ± 0.2**	**111.2 ± 0.1**

uncertainty is statistical only

$$\sigma_t = \frac{161\ ps}{\sqrt{2}} = 114\ ps$$

With minimum-ionizing particles (corresponding to ~114/4 ~ 30ps for 511 keV converted photons)

Excellent result for a silicon pixel detector without internal gain,
obtained on a large capacitance (750 fF) and power consumption of 150 mW/cm^2.

L. Paolozzi *et al.*, 2019 JINST **14** P02009, https://doi.org/10.1088/1748-0221/14/02/P02009
P. Valerio *et al.*, 2019 JINST **14** P07013, https://doi.org/10.1088/1748-0221/14/07/P07013

The “hexagonal” prototype sensor

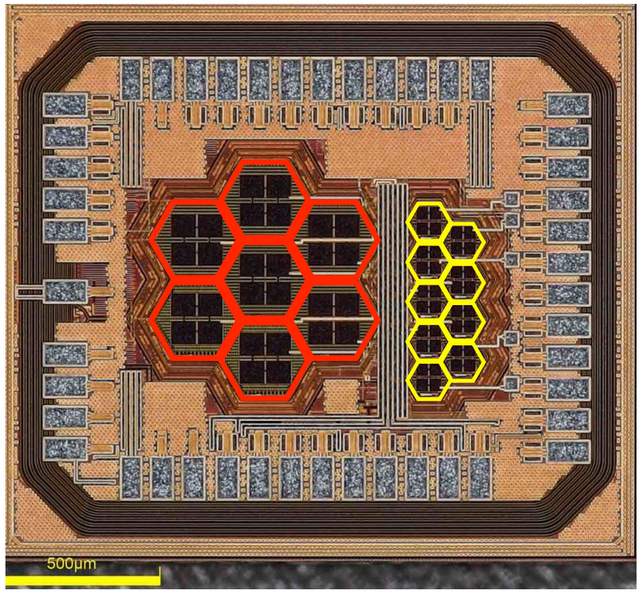
Developed in IHP **SG13G2** technology (130nm).

Matrices with hexagons of two sizes:

- ➞ hexagon side 130µm and 65µm, with 10µm inter-pixel spacing
- ➞ C_{TOT} = 220 and 70 fF

Exploits:

- ➞ New dedicated custom components developed together with foundry
- ➞ New guard-ring structure



Collaboration of:

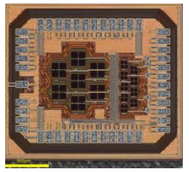
UNIVERSITÉ DE GENÈVE
FACULTÉ DES SCIENCES
Département de physique nucléaire et corpusculaire

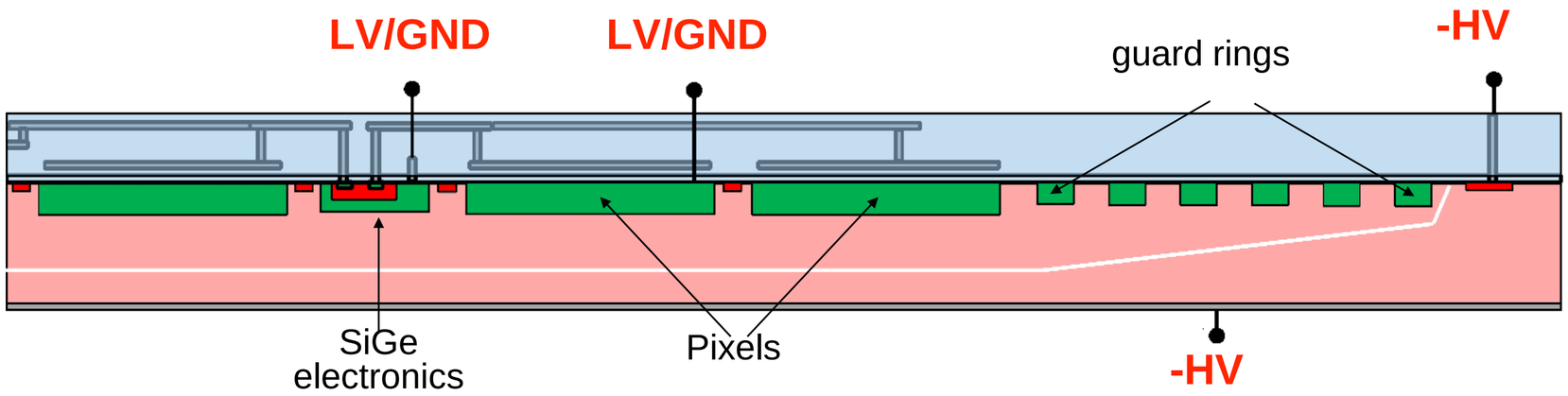
Università di Roma Tor Vergata

CERN Idea^s

ihp innovations for high performance microelectronics
Leibniz-Institut für innovative Mikroelektronik

The “hexagonal” prototype sensor





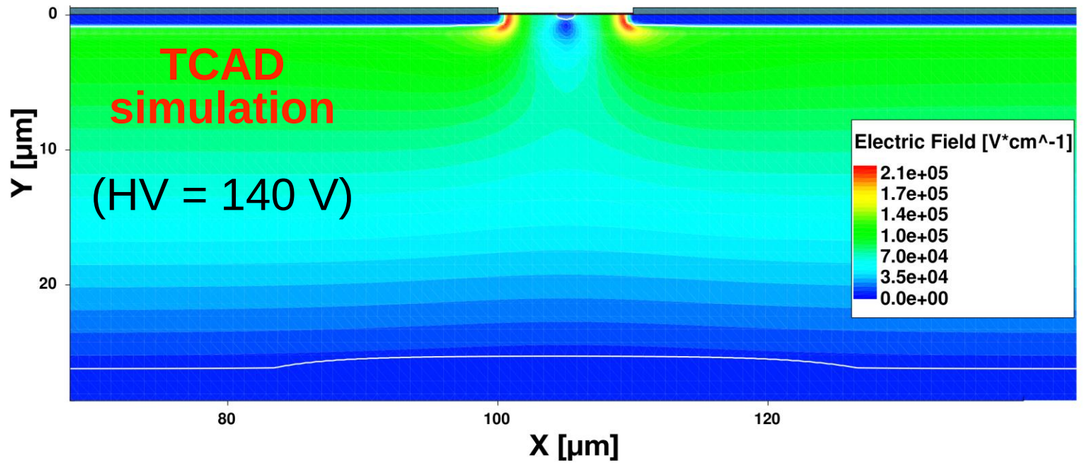
Standard substrate resistivity ρ = 50 Ωcm
No backside metallisation ⟹ **not fully depleted**
PRO: much easier **production**, but

➞ slightly degraded performance because of regions where drift velocity is not saturated

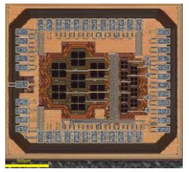
Depletion depth is **26µm** at HV = 140 V

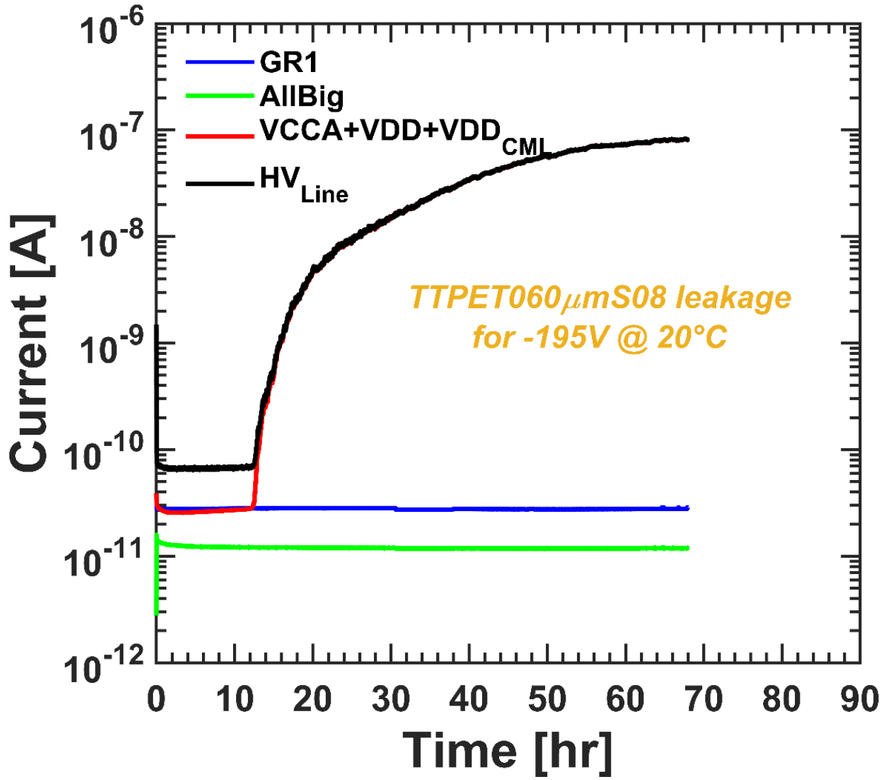
➞ Most probable deposited charge for a MIP **≈ 1600 electrons**

➞ CADENCE Spectre simulation for 1600e⁻ (0.25 fC): ideally, **ToA jitter = 22 ps**

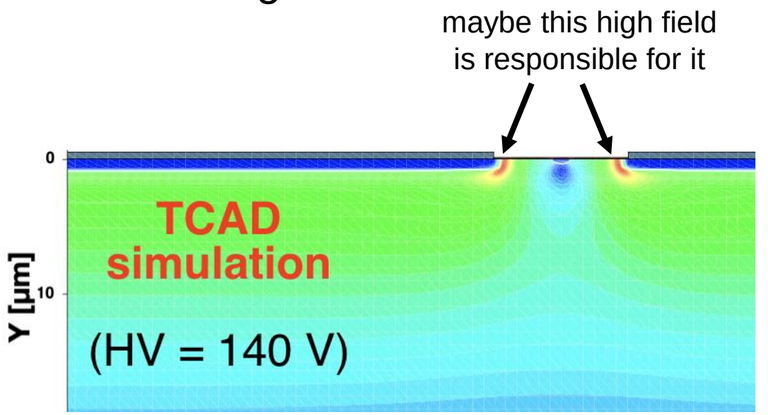


CAVEAT:





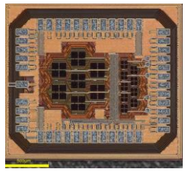
- Current drift up to ~100nA after two days of continuous operation.
- reversible.
- under investigation

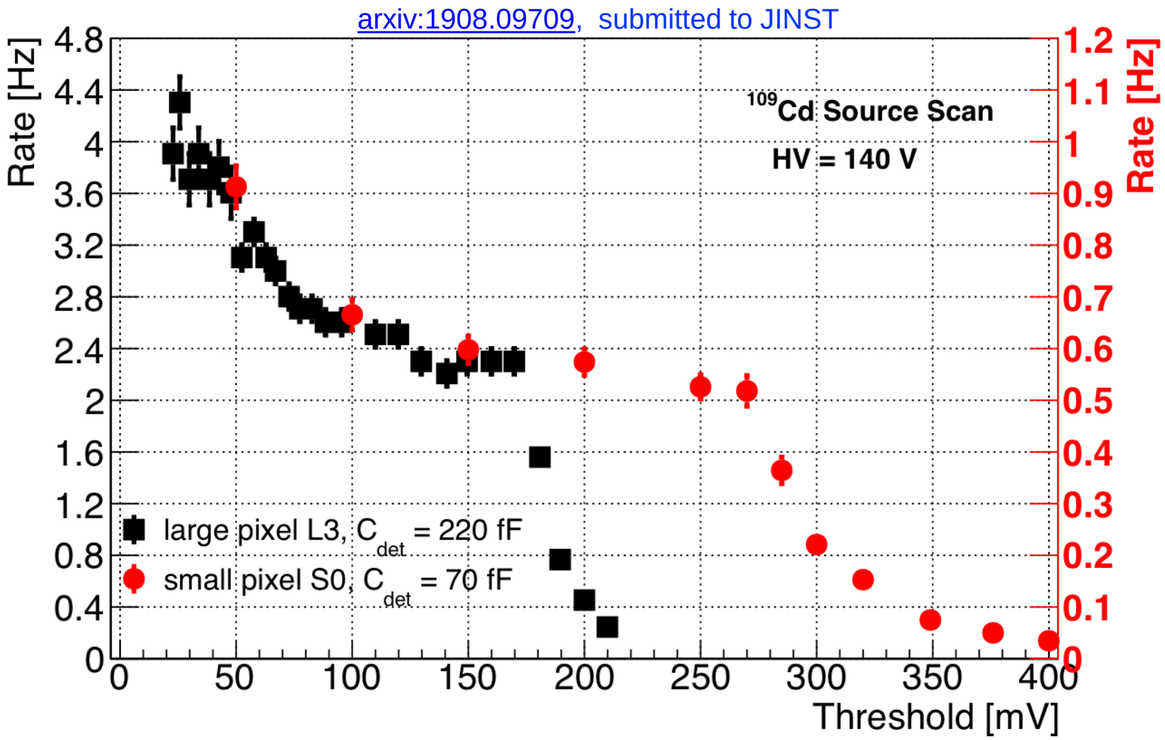


This behaviour does not compromise the chip performance.

Therefore, we made measurements with a source and at a testbeam

^{109}Cd radioactive source calibrations



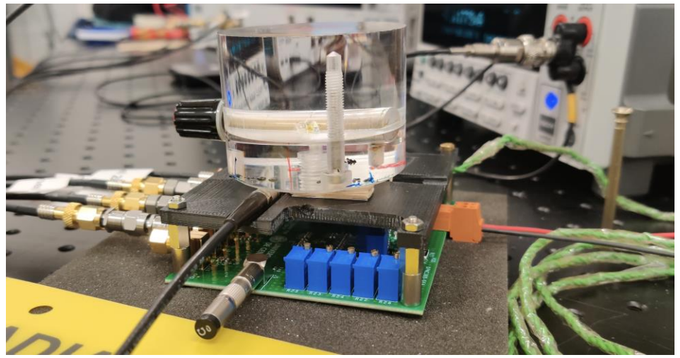


Rate ≈constant for low thresh. values ⟹ good discrimination of γ peak.

^{109}Cd photons (~22 keV) energetic enough for measurement of the gain:

- A_Q = 290 mV fC^{-1} for the small pixel ⟹ ENC = σ_V/A_Q = 90 electrons
- A_Q = 185 mV fC^{-1} for the large pixel ⟹ ENC = σ_V/A_Q = 160 electrons

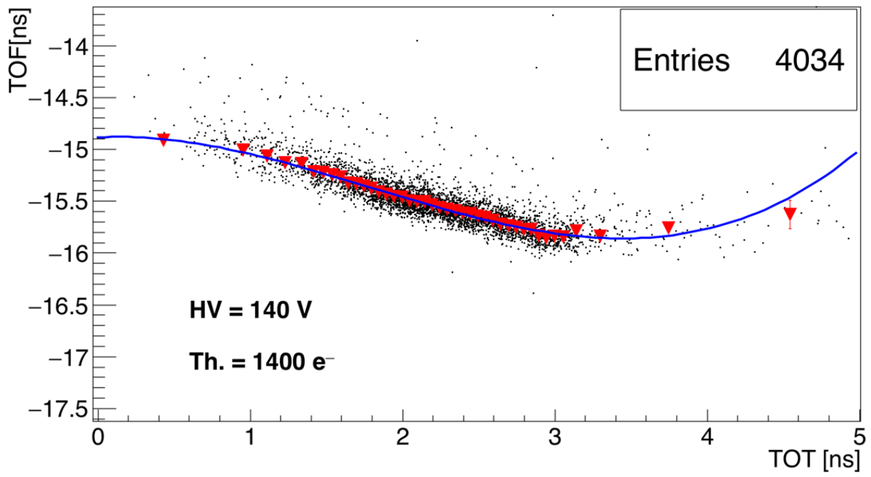
^{90}Sr source experimental setup



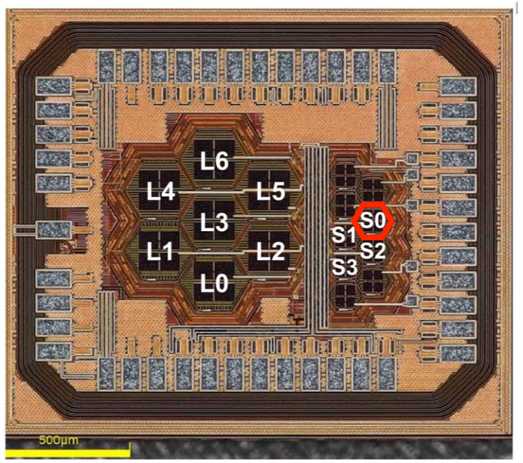
No analysis selection applied to the events in our monolithic SiGe prototype

Time-walk correction and TOF

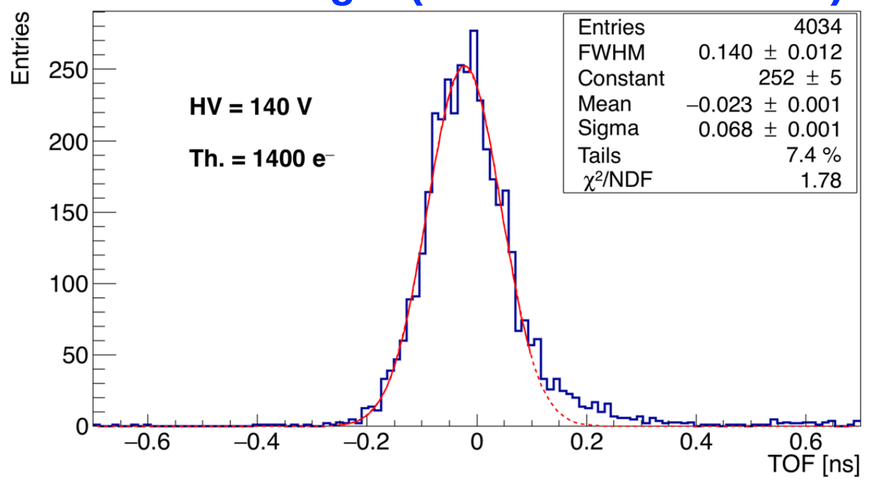
Time-walk correction



Small pixel S0, C = 70 fF



Time of Flight (time-walk corrected)



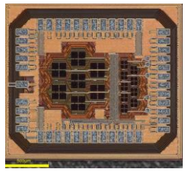
non-Gaussian tail (≈10%) for TOF ≥ 100ps, maybe due to e⁻ from the ^{90}Sr source

crossing the 10µm region between two pixels. Requires to be investigated in a testbeam.

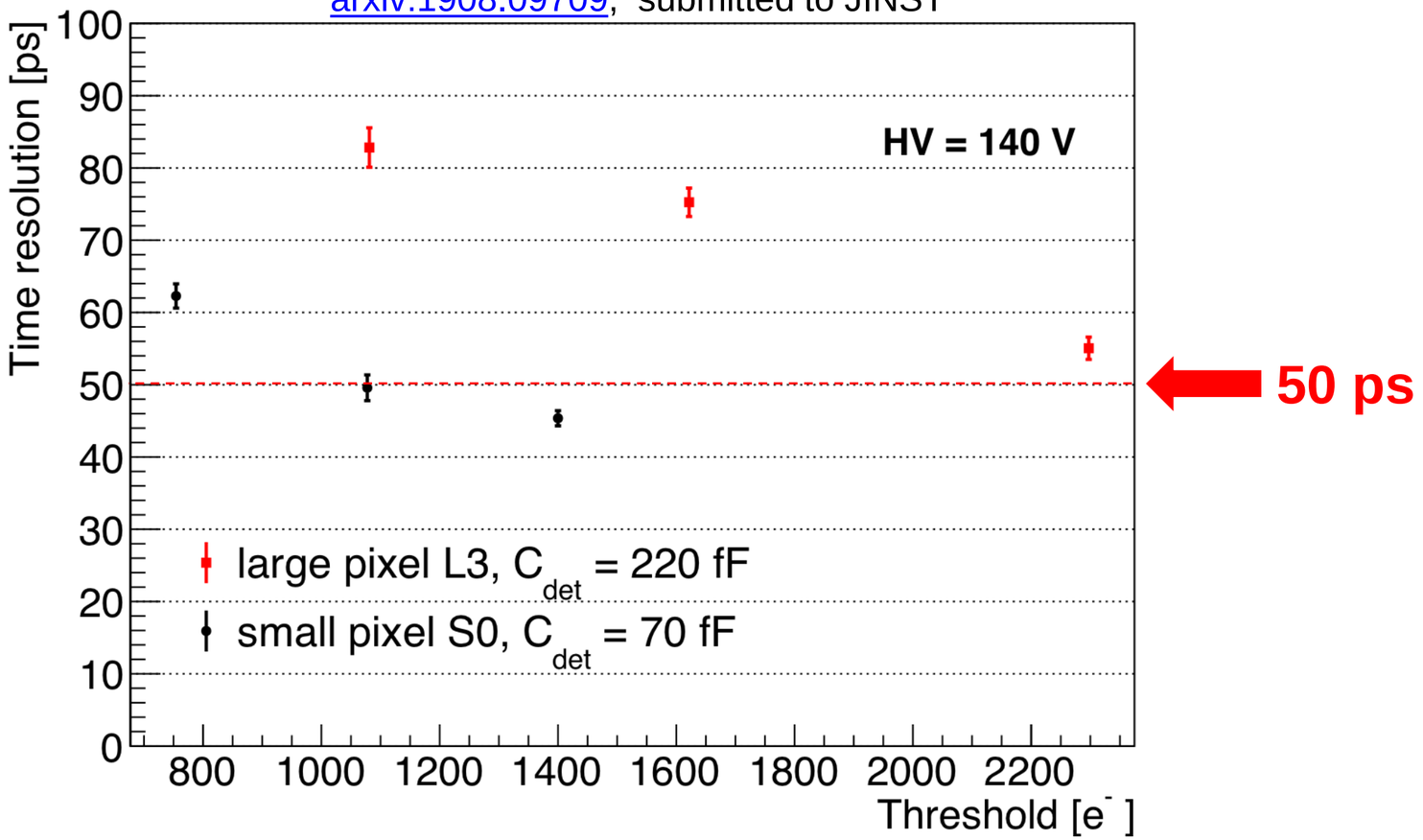
Time resolution of Gaussian part:

$$\sqrt{68^2 - 50^2} \simeq (46 \pm 2)\text{ps}$$

Time resolution vs. threshold

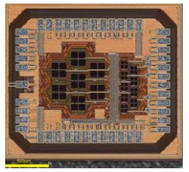


arxiv:1908.09709, submitted to JINST

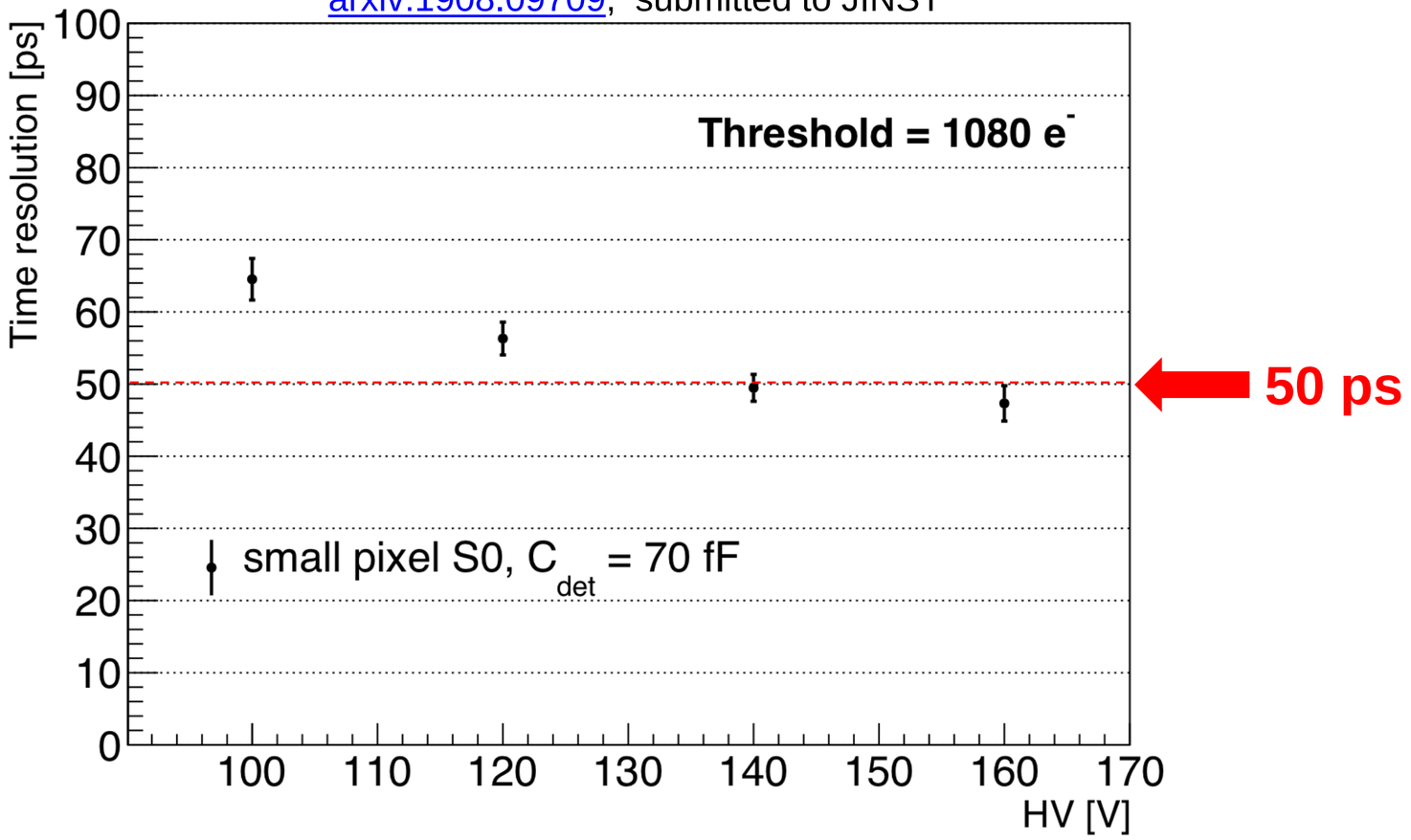


50 ps

Time resolution vs. HV

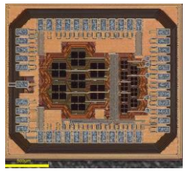


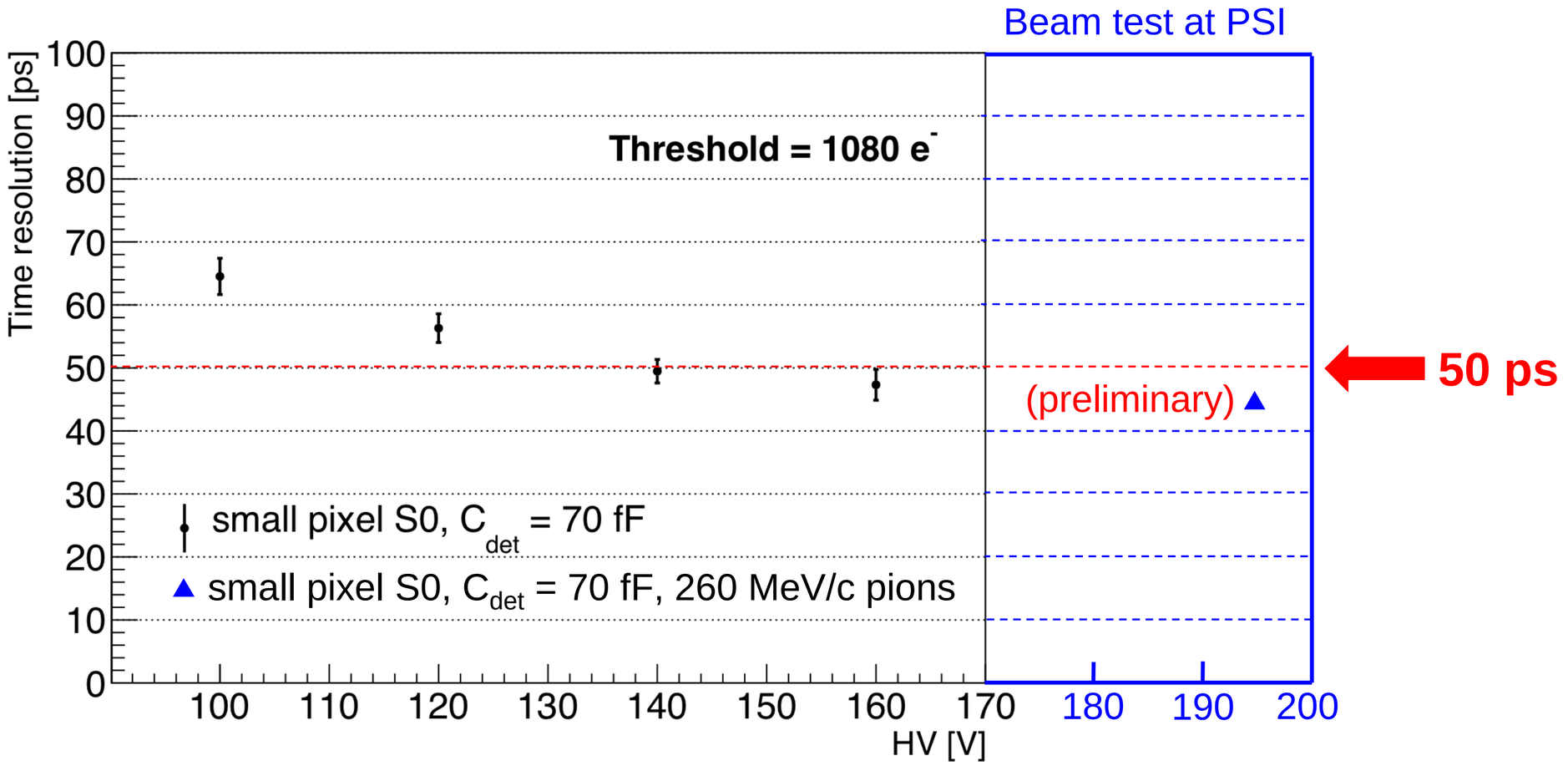
arxiv:1908.09709, submitted to JINST



50 ps

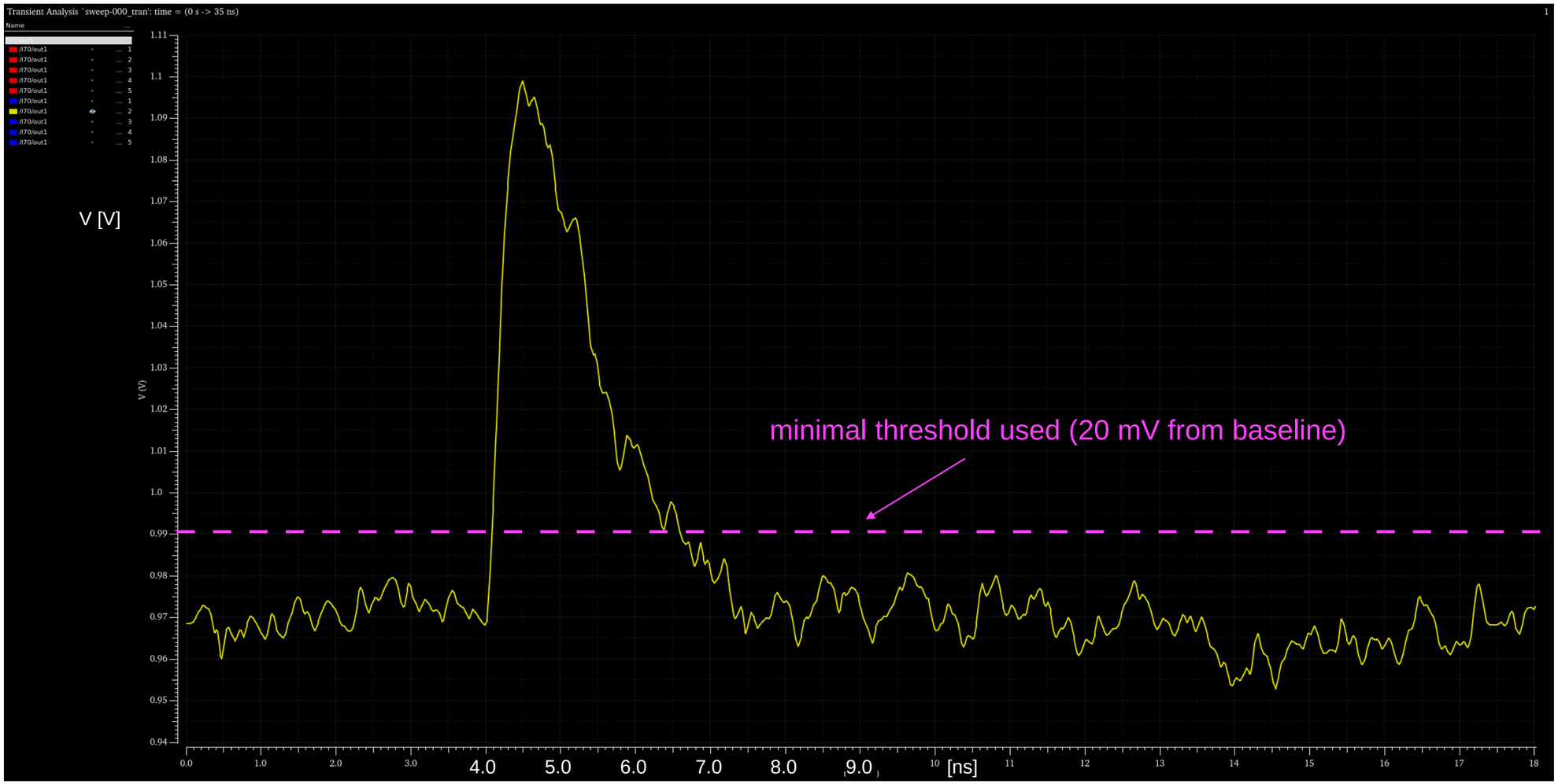
Time resolution vs. HV



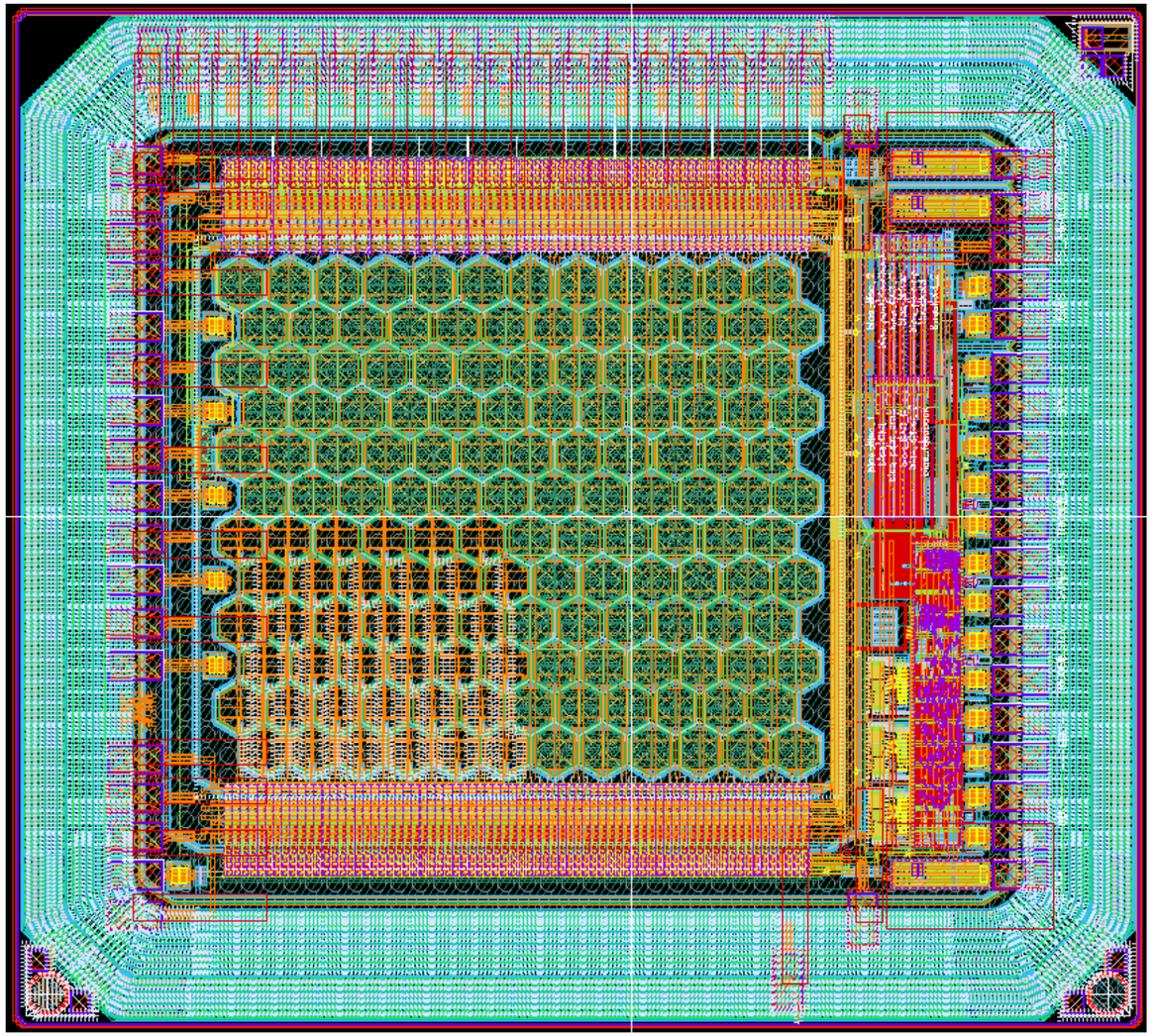


CADENCE simulation

Signal in the hexagonal small pixels:



Next steps



CONCLUSIONS

- **Timing** capability of silicon still to be fully exploited
- **SiGe HBT** allows for low-noise and fast amplifiers and picosecond readout
- **Monolithic** ASICs in IHP 130nm SiGe processes without internal gain provided
  - **full efficiency**
  - **excellent time resolution**: 220 → 115 → 50 ps RMS → ???

Publications and patents

Articles:

- Hexagonal small-area pixels — arxiv:1908.09709, submitted to JINST
- TT-PET demonstrator chip testbeam: JINST 14 (2019) P02009, https://doi.org/10.1088/1748-0221/14/02/P02009
- TT-PET demonstrator chip design: JINST 14 (2019) P07013, https://doi.org/10.1088/1748-0221/14/07/P07013
- First TT-PET prototype: JINST 13 (2017) P02015, https://doi.org/10.1088/1748-0221/13/04/P04015
- Proof-of-concept amplifier: JINST 11 (2016) P03011, https://doi.org/10.1088/1748-0221/11/03/P03011

- TT-PET engineering: arxiv:1812.00788
- TT-PET simulation & performance: arxiv:1811.12381

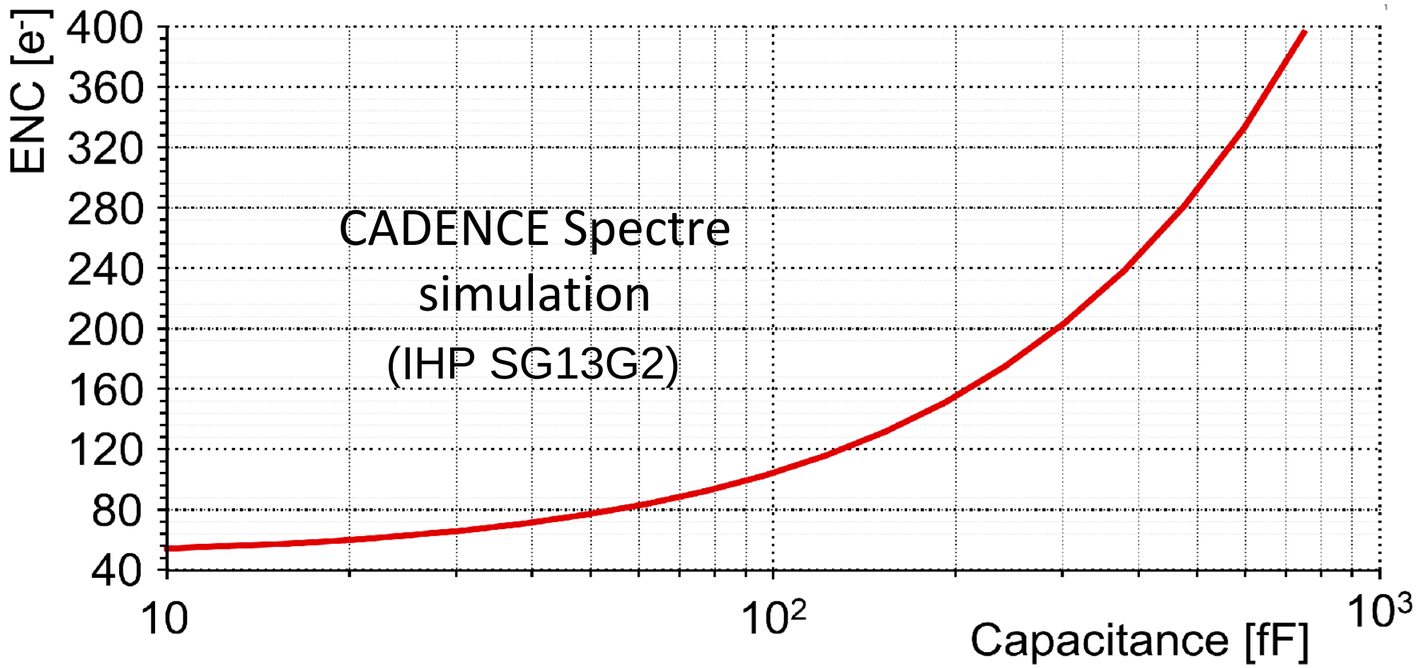
Patents:

- PLL-less TDC & synchronisation System: EU Patent EP18181123.3
- Picosecond Avalanche Detector (pending): EU Patent Application EP18207008.6

Extra Material

Towards **1 ps** time resolution: SiGe electronics

Performance of our **present** electronics

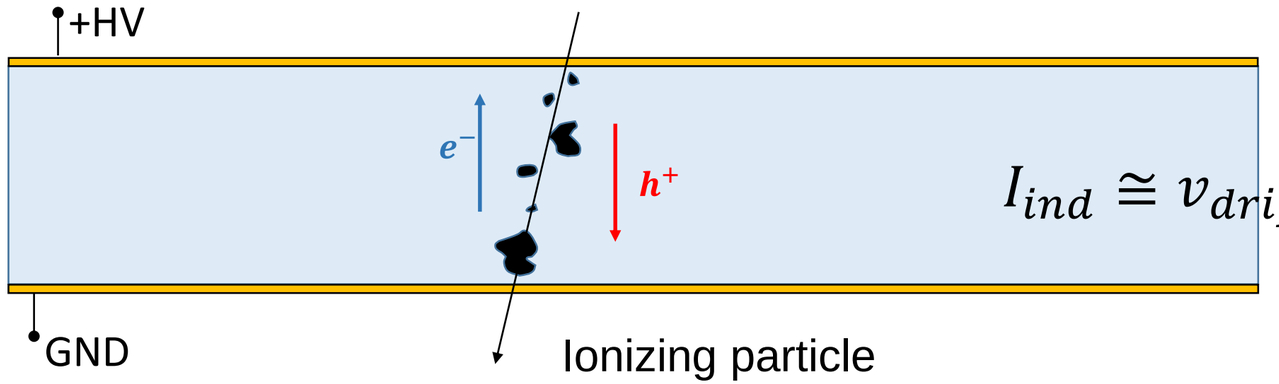


Frontend ENC (CADENCE simulation):

80 e^- RMS for C_{in} = 50 fF and Gain = 30 $\Longrightarrow$ σ_{time} = 4 ps

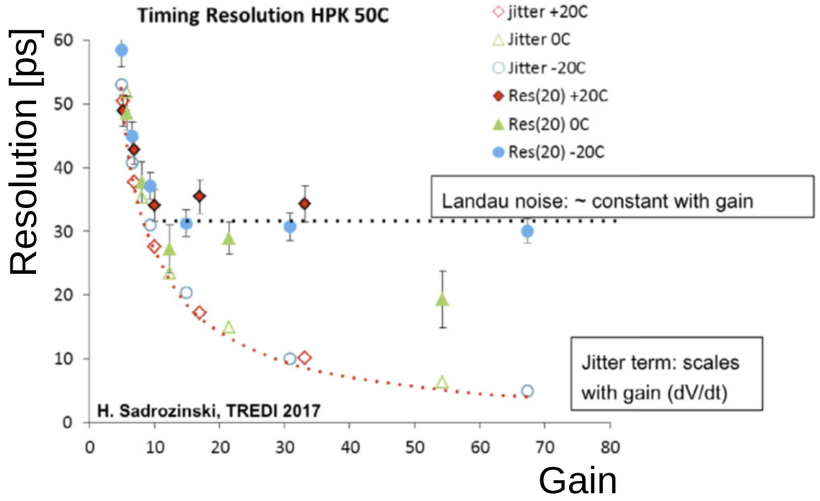
We are working on new version of FE electronics and on a ps TDC

Towards **1 ps** time resolution: Landau noise



$$I_{ind} \cong v_{drift} \frac{1}{D} \sum_i q_i$$

Landau fluctuations of the charge deposition constitute an irreducible effect of standard PN-junction sensors



N. Cartiglia et al., NIM A 924 (2019) 350-354

Need for a **novel** silicon sensor to go beyond this ⟹

Towards **1 ps** time resolution

We designed a new sensor, the

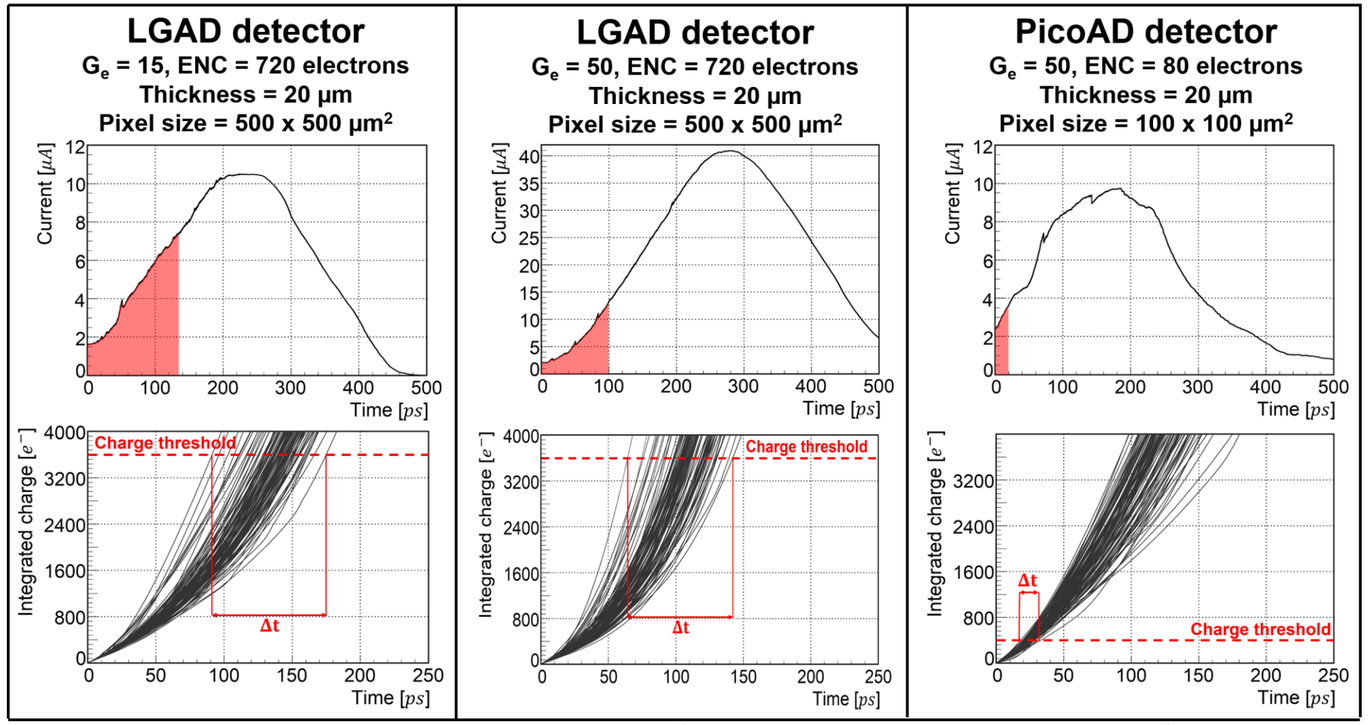
PicoAD: Picosecond Avalanche Detector

Patent pending (EP 18207008.6)

The PicoAD time resolution

One order of magnitude better than present best results

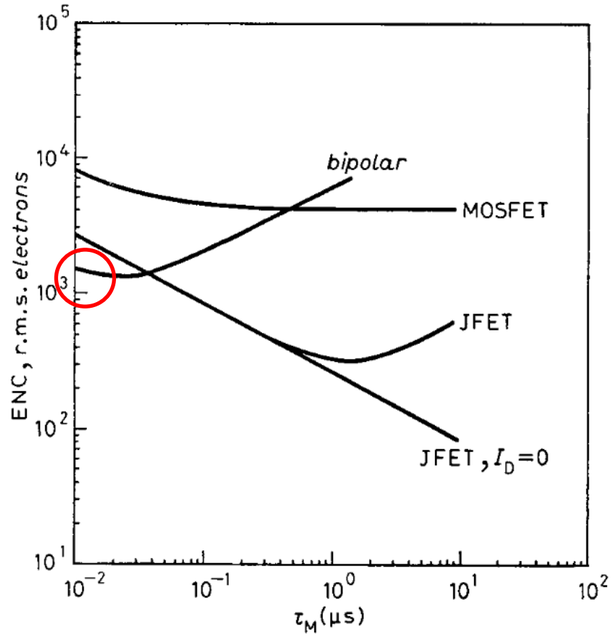
GEANT4 + TCAD + CADENCE Spectre **simulation**



LGAD read out by our SiGe HBT ultra-fast low-noise electronics

PicoAD

Bipolar transistors for fast low-noise amplifiers



E. Gatti, P. F. Manfredi, *Processing the Signals from Solid-State Detectors in Elementary-Particle Physics*, rivista del Nuovo Cimento Vol. 9, No. 1 (1986).

It is known since a long time that for BJT technology the Equivalent Noise Charge (ENC) depends on the capacitance C_{tot} and the integration time τ as follows:

$$ENC = \sqrt{k_1 \cdot \tau + k_2 \cdot \frac{C_{tot}^2}{\tau} + k_3 C_{tot}^2}$$

parallel noise

dominating term: series noise

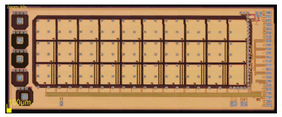
1/f noise

BJT technology: can provide a fast integrator that minimises series noise

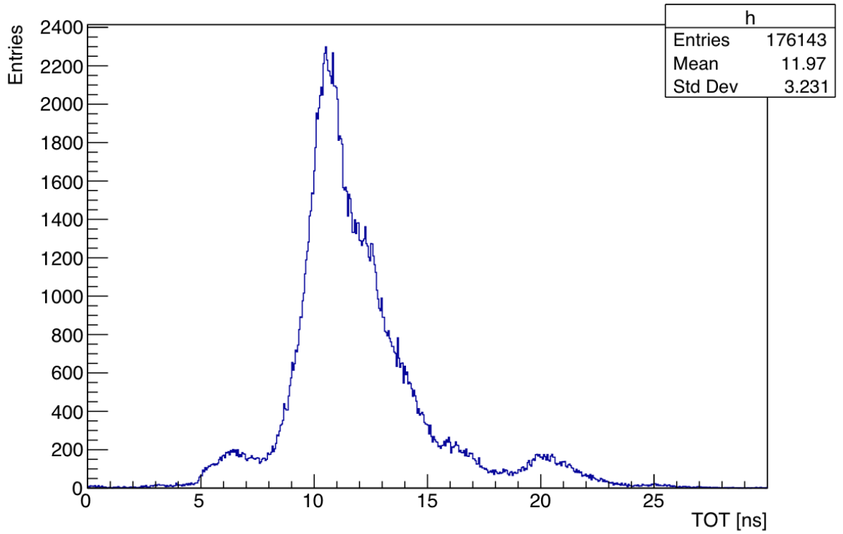
↓

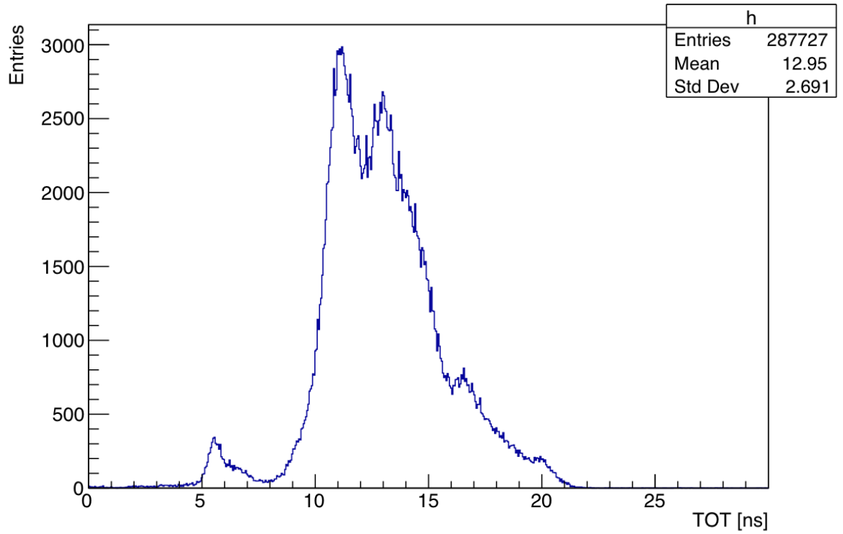
to produce fast and low-noise amplifiers

CAVEAT 2: TOT distribution



It was found that **the single-ended digital trigger signal** affected the grounding of the pixel matrix and induced a small residual noise.
Consequence: the TOT distributions show **peaks**, with time difference between peaks caused by the delay of the fast-OR line.



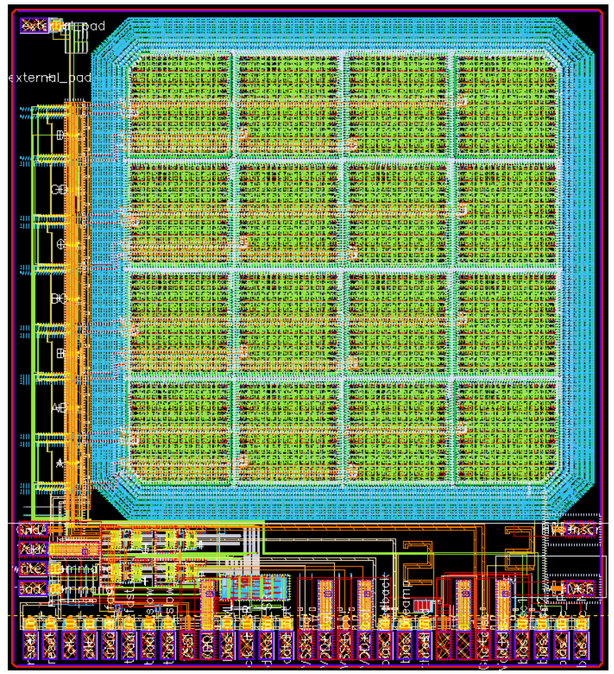


This modulation of the TOT distribution **degrades** the time-walk correction, and therefore **the time resolution**

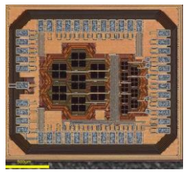
Mitigation measure: introduction of **trigger signals in a differential configuration**

- These two caveats are fixed in a new chip, that we just received back from IHP.

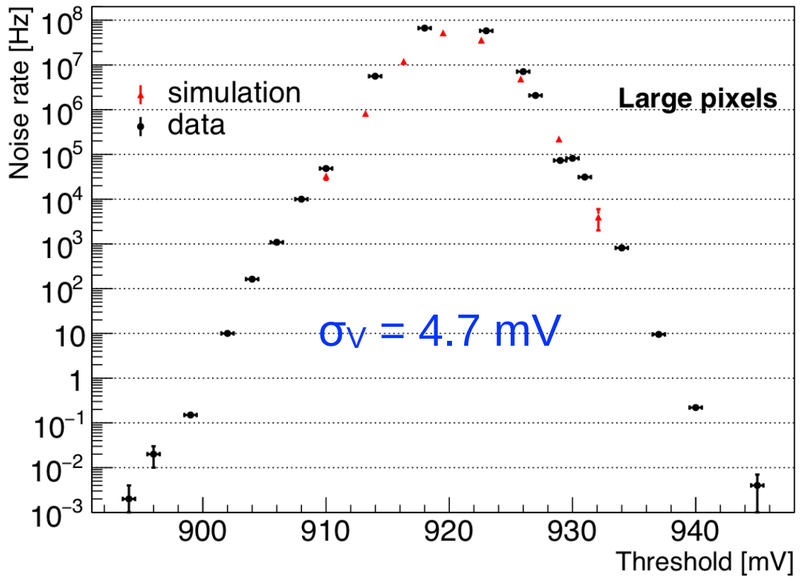
- The chip contains also front-end test structures:
  - peak-sensing fast ADC
  - higher gain pre-amp
  - new differential driver



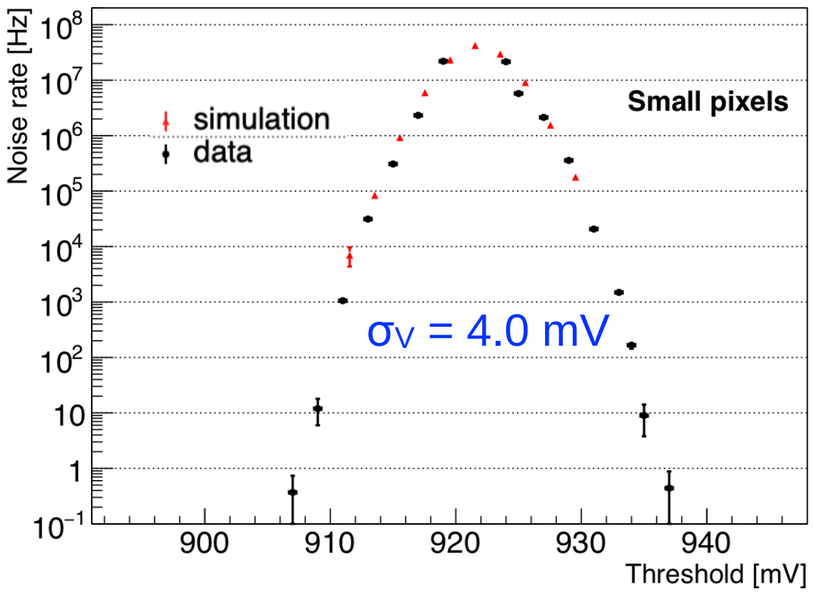
Noise rates



Large pixels (220 fF)

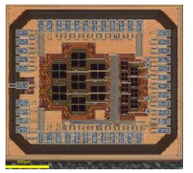


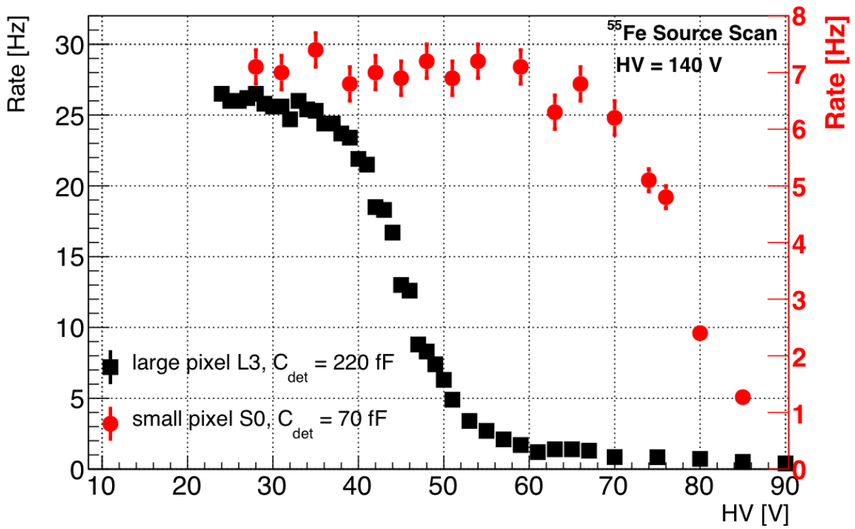
Small pixels (70 fF)

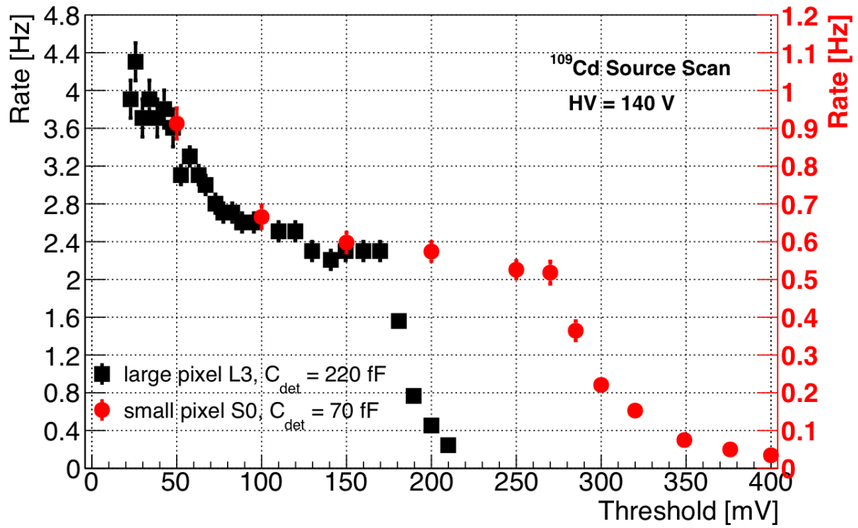


Measured noise rates agree well with CADENCE Spectre simulation

^{55}Fe and ^{109}Cd source calibrations



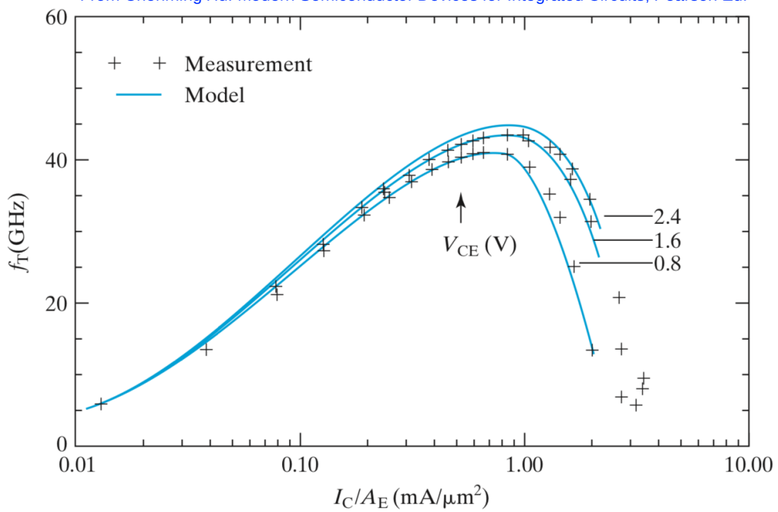




Time resolution vs. power consumption

f_T depends on the collector current I_c
(that is proportional to the power: $P = I_c \cdot V_{cc}$)

From Chenming Hu: Modern Semiconductor Devices for Integrated Circuits, Pearson Ed.



The charge gain can be written as:

$$A_Q = \frac{1}{C_f + \frac{C_{det}}{|A_V|}}$$

In our case, the capacitance C_f between the Base and the Collector of the HBT is much smaller than the detector capacitance: $C_{det}/|A_V| \gg C_f$

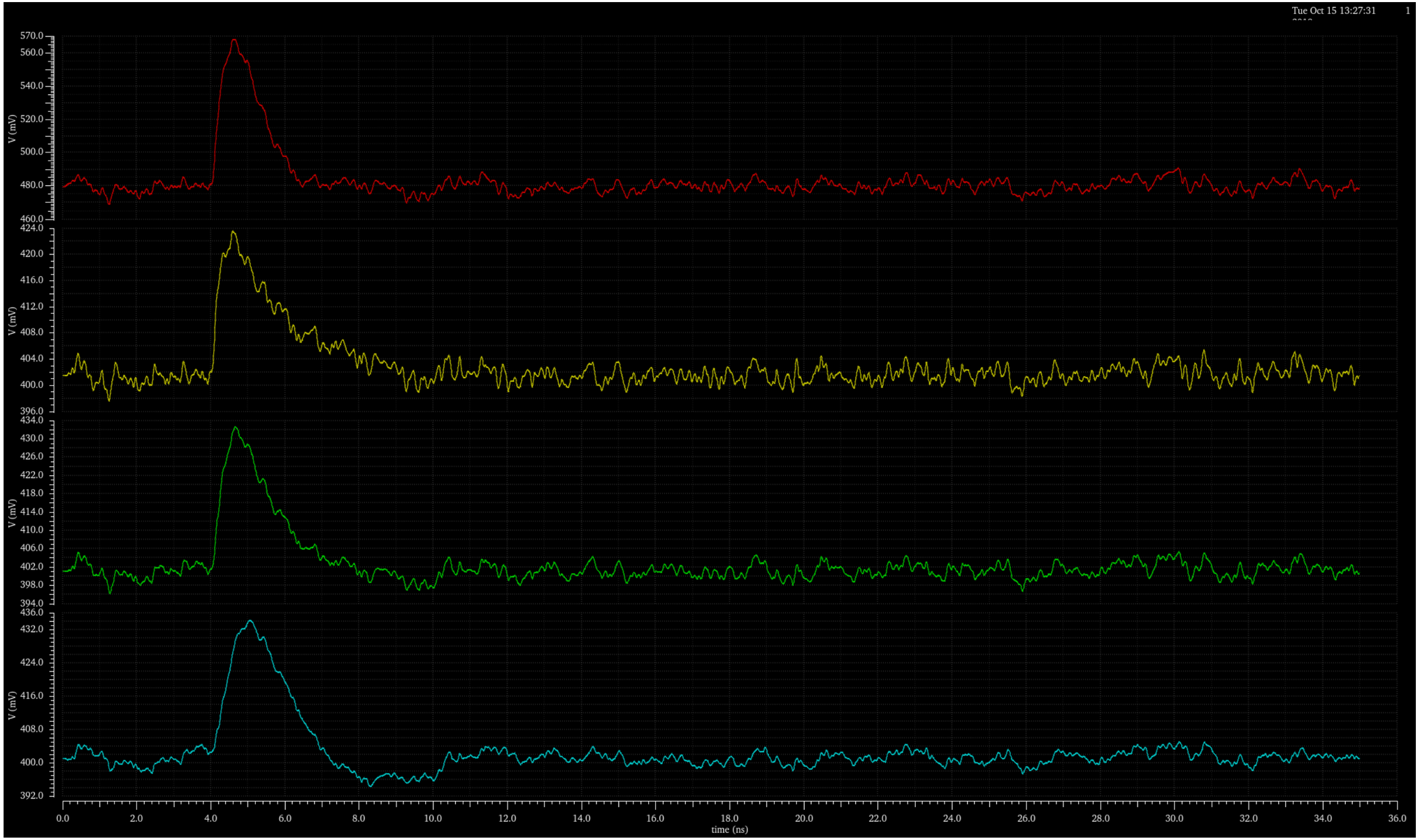
Therefore, since A_V is proportional to f_T:
larger power $\Longrightarrow$ larger f_T $\Longrightarrow$ larger A_V $\Longrightarrow$ smaller ratio $C_{det}/|A_V|$ $\Longrightarrow$ higher A_Q

150, 2.5

150, 1.2

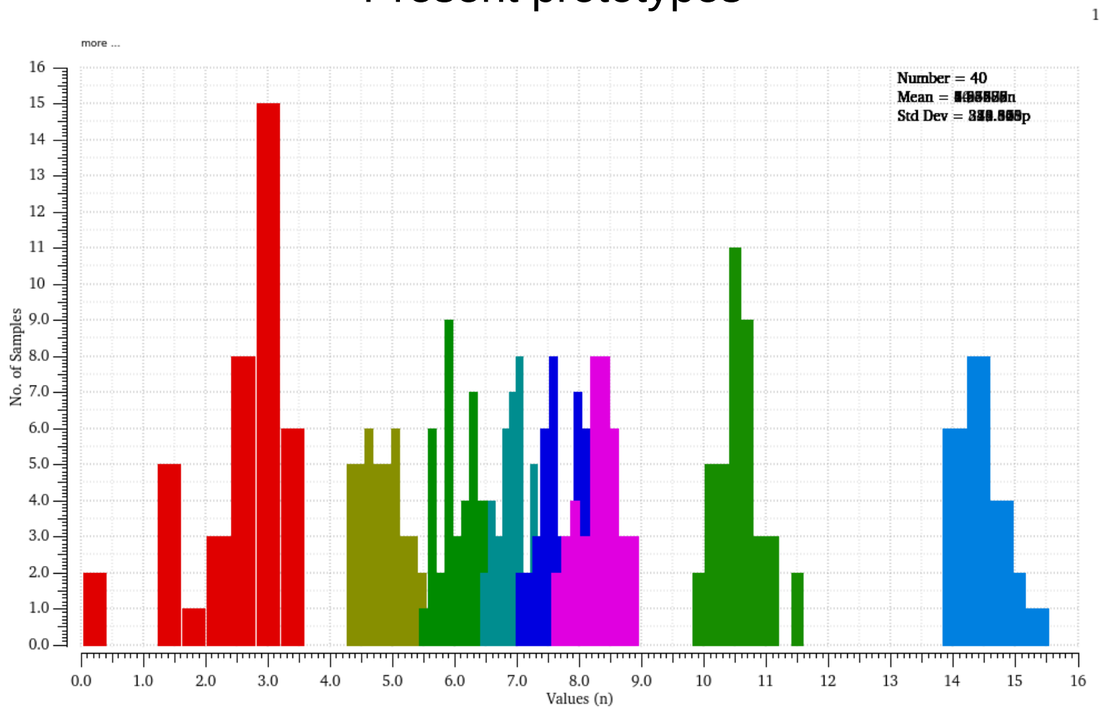
50, 1.2

20, 1.2



Improvement of time walk correction

Present prototypes



New technique