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Recent depleted CMOS developments within the CERN-RD50 framework

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RD50

CERN-RD50 – Depleted CMOS programme

- **Depleted CMOS sensors** have huge potential for future experiments in physics
- **CERN-RD50 programme** to develop and study these sensors with high priority
- The programme includes
  - ➔ ASIC design
  - ➔ TCAD simulations
  - ➔ DAQ development
  - ➔ Performance evaluation
- It involves
  - ➔ ~ 25 people
  - ➔ ~ 12 institutes

RD50-MPW1 – Submission

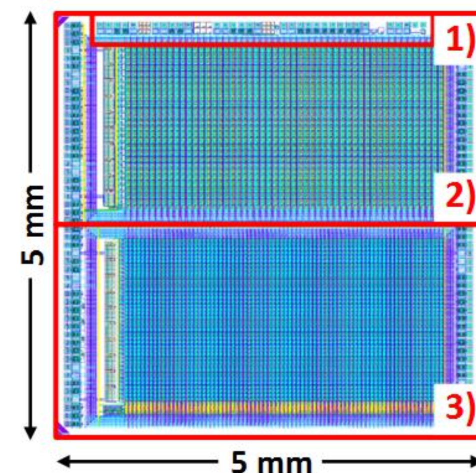
RD50-MPW1 - General design details

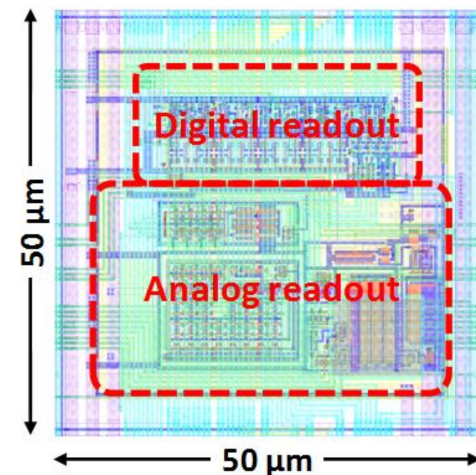
- MPW in the **150 nm HV-CMOS process from LFoundry**
- Submitted in November 2017 and received in April 2018
- To gain expertise, test the process and test novel designs
- Fabricated using 2 different substrate resistivities
  - ➔ 500 Ω·cm (40 samples) and 1.9k Ω·cm (80 samples)

RD50-MPW1 – Chip contents

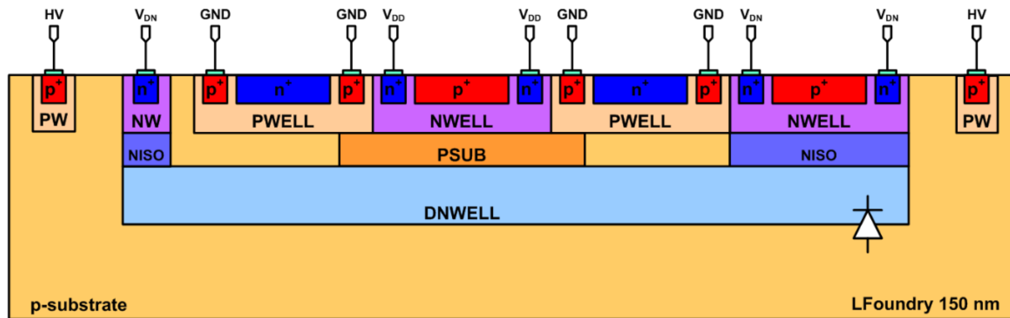
1) Tests structures for e-TCT and C_{DET} measurements
2) Matrix of depleted CMOS pixels with 16-bit counter
   - ➔ 26 x 52 pixels
   - ➔ 75 µm x 75 µm pixel area
   - ➔ For photon counting applications (proof-of-concept)
3) Matrix of depleted CMOS pixels with FE-I3 style readout
   - ➔ 40 x 78 pixels
   - ➔ 50 µm x 50 µm pixel area
   - ➔ For particle physics applications

- Analog and digital readout embedded in the sensing area
- Completely independent matrices

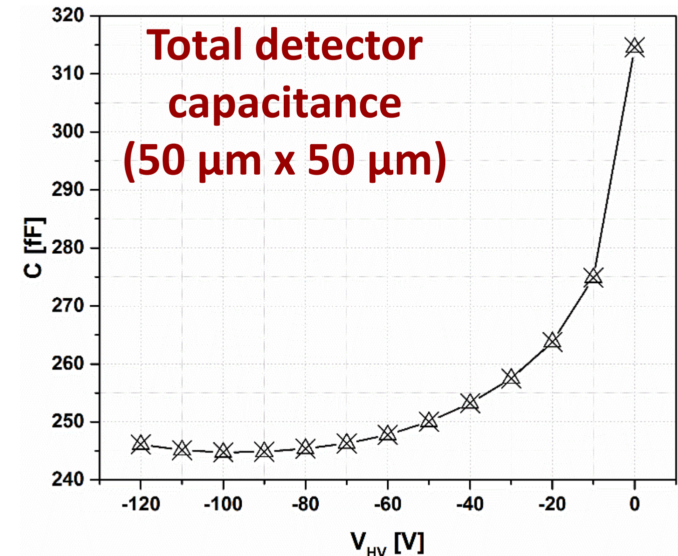


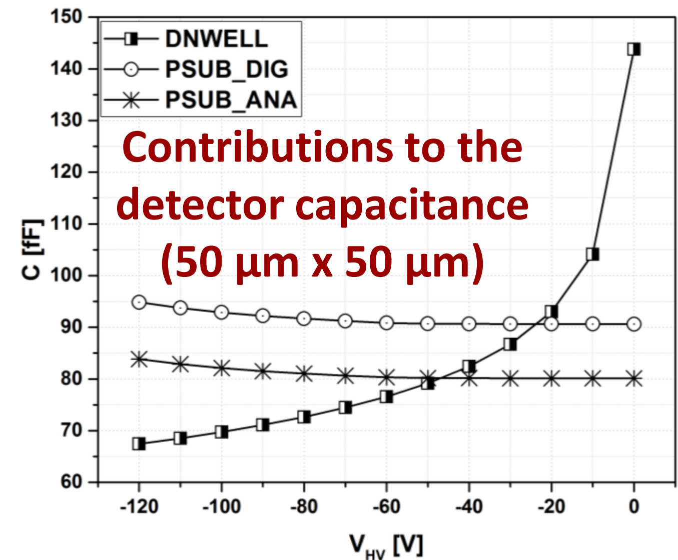


RD50-MPW1 – Pixel cross-section

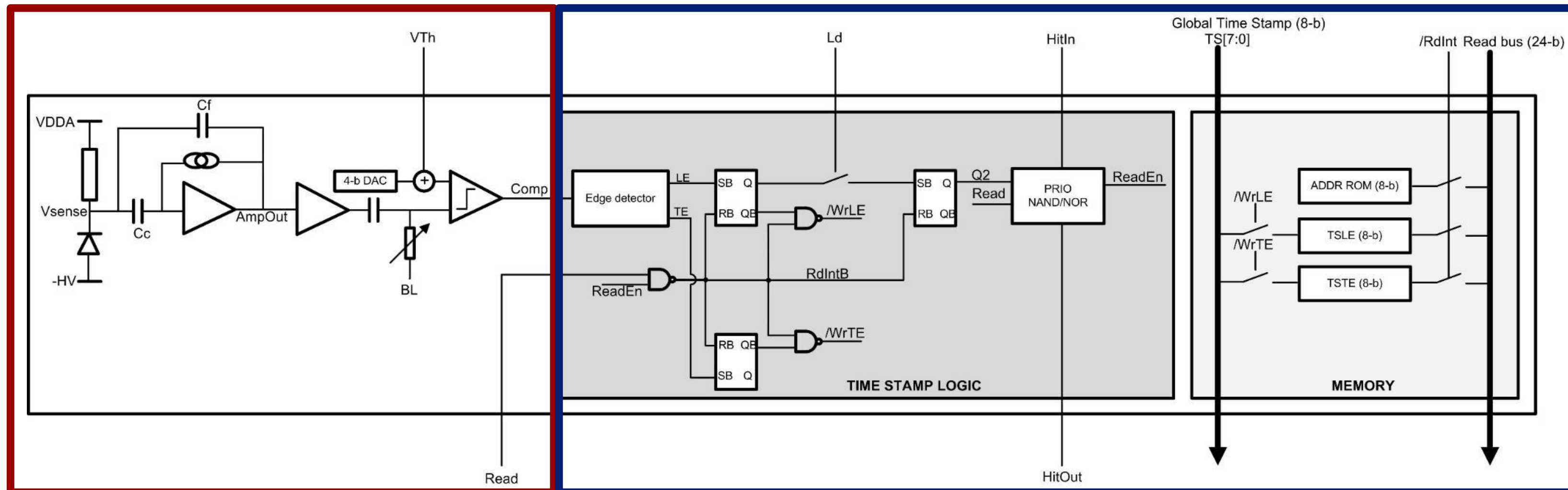


- Large fill-factor pixel
- PSUB layer isolates NWELL from DNWELL
  - ➔ CMOS electronics in pixel area are possible
- Detector capacitance has 2 contributions
  - ➔ P-substrate/DNWELL
  - ➔ PSUB/DNWELL
  - ➔ Total capacitance ~ 250 fF
- Equivalent Noise Charge (ENC) ~ 100 – 120 e^-





RD50-MPW1 – Pixel readout electronics



Analog readout

- Sensor biasing circuit, CSA, RC-CR filters and CMOS comparator
- CSA with programmable discharging current
- CMOS comparator with global V_{Th} and local 4-bit DAC for fine tuning

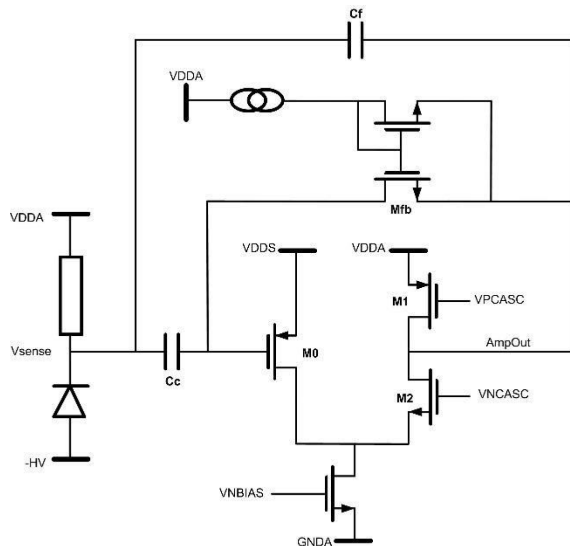
Total power consumption is ~ 23 μW

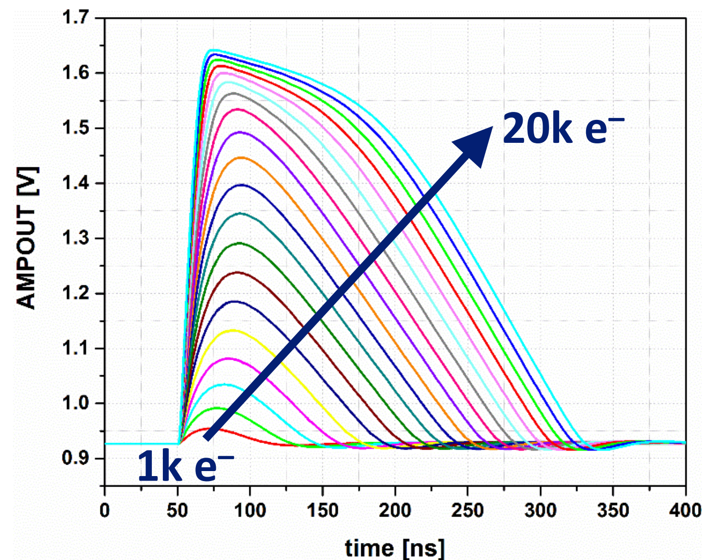
Digital readout

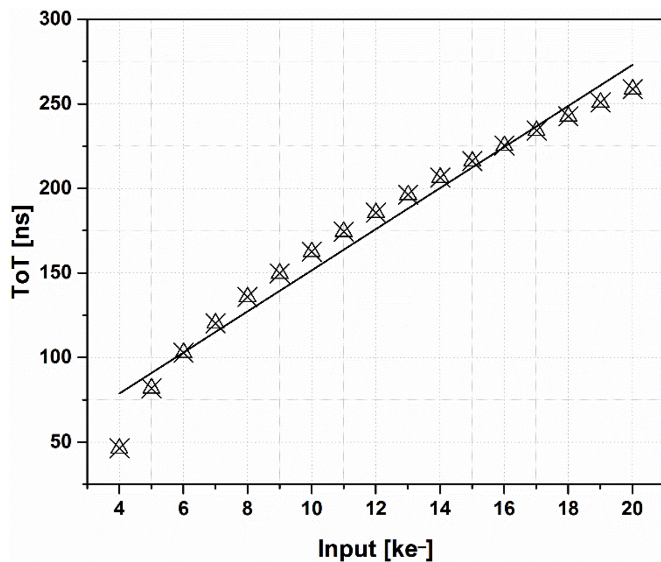
- Column drain readout (synchronous, triggerless, hit flag + priority encoding)
- Global 8-bit Gray encoded time-stamp (40 MHz)
- For each hit
  - ➔ Leading edge (LE): 8-bit DRAM memory
  - ➔ Trailing edge (TE): 8-bit DRAM memory
  - ➔ Address (ADDR): 6-bit ROM memory

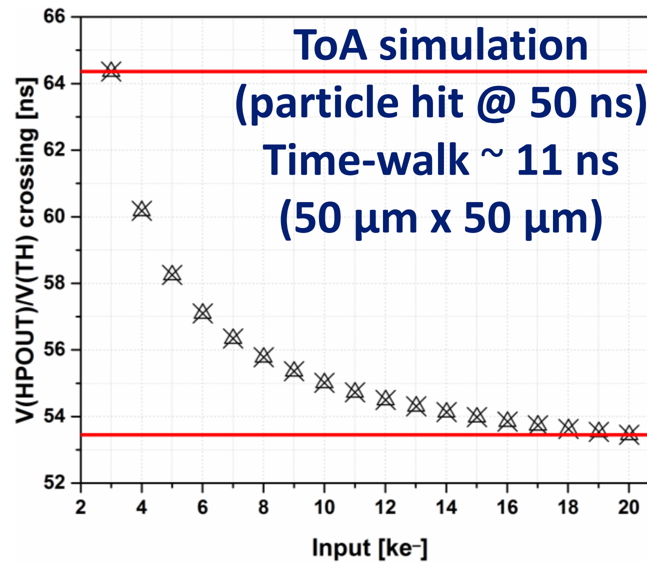
} ToT = LE – TE (off-chip)

RD50-MPW1 – Pixel readout electronics



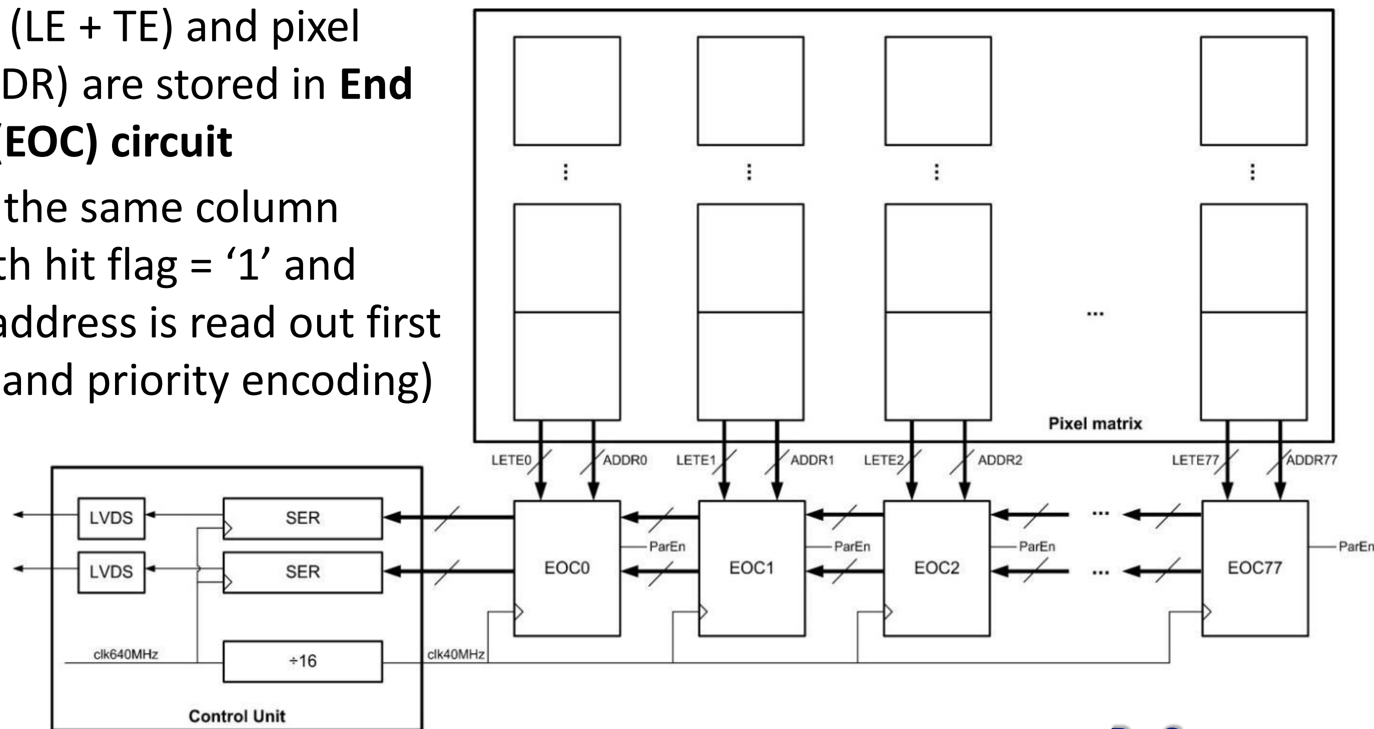






RD50-MPW1 – Readout architecture

- Time-stamp (LE + TE) and pixel address (ADDR) are stored in **End Of Column (EOC) circuit**
- If > 1 hits in the same column
  ➔ Pixel with hit flag = '1' and largest address is read out first (hit flag and priority encoding)



R. Casanova, TWEPP 2019

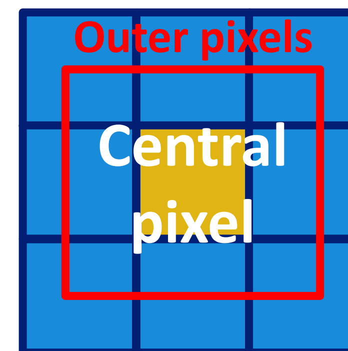
- Shift register with 78 EOC circuits (one EOC per column) @ 40 MHz
- **Continuous readout sequence**:
  1) LE, TE and ADDR of the hit pixel with hit flag = '1' and highest priority stored in EOC (1 clock cycle)
  2) CU reads sequentially the data stored in each EOC @ 40 MHz (78 clock cycles)
  3) Serializers send data off-chip @ max. speed of 640 MHz

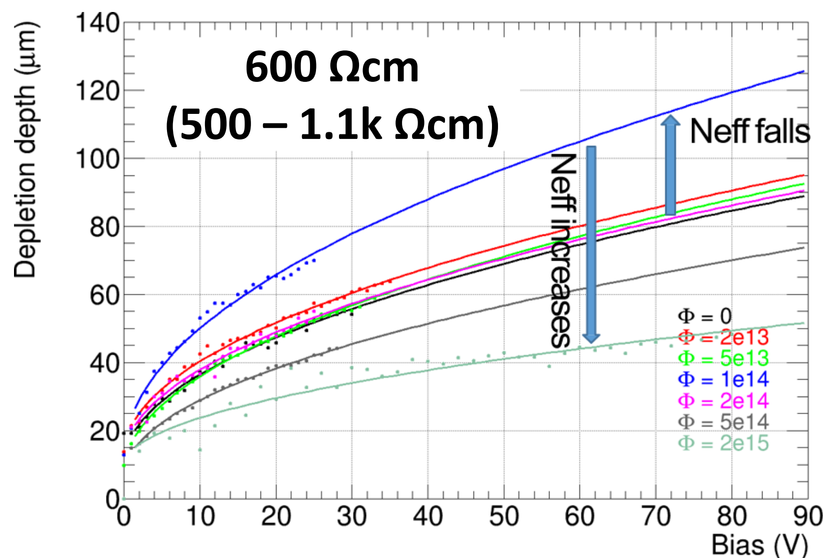
RD50-MPW1 – Measurements

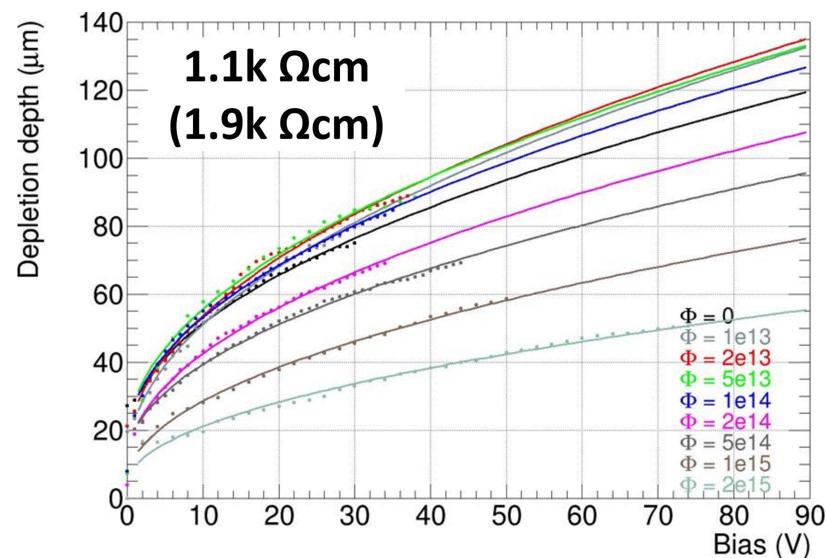
eTCT measurements to study sensor depletion region

I. Mandic, TREDI 2019

- Samples irradiated at TRIGA reactor in Ljubljana to several different n-fluences ranging from 1E13 to 2E15 n_{eq}/cm^2
- **Test structure**
  - ➔ 3 x 3 pixels matrix without readout electronics
  - ➔ Central pixel to read out
  - ➔ Outer pixels connected together
  - ➔ Pixel size is 50 µm x 50 µm



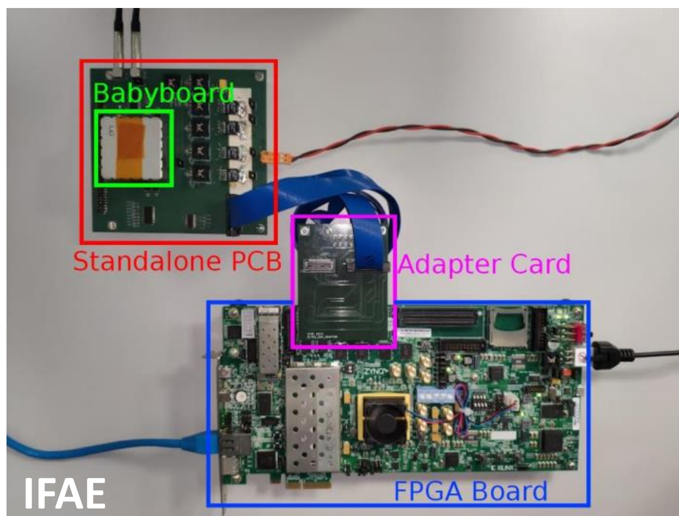




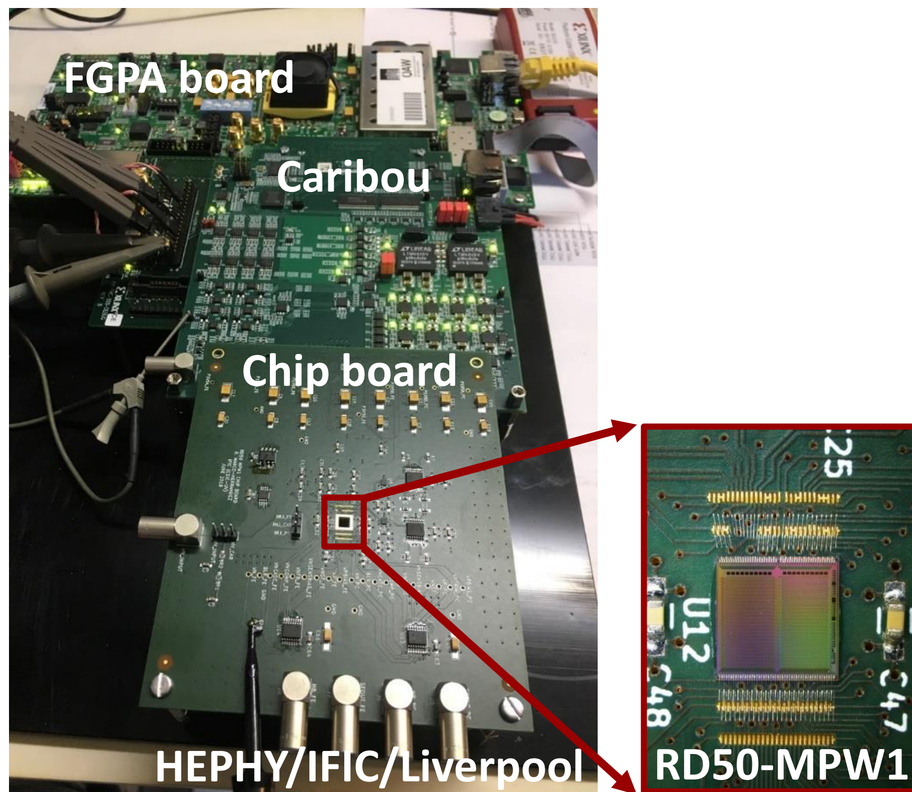
- Depletion depth changes with irradiation + acceptor removal effects seen

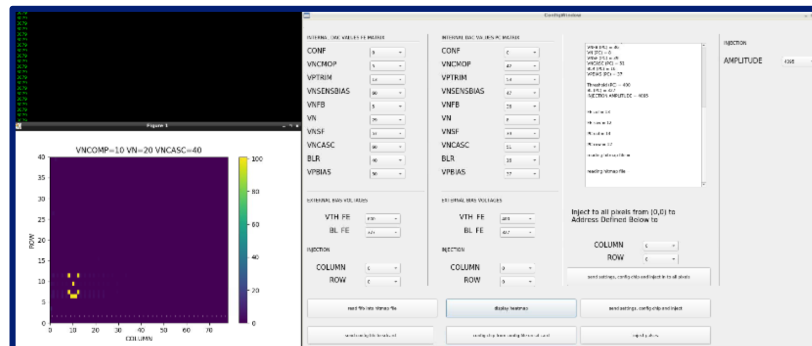
RD50-MPW1 – Experimental set-ups

2 experimental set-ups available



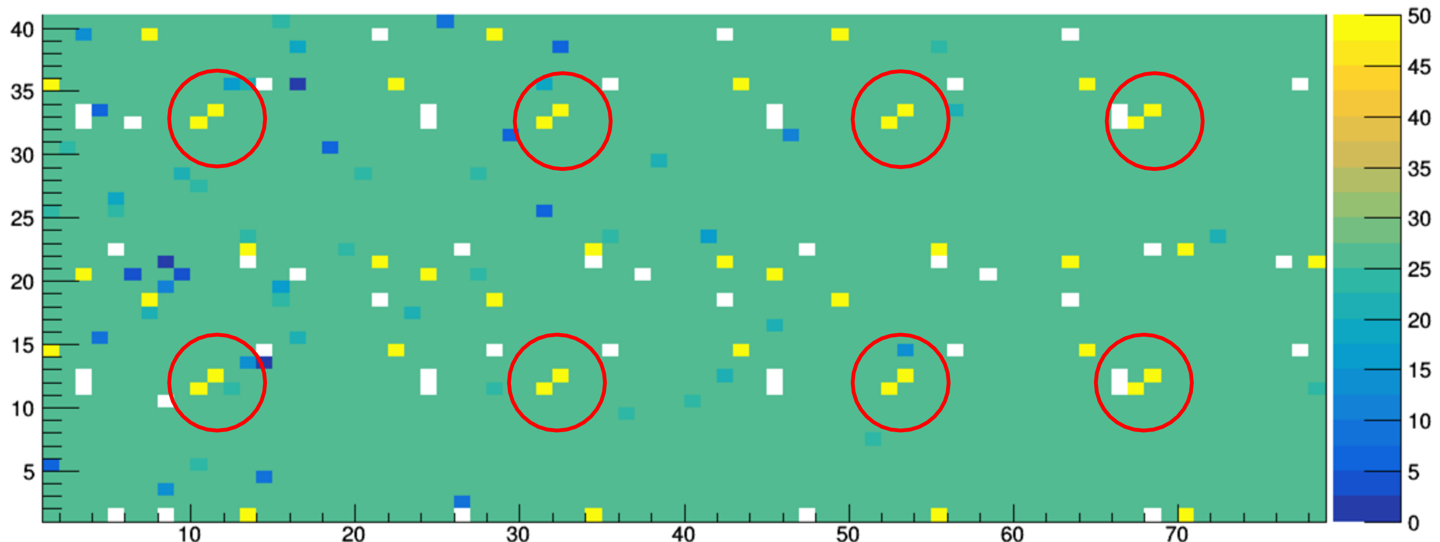
- RD50-MPW1
- Babyboard/chip board
- Standalone PCB/Caribou
- Adaptor card and/or FMC
- Xilinx ZC706 FPGA board
- User interface





RD50-MPW1 – Measurements

Hit map – Test pulse injection



- Test pulse injection to one selected pixel (before irradiation)
  - ➔ V_{test} = 1.5 V (square pulse)
  - ➔ 25 times per pixel
- Matrix readout
- Expected result ➔ 25 hits from each pixel
- Reality
  - ➔ > 25 hits from each pixel
  - ➔ There is crosstalk (address lines) + a few inefficient pixels
- Doing new chip simulations to understand this problem

F. Förster, RD50 WS 2019
R. Casanova, TWEPP 2019

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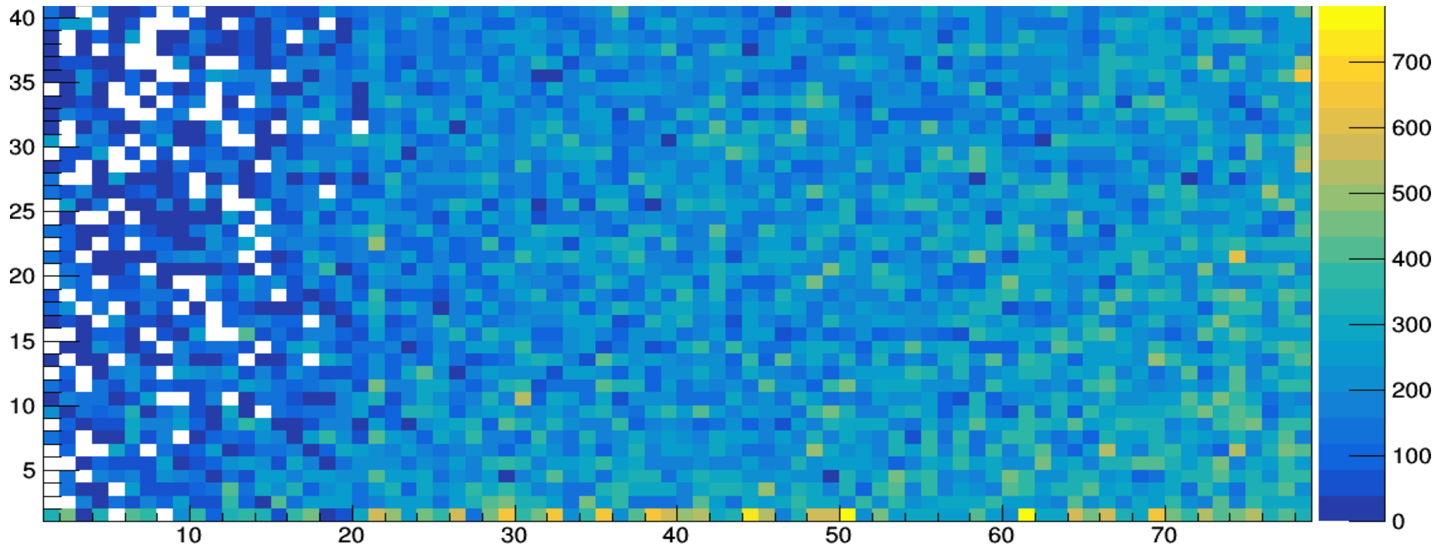
RD50-MPW1 – Measurements

Hit map – Sr90

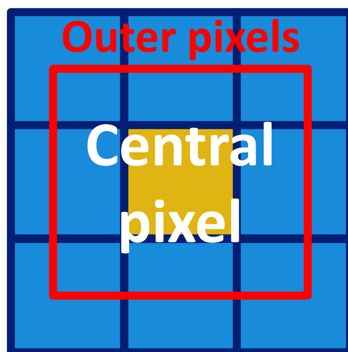


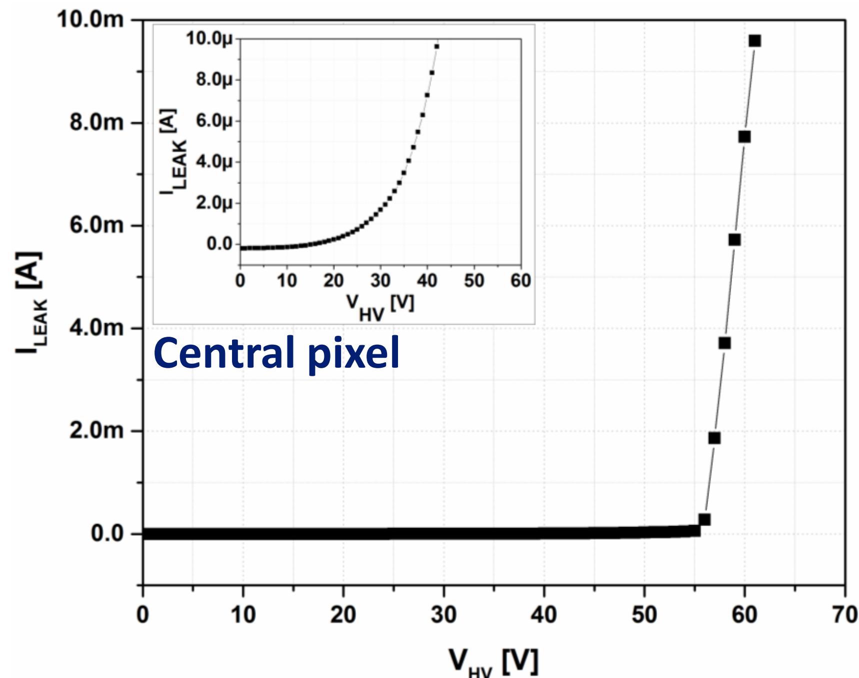
- Sr90 source placed on the centre of the matrix
  ➔ The matrix is small (~ 4 mm x 2 mm)
- Expected result ➔ Uniform matrix
- Reality ➔ Left / right asymmetry
- Studying possible voltage drops in the matrix

F. Förster,
RD50 WS 2019
R. Casanova,
TWEPP 2019

RD50-MPW1 – Measurements

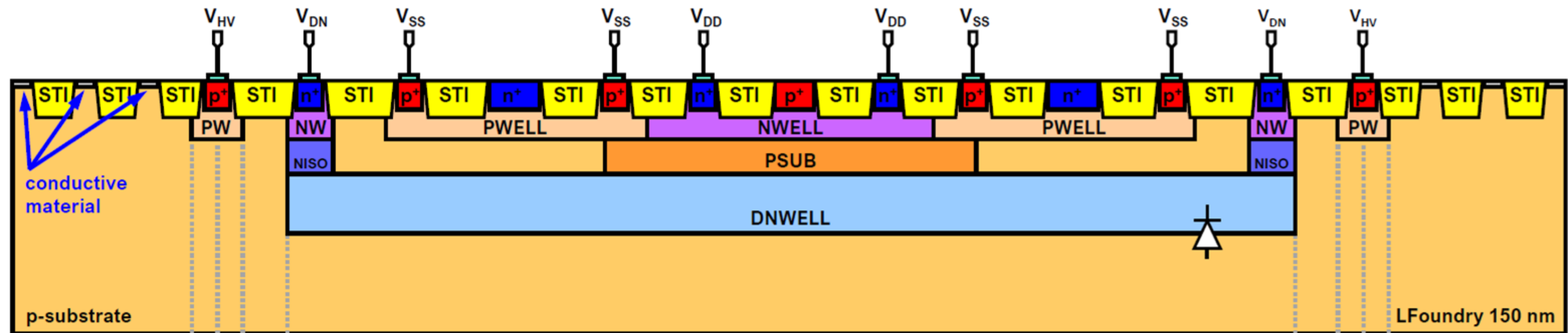
I-V curve



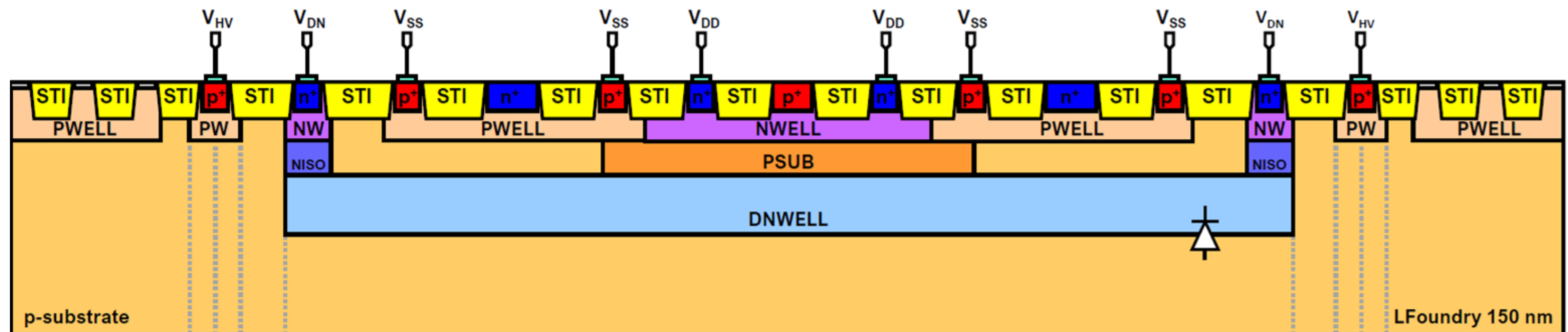


- I-V of central pixel of test structure (pixel size is 50 µm x 50 µm)
- Measurement done using a probe station with sensor in complete darkness
- **V_{BD}~ 55-60 V as expected from the design**
- **I_{LEAK} is too high (µA order well before V_{BD})**
- This issue has been extensively studied: *TCAD* + *support from the foundry*
- Methodologies to optimize leakage current in *new prototype RD50-MPW2*

Post-processing – Lessons learned



- LFoundry adds structures to the design files to prepare them for fabrication.
- These structures (in the pixels, peripheral readout electronics, I/O pads, etc.) **involve conductive material**.
- We believe these structures **contribute quite significantly to the high I_{LEAK}**.



- We have **minimised the presence of these structures** as much as possible to minimize I_{LEAK} in RD50-MPW2.
- Wherever not possible, LFoundry suggested **placing these structures inside a PWELL**.

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Post-processing – TCAD simulations

Electron current density in pad diodes

V_{HV} = -100 V V_{DN} = 0 V V_{DN} = 0 V V_{HV} = -100 V

"Ideal"

Shallow Trench Isolation PW STI NW NISO PWELL PSUB DNWELL NW NISO STI PW STI

e- current density [Acm^{-2}] ≈1E-3 ≈1E-20

p-substrate, ρ = 1.9 kΩ·cm @ -100 V TCAD simulation

RD50-MPW1

STI(s) PW STI NW NISO PWELL PSUB DNWELL NW NISO STI PW STI(s)

conductive material

e- current density [Acm^{-2}] ≈1E-3 ≈1E-20

p-substrate, ρ = 1.9 kΩ·cm @ -100V TCAD simulation

RD50-MPW2

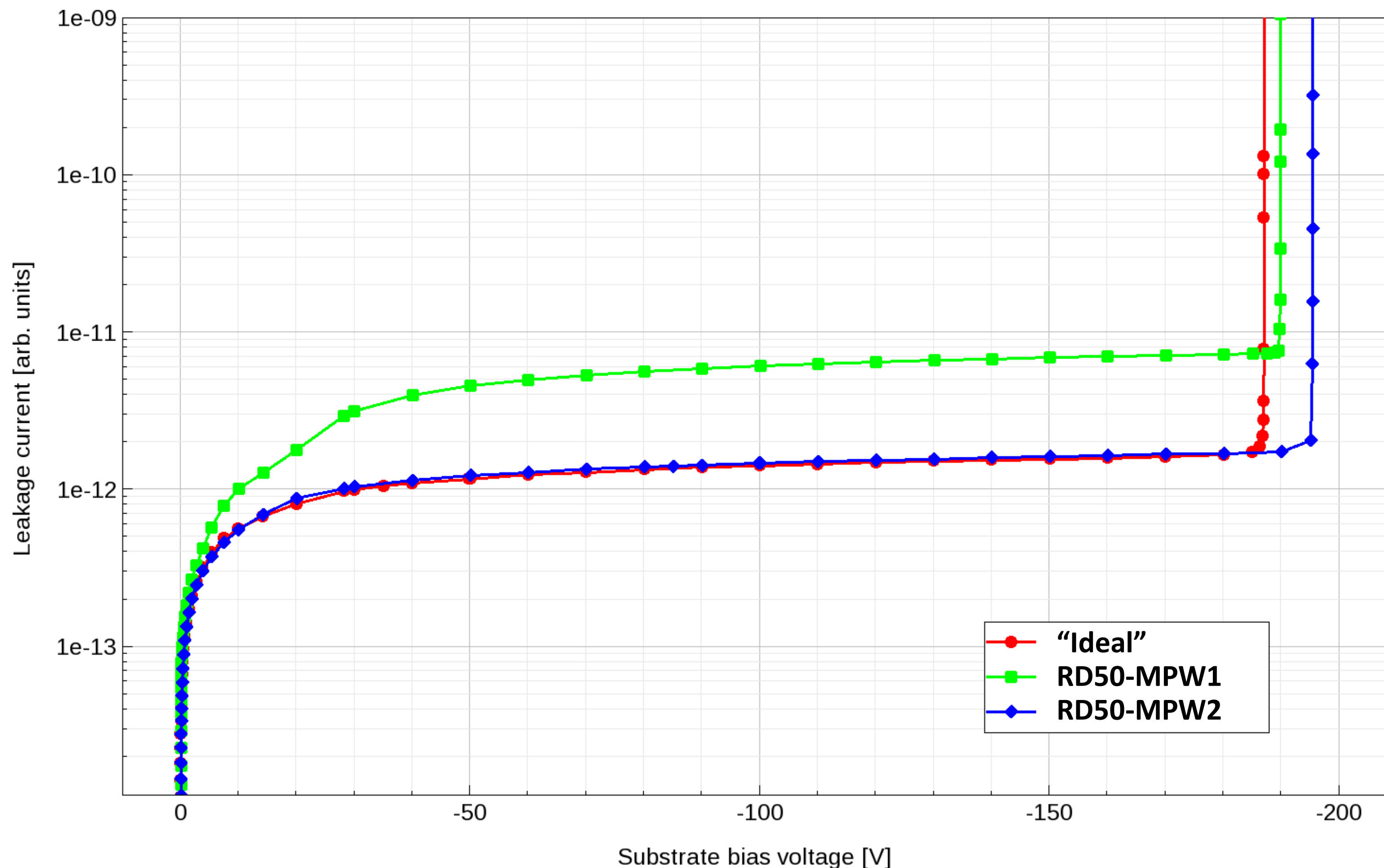
PWELL PW STI NW NISO PWELL PSUB DNWELL NW NISO STI PW PWELL

conductive material

e- current density [Acm^{-2}] ≈1E-3 ≈1E-20

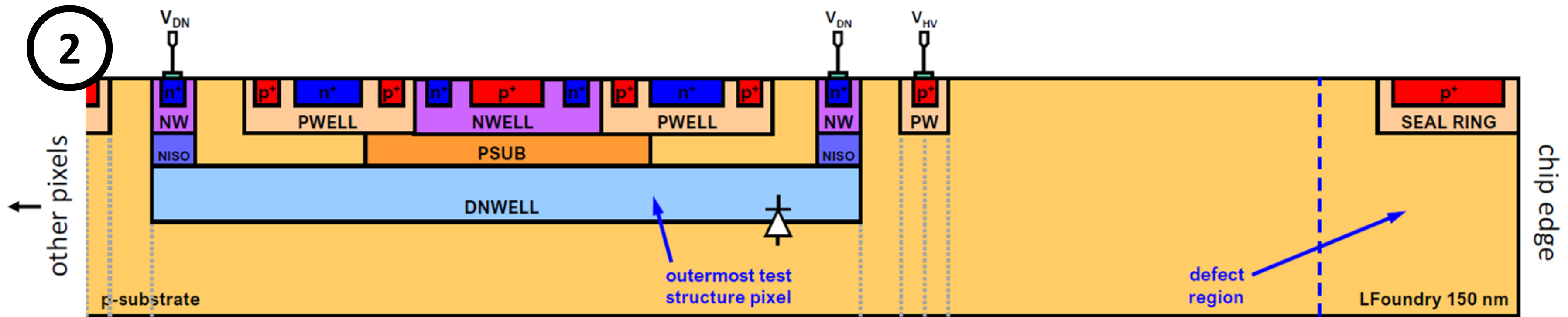
p-substrate, ρ = 1.9 kΩ·cm @ -100V TCAD simulation

Post-processing – TCAD simulations

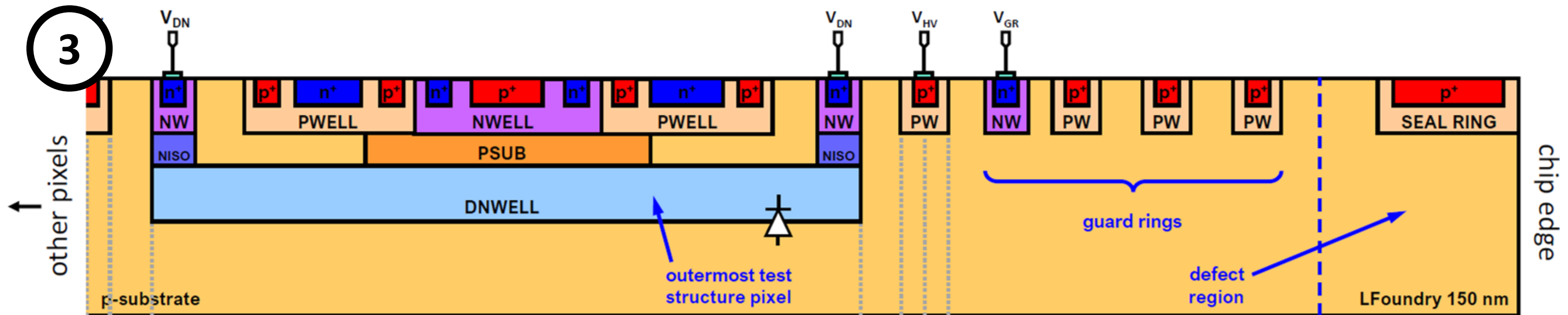


- Simulated leakage current for pad diodes.
- Increase in I_{LEAK} when conductive material is present on the surface (RD50-MPW1).
- I_{LEAK} is reduced when conductive material is placed in PWELL (RD50-MPW2).

Edge defects – Lessons learned

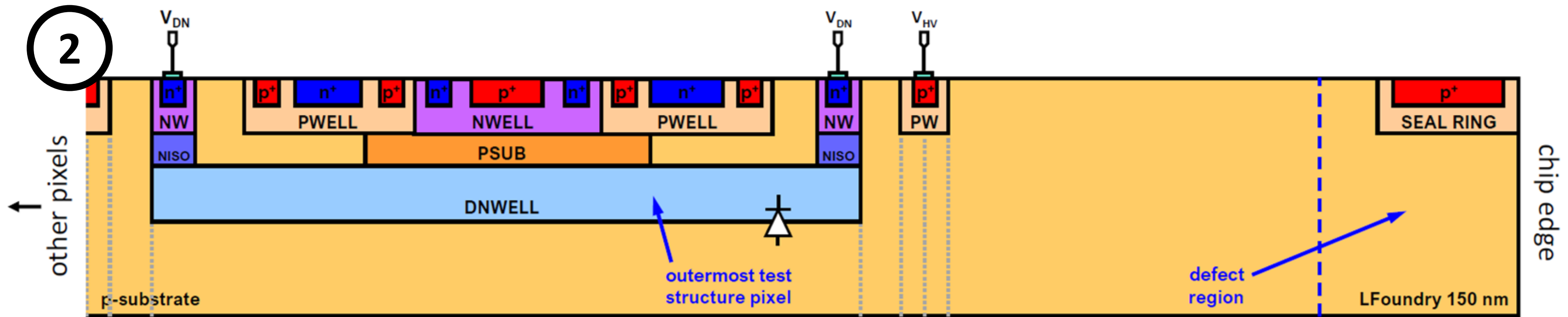


- Some pixels can be quite close to the edge of the chip.
- Defects in silicon lattice due to dicing can become significant.
- I_{LEAK} Increases when the pixel depletion region is near the defect region



- **N-type guard ring** added as safeguard to “collect” leakage current.
- **P-type guard rings** added to reduce “lateral” depletion.

Edge defects – Lessons learned



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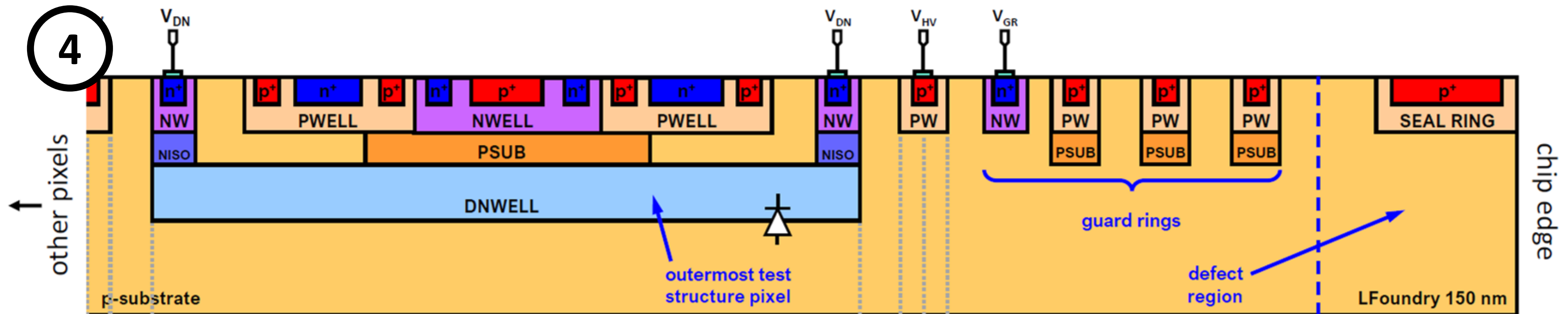
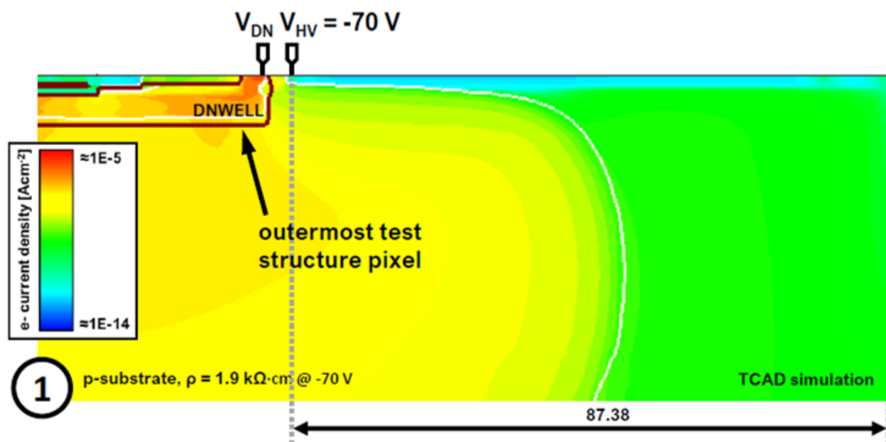
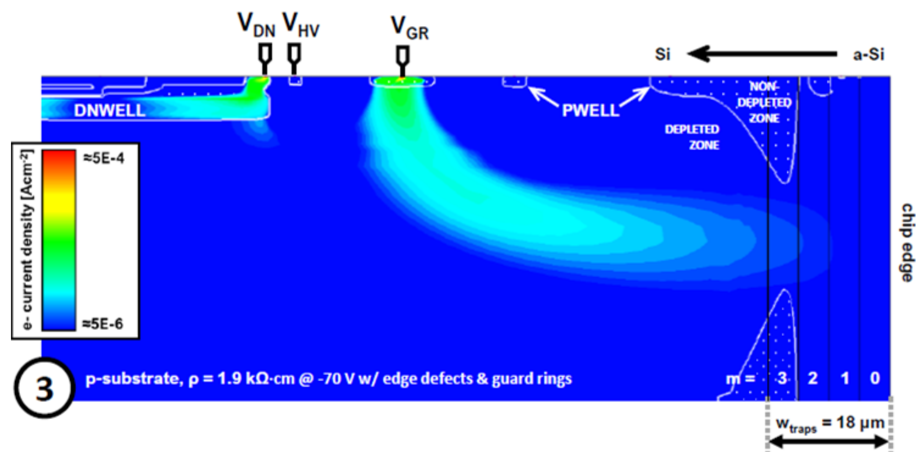
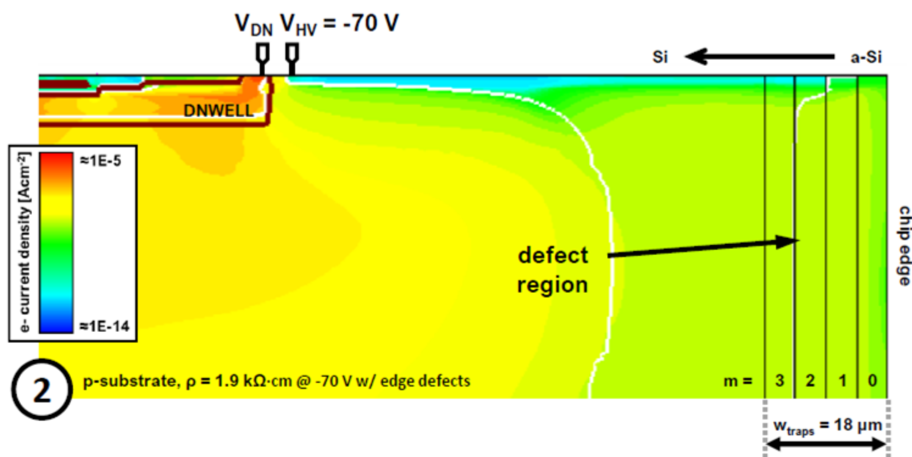


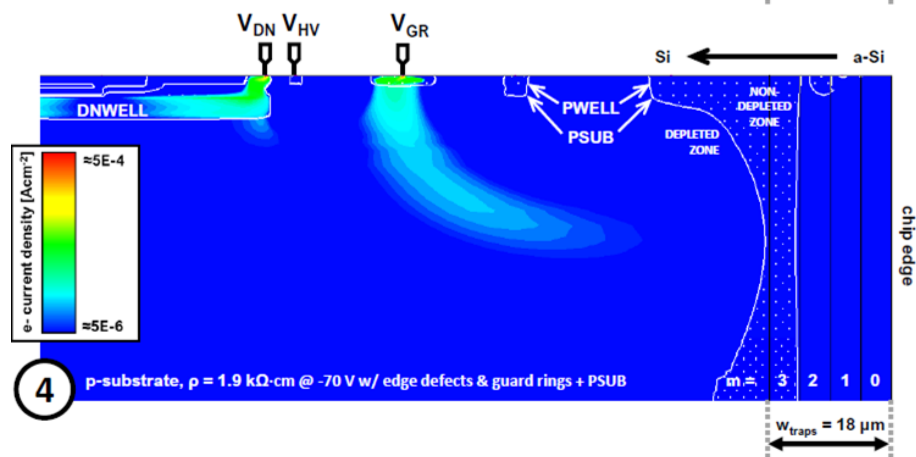
- **N-type guard ring** added as safeguard to “collect” leakage current.
- **P-type guard rings** added to reduce “lateral” depletion.
- **PSUB** added below P-type guard rings to further reduce ”lateral” depletion.

Edge defects – TCAD simulations









1) Without defects (ideal case).
2) With defects and no guard rings.
3) With defects, and NWELL and PWELL guard rings.
4) With defects, and NWELL and PWELL with PSUB guard rings.

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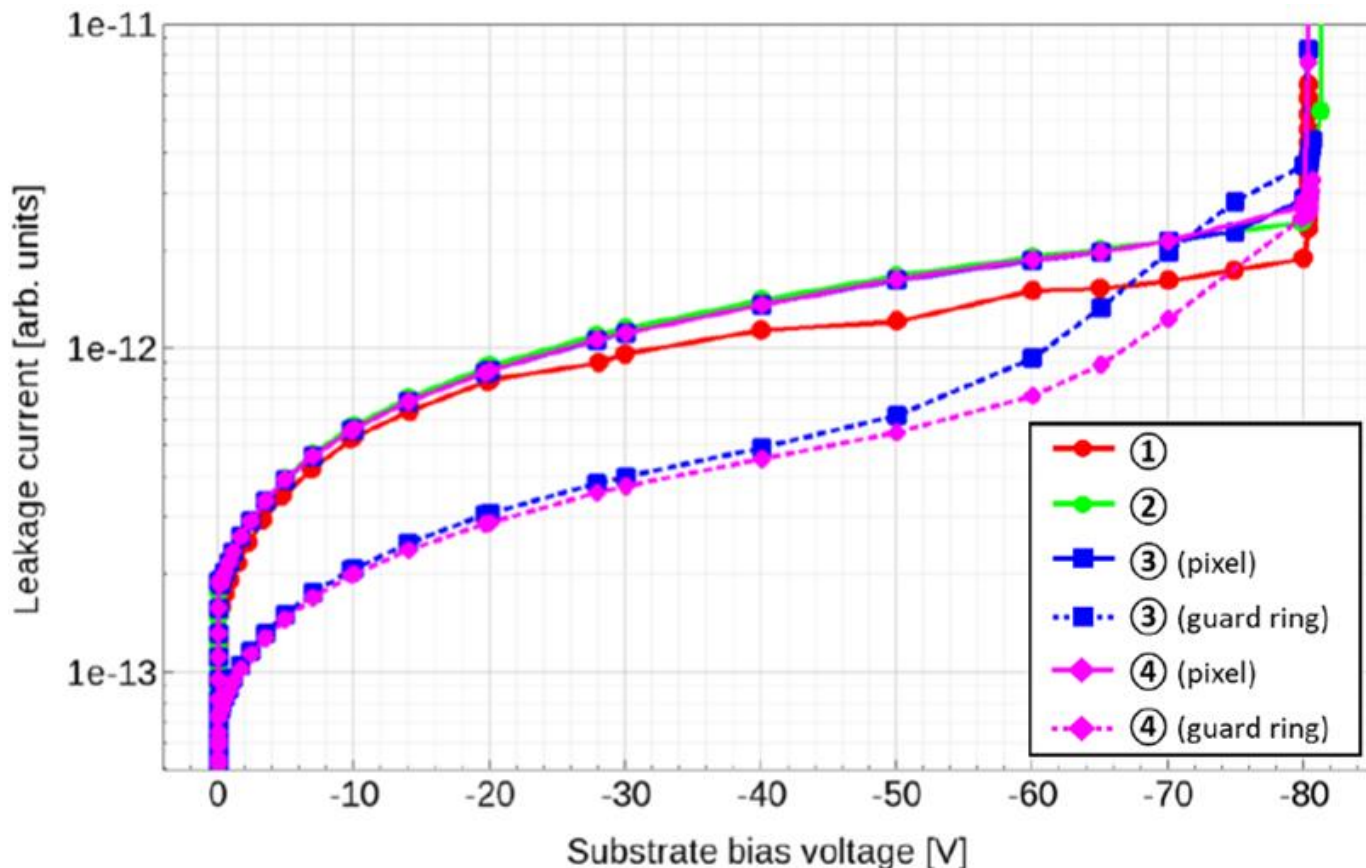
Edge defects – TCAD simulations



M. Franks, TREDI 2019

1) Without defects (ideal case).
2) With defects and no guard rings.
3) With defects, and NWELL and PWELL guard rings.
4) With defects, and NWELL and PWELL with PSUB guard rings.

Similar I_{LEAK}!! N-type guard ring acts as a diode increasing lateral depletion into defect region. PSUB reduces I_{LEAK} ☺

RD50-MPW2 – Submission

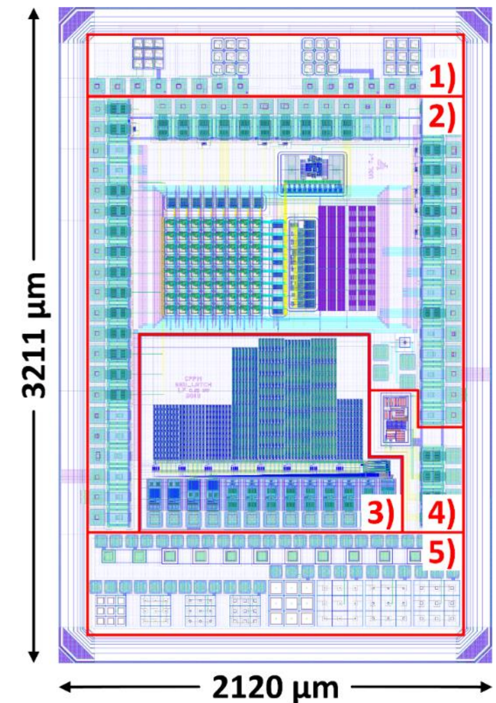
RD50-MPW2 - General design details

- MPW in the **150 nm HV-CMOS process from LFoundry**
- Submitted in January 2019 (dies expected in December)
- To implement methods to minimize the leakage current
- Fabricated using 4 different substrate resistivities
  - ➔ 10 Ω·cm (80 samples), 100 Ω·cm (80 samples), 1.9k Ω·cm (80 samples) and 3k Ω·cm (80 samples)

RD50-MPW2 – Chip contents

1) Tests structures with depleted CMOS pixels
2) Matrix of depleted CMOS pixels with analog readout
   - ➔ 8 x 8 pixels
   - ➔ 60 µm x 60 µm pixel area
   - ➔ Analog readout embedded in the sensing area
   - ➔ Aimed at improving the amplifier response rate
3) SEU tolerant memory array
4) Bandgap reference voltage
5) Test structures with SPADs and depleted CMOS pixels

- New methodologies to minimize leakage current



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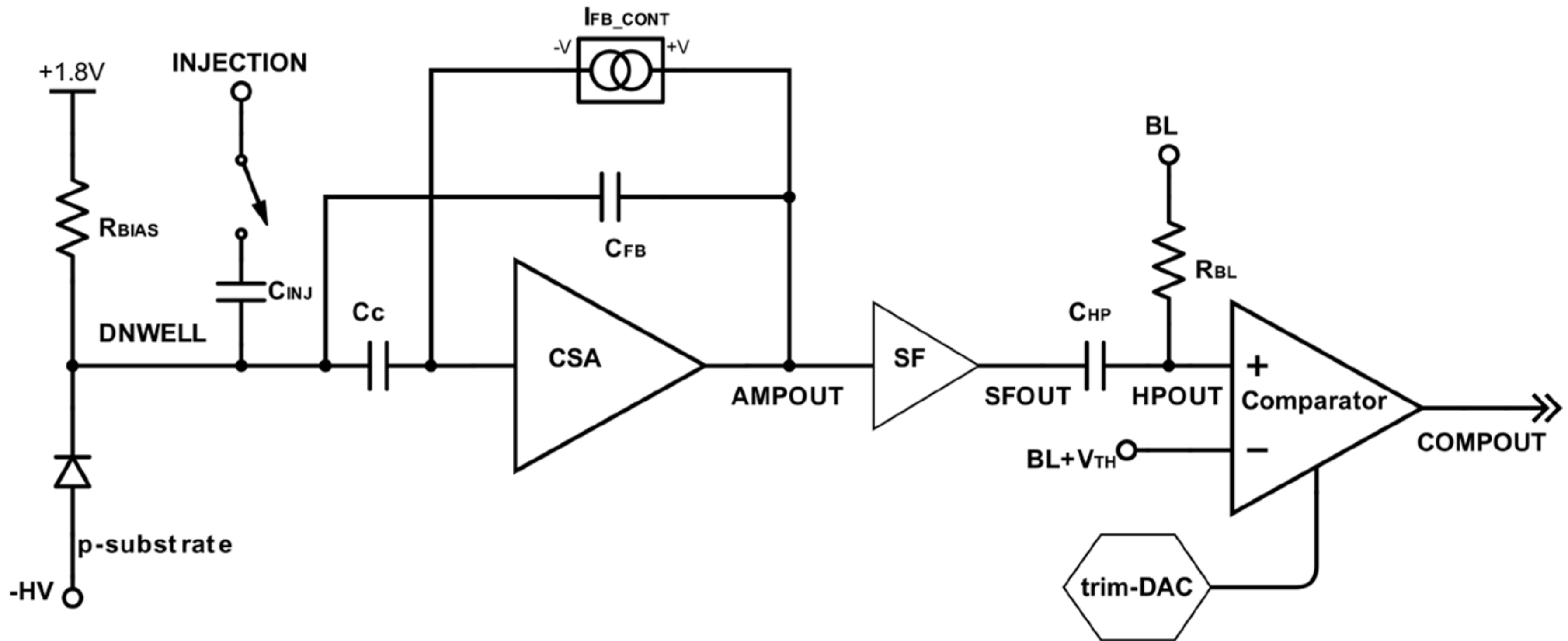
RD50-MPW2 – Matrix of depleted CMOS pixels

2 pixel flavours focused on improving the readout speed

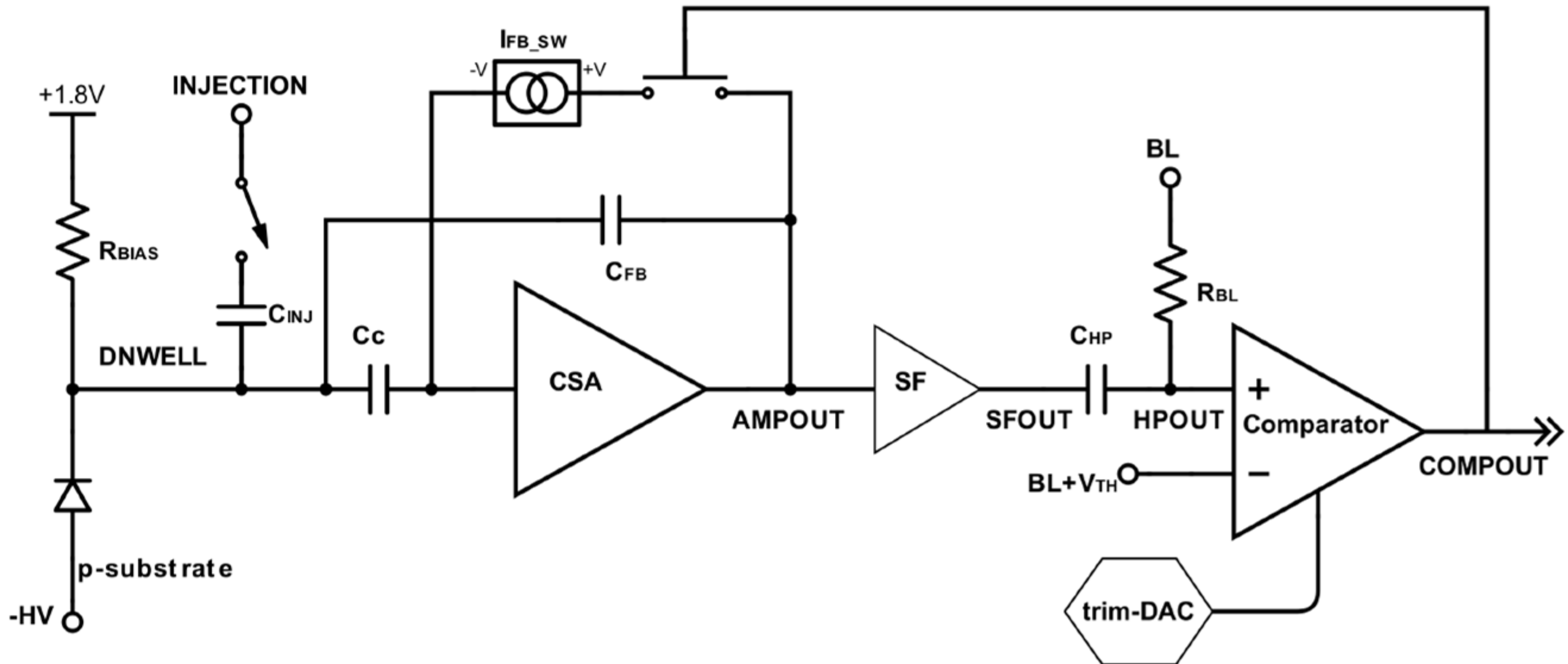
RD50-MPW2 – Pixel readout electronics



Pixel flavour with continuous reset – Analog readout

- Sensor biasing circuit, CSA, RC-CR filters and CMOS comparator
- CSA with programmable discharging current (I_{FB_CONT})
- CMOS comparator with global V_{Th} and local 4-bit DAC for fine tuning
- Very detailed design to minimize rising/falling edges of sensor amplifier
  - ➔ Falling edge controlled by C_{FB} and I_{FB_CONT}
  - ➔ I_{FB_CONT} is constant for linear discharge (ToT is possible)

RD50-MPW2 – Pixel readout electronics

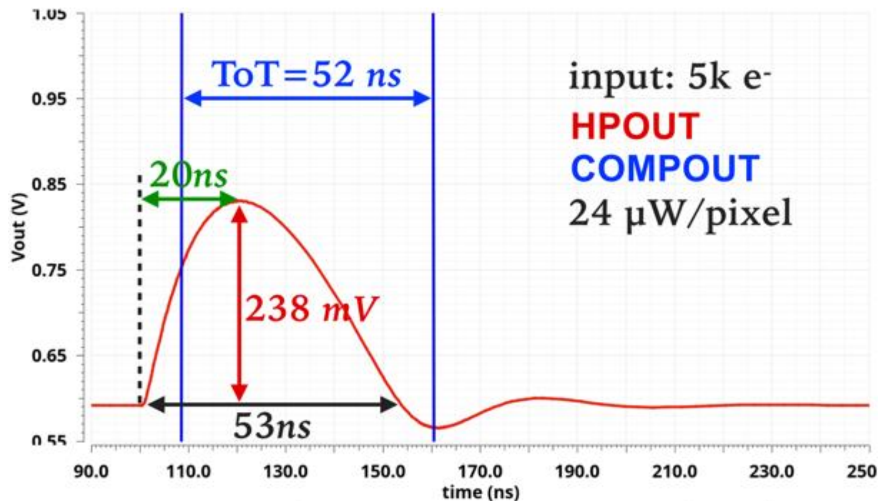


Pixel flavour with switched reset – Analog readout

- Sensor biasing circuit, CSA, RC-CR filters and CMOS comparator
- CSA with programmable discharging current (I_{FB_CONT}) + extra current upon particle hit controlled by switch / comparator output (I_{FB_SW})
- Very detailed design to minimize rising/falling edges of sensor amplifier
  - ➔ Falling edge controlled by C_{FB} and I_{FB_CONT} + I_{FB_SW}
  - ➔ Total discharging current is not constant for immediate discharge (ToA is possible)

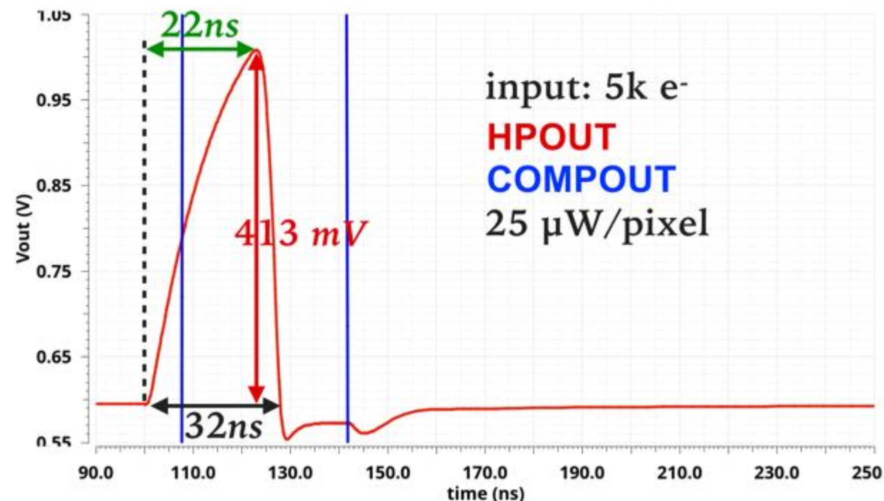
RD50-MPW2 – Pixel readout electronics

Continuous reset



- Linear discharge
- Fall time proportional to the number of e⁻ collected by the sensor
- Time-walk = 7 ns

Switched reset

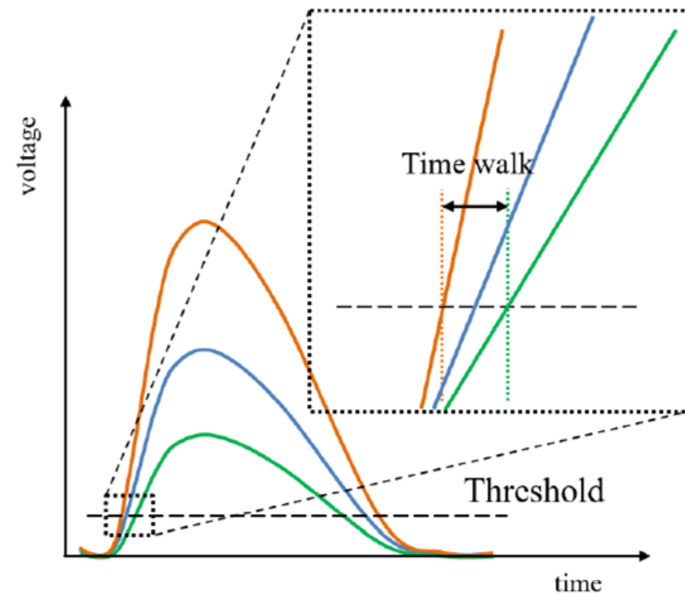


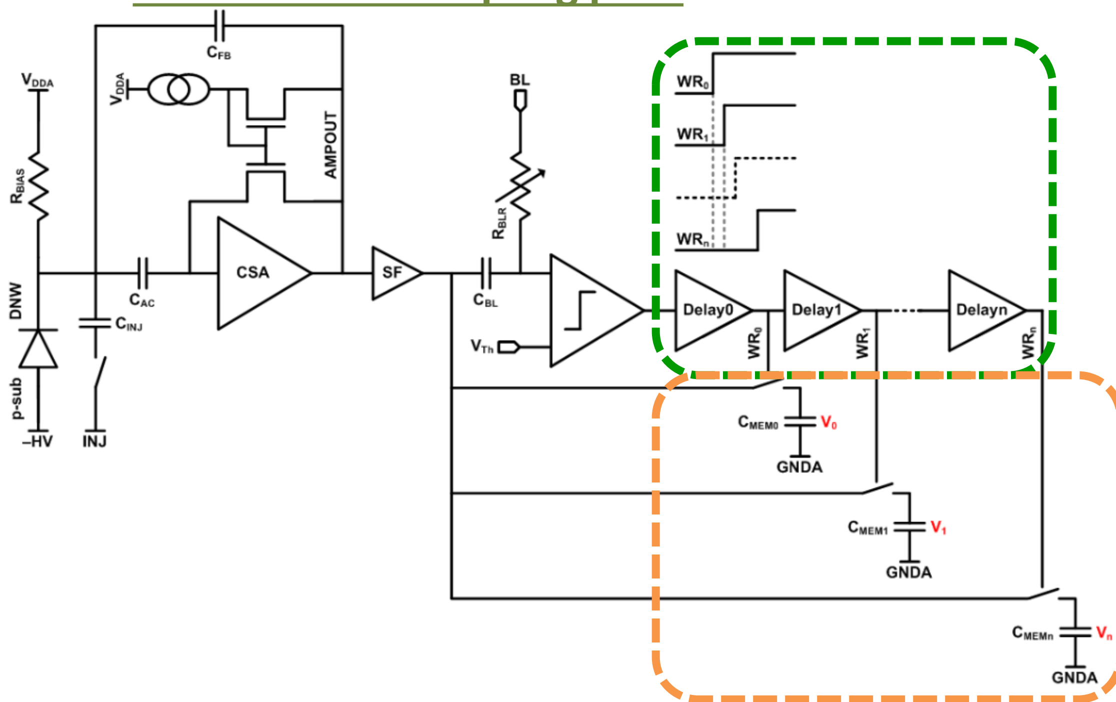
- Non-linear discharge
- Fall time NOT proportional to the number of e⁻ collected by the sensor
- Time-walk = 6 ns

C. Zhang, TWEPP 2019

New pixel flavour – Sampling pixel

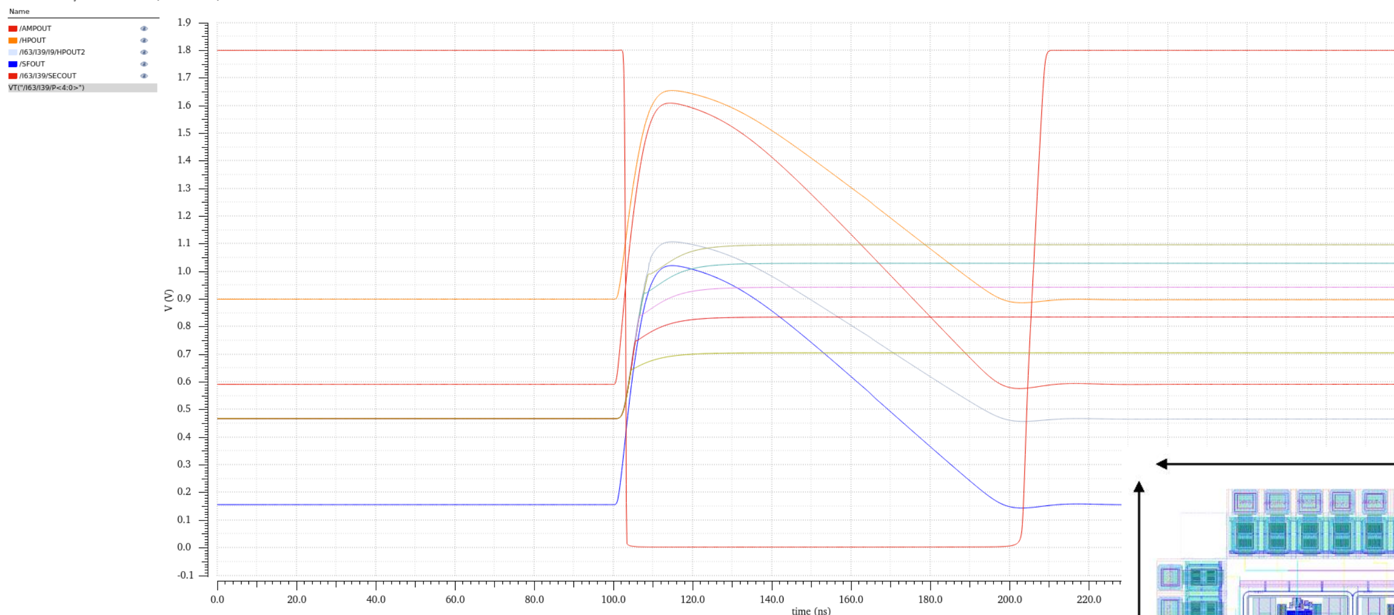
- Aim: Minimize the time-walk.
- Time-walk: Time difference in the detection of events that generate smaller or larger signals.
- A few methods for on-chip time-walk correction in depleted CMOS sensors developed already (compensated comparator, 2-thresholds, etc.).
- Best result so far found in the literature is ~ 6 ns.
- **Schematic of sampling pixel:**



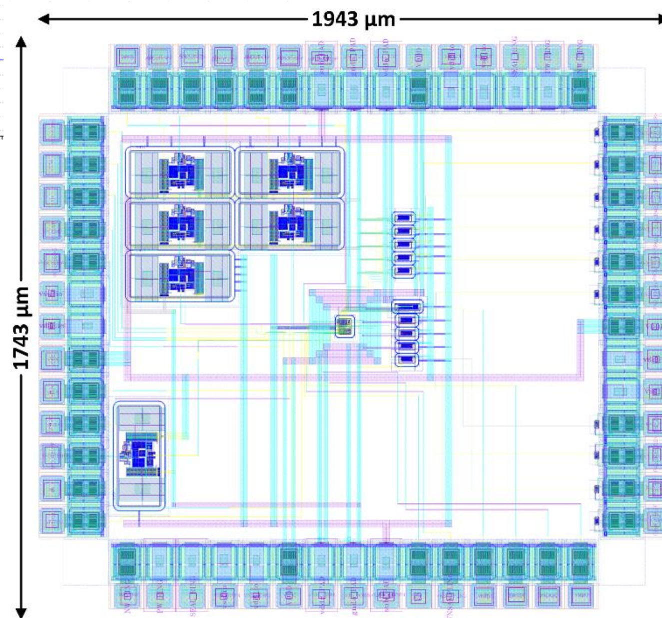


- Programmable chain delay to sample a few points of SF signal (i.e. 5)
- Analog memories to store the voltage values
- Off-chip ADCs
- Off-chip processing to determine t_0 (time of event)

New pixel flavour – Sampling pixel



O. Alonso, LCWS 2018
S. Moreno, TWEPP 2019



- Best achieved time resolution with the sampling pixel is ~ 2 ns.
- Proof-of-concept pixel submitted in June 2019 (dies expected in spring 2020).

Conclusion

- **CERN-RD50 programme** to develop and study **depleted CMOS sensors**
- This programme includes
  - ➔ASIC design
  - ➔TCAD simulations
  - ➔DAQ development
  - ➔Performance evaluation
- We have developed 2 MPW prototypes (RD50-MPW1, RD50-MPW2) already with
  - ➔Small pixel sizes
  - ➔Optimized leakage current and radiation tolerance
  - ➔Improved response rate and time-walk
- We have plans to continue developing depleted CMOS sensors within our collaboration

Back up slides

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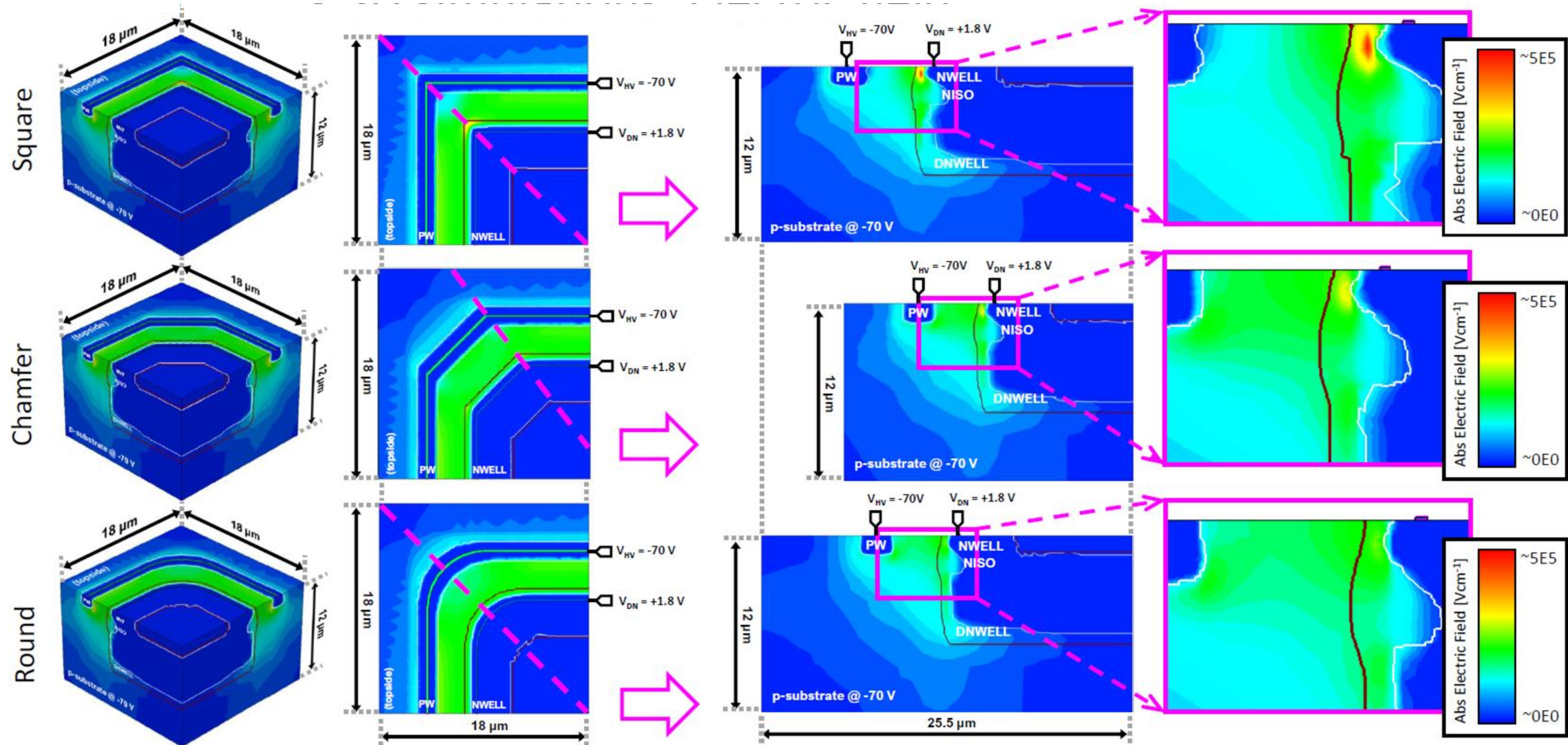
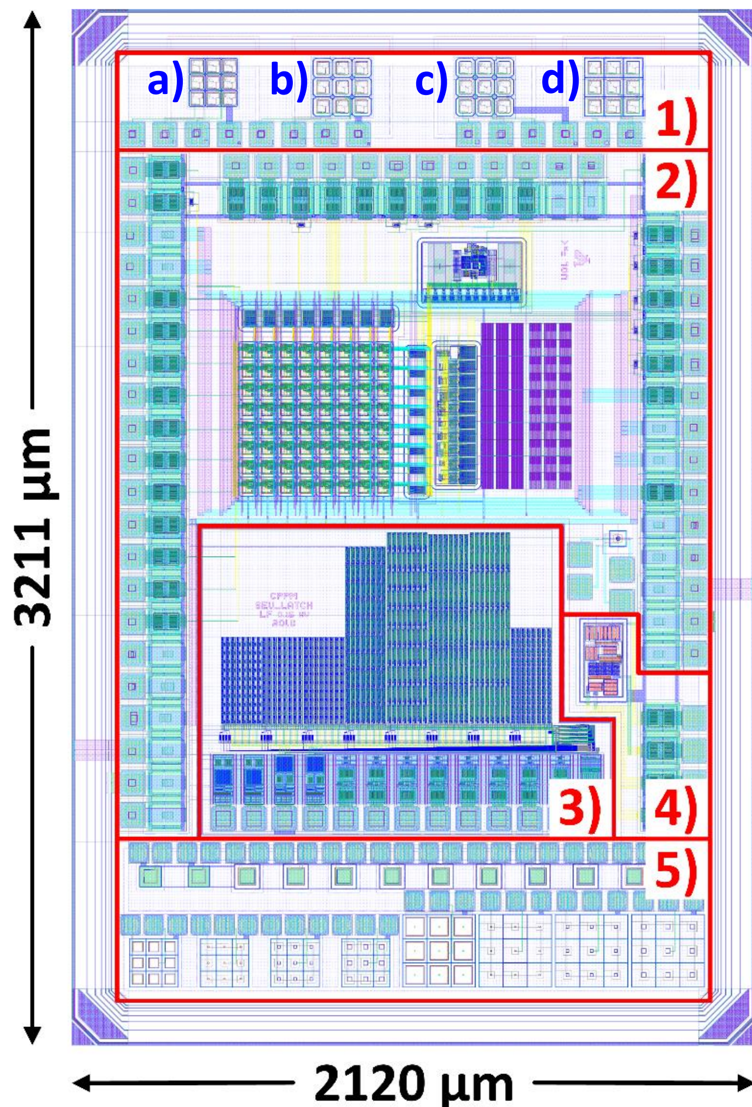
Pixel geometry – TCAD simulations

3D simulations – Electric field as a function of corner geometry in pixel



RD50-MPW2 – Test structures 1)



Matrices of 3 x 3 depleted CMOS pixels

- For I-V and e-TCT measurements
- Very similar to other test structures used in the past
- 8 external pixels are shorted together
- I/O pads for central and external pixels
- No electronics in the pixels
- No electronics in the I/O pads

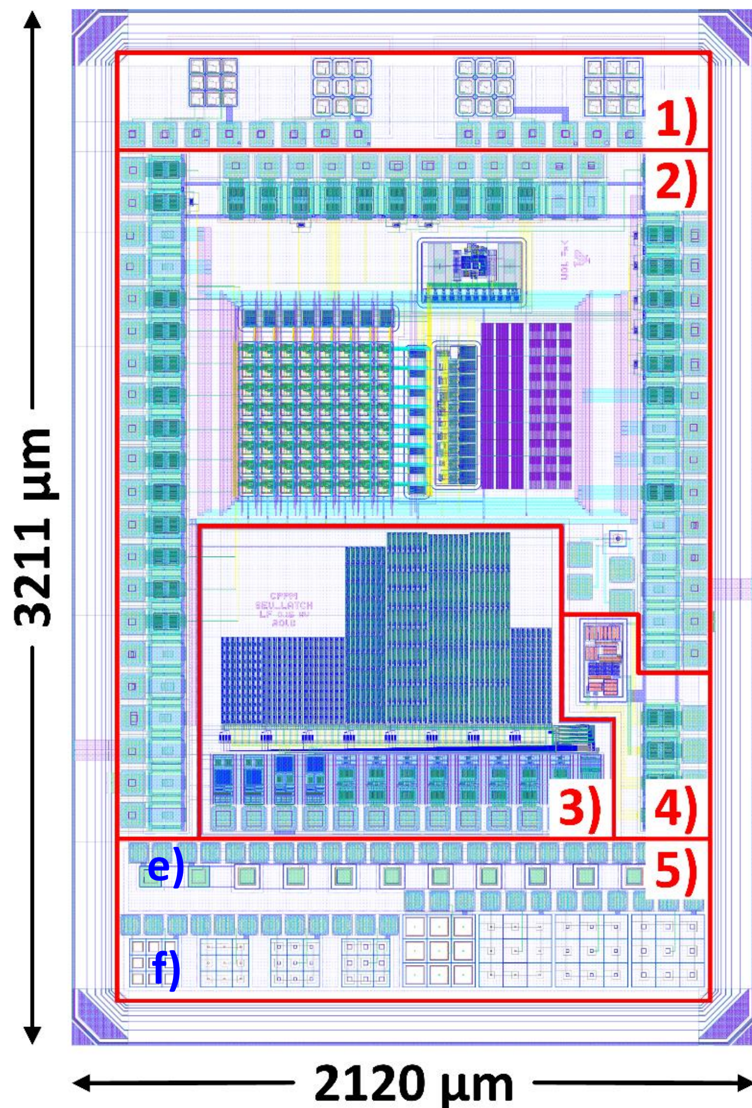
a) Pixel size → 50 µm x 50 µm
P-substrate/deep n-well spacing → 3 µm
Corners → rounded

b) Pixel size → 60 µm x 60 µm
P-substrate/deep n-well spacing → 8 µm
Corners → rounded

c) Pixel size → 60 µm x 60 µm
P-substrate/deep n-well spacing → 8 µm
Corners → chamfered

d) Pixel size → 60 µm x 60 µm
P-substrate/deep n-well spacing → 8 µm
Corners → squared

RD50-MPW2 – Test structures 5)

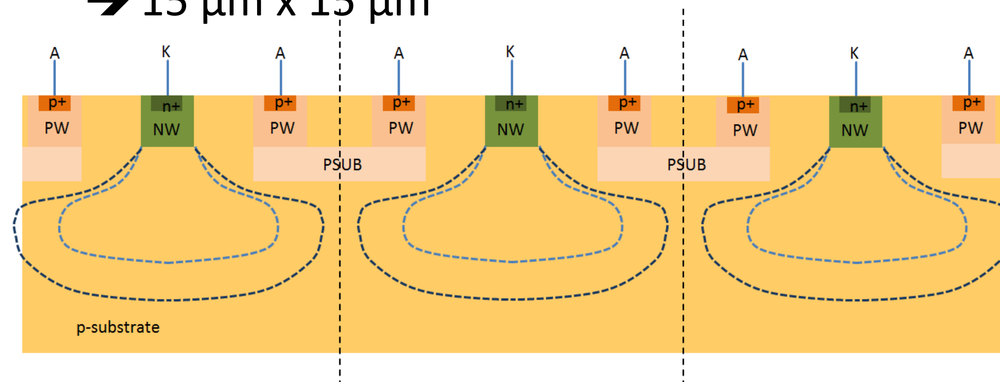


e) SPADs

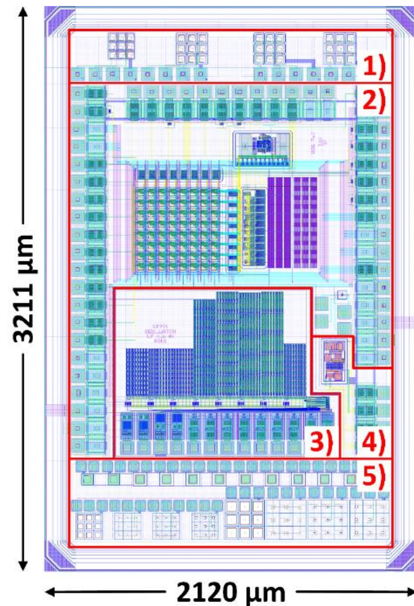
- 12 single diodes
- Different cross-sections
- *Problematic* layers have been prevented

f) Matrices of 3 x 3 depleted CMOS pixels

- To compare large and small FF pixels
- Large and small FF pixels with different size:
  - ➔ 50 µm x 50 µm
  - ➔ 75 µm x 75 µm
- To study the depletion region as a function of the collecting electrode size:
  - ➔ 5 µm x 5 µm
  - ➔ 10 µm x 10 µm
  - ➔ 15 µm x 15 µm



RD50-MPW2 – SEU tolerant memory array



To study the SEU tolerance of several memory cells by comparing them to the standard cell. The array has 8 different flavours:

3.1) Standard cell from the LFoundry library (latch cell)
- It uses 8 transistors

3.2) DICE cell (Dual Interlocked Storage Cell, full custom)
- Special cell based on 2 cross-coupled inverters
- It uses 12 transistors
- Immunity against SEUs (non-simultaneous)

3.3) Enhanced DICE cell (full custom)
- DICE cell with larger spacing between sensitive nodes
- Immunity against simultaneous SEUs

3.4) Standard cell with TRL (Triple Redundancy Logic)
- With feedback correction driven by error detection

3.5) DICE cell (full custom) with TRL

3.6) Standard cell with TRL and split latch
- TRL split between 2 bits to separate sensitive nodes further

3.7) DICE cell (full custom) with TRL and split latch

3.8) SRAM cell
- It uses 6 transistors

The memory array will be tested in sites like Leuven, Jyväskylä and Groningen.