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Recent depleted CMOS developments within the CERN-RD50 framework

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Depleted Monolithic Active Pixel Sensors (DMAPS) in commercial High Voltage-CMOS (HV-CMOS) processes are groundbreaking tracking detectors for particle physics experiments, as they offer a competitive and cost-effective solution over a large range of applications. In spite of the major improvements demonstrated by DMAPS during the last few years, these sensors require further research especially in terms of improving the time resolution and radiation tolerance to realise the full potential of the extremely challenging particle physics experiments planned for the near future. In this context, the CERN-RD50 collaboration has started to study depleted CMOS sensors as one of its main priorities.

This contribution presents the R&D programme within the CERN-RD50 collaboration to study depleted CMOS sensors. We will describe the 2 test prototypes developed so far, which are in the 150 nm HV-CMOS technology process from LFoundry and manufactured on high resistivity substrates. Following from work in the wider community, the first prototype (RD50-MPW1) integrates 2 fully monolithic matrices of depleted CMOS pixels and test structures for edge Transient Current Technique (eTCT) characterisation. One of the matrices has 50 µm x 50 µm pixels with FE-I3 style readout electronics embedded inside the sensing area of the pixels, while the other matrix has 75 µm x 75 µm pixels with a 16-bit counter for photon counting applications. The second prototype (RD50-MPW2) implements a small matrix of depleted CMOS pixels with analog readout electronics to minimise the sensor readout time, several other readout circuits and test structures. All the designs of RD50-MPW2 incorporate new methodologies to reduce the large leakage currents, and therefore increase the radiation tolerance, measured with RD50-MPW1. These methodologies comprise blocking the generation of certain filling layers added by the foundry during the post-processing stage and adding a series of guard rings around the chip. We will also describe the design work towards a new pixel flavour, named sampling pixel and recently submitted for fabrication with LFoundry as a proof-of-concept, which in simulations improves the time resolution of depleted CMOS sensors to approximately 2 ns. This design and others will be included in the large area submission RD50-ENGRUN1 planned by the collaboration.

The details that will be covered in this presentation include device simulations with TCAD to optimise the leakage current of DMAPS, ASIC design aspects of the pixel flavours that have been fabricated so far, the development of a common and flexible data acquisition system based on the Caribou generic board and used in the experimental evaluation of the prototypes, and the main performance results achieved already.

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