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## Real-time reconstruction of pixel vertex detectors with FPGAs

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The LHCb experiment is undergoing a major upgrade in view of Run-3, in which the complete detector will be read out, and events fully reconstructed, at the full LHC crossing rate (averaging 30 MHz). One of the key steps of event reconstruction is finding tracks in the new, high precision pixel vertex detector (VELOPIX). This step is the necessary starting point for most of the rest of the reconstruction, and requires a significant fraction (close to a half) of the total CPU time that will be available in the upgraded Event Filter Farm. We present the current status of a LHCb R&D project devoted to accelerating this computation by the use of an array of commercial state-of-the-art FPGA cards embedded in the DAQ system, performing pattern recognition in the vertex detector 'on the fly', while the detector is being readout at 30 MHz.

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