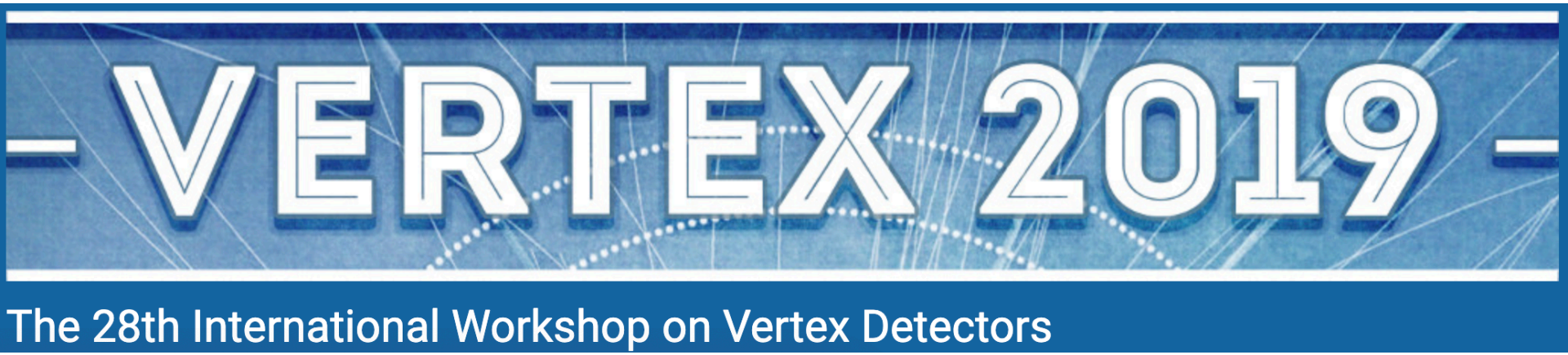
VERTEX AND TRACKING DETECTORS FOR THE CIRCULAR ELECTRON POSITRON COLLIDER (CEPC)

Hongbo Zhu (IHEP, Beijing)

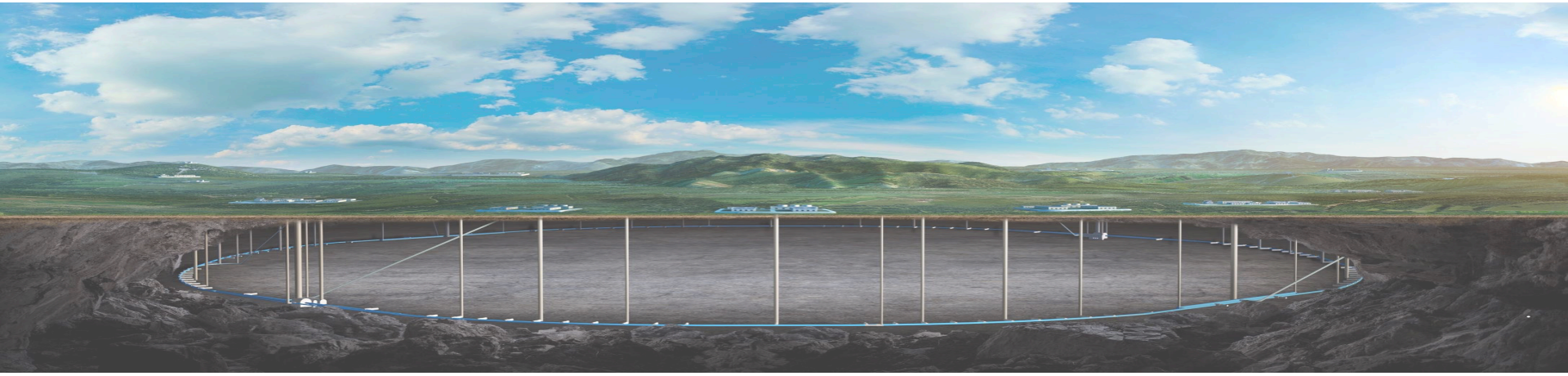
On behalf of the CEPC Study Group



The 28th International Workshop on Vertex Detectors, 13 - 18 October 2019, Lopud Island, Croatia

OUTLINE

- Introduction to CEPC
- CEPC vertex & tracker layout
- Vertex detector design & R&D
- Silicon tracker design & R&D
- Summary & outlook



Circular Electron Positron Collider (CEPC)

- **Phase I:** Circular Electron-Positron Collider (CEPC)
  - **Higgs Factory**, CM energy ~240 GeV (*ZH* threshold), peak luminosity ~3×10^{34} $cm^{-2}s^{-1}$, 2 interaction points → Higgs precision measurements (mass, width, branching ratios, couplings ...)
  - Operation at 91/160 GeV → EW precision measurements

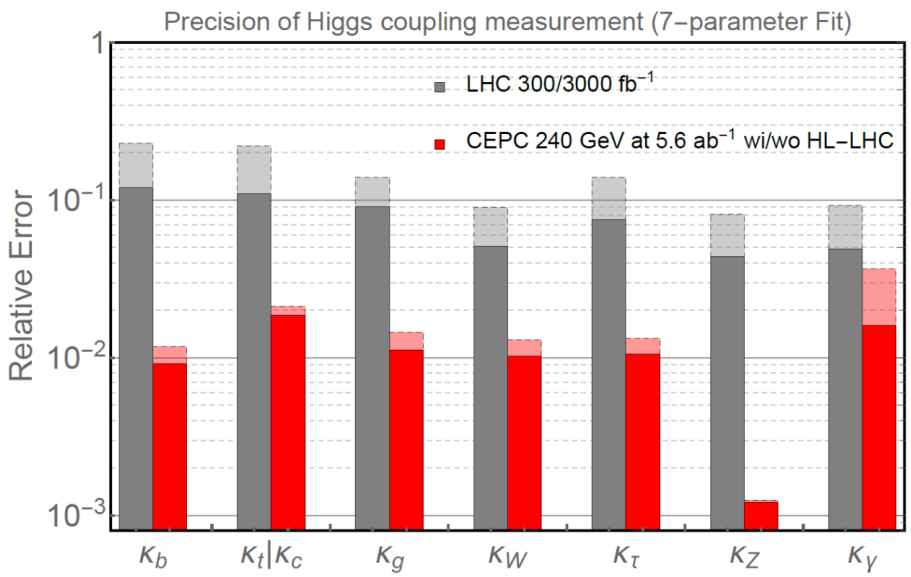
- **Phase II:** Super Proton-Proton Collider (SppC)
  - Discovery Machine, center-of-mass energy 50-100 TeV, luminosity ~1×10^{35} $cm^{-2}s^{-1}$, 2 interaction points → Energy Frontier for New Physics
  - Other possible collision modes: *ep, eA, pA or AA*

Higgs Precision Measurements

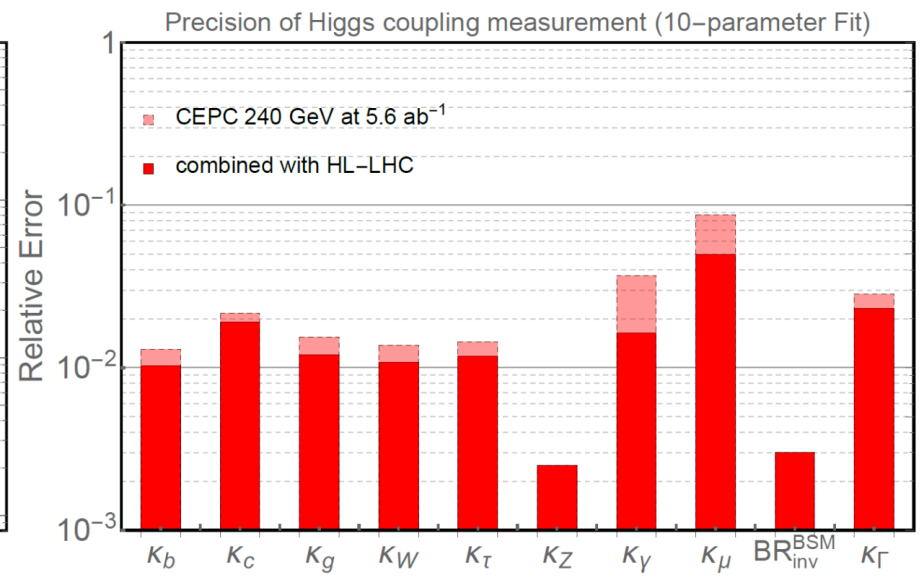
- Higgs coupling deviations from the Standard Model (SM) predictions parameterized as:

$$\kappa_f = \frac{g(hff)}{g(hff;\mathrm{SM})}, \kappa_V = \frac{g(hVV)}{g(hVV;\mathrm{SM})}$$

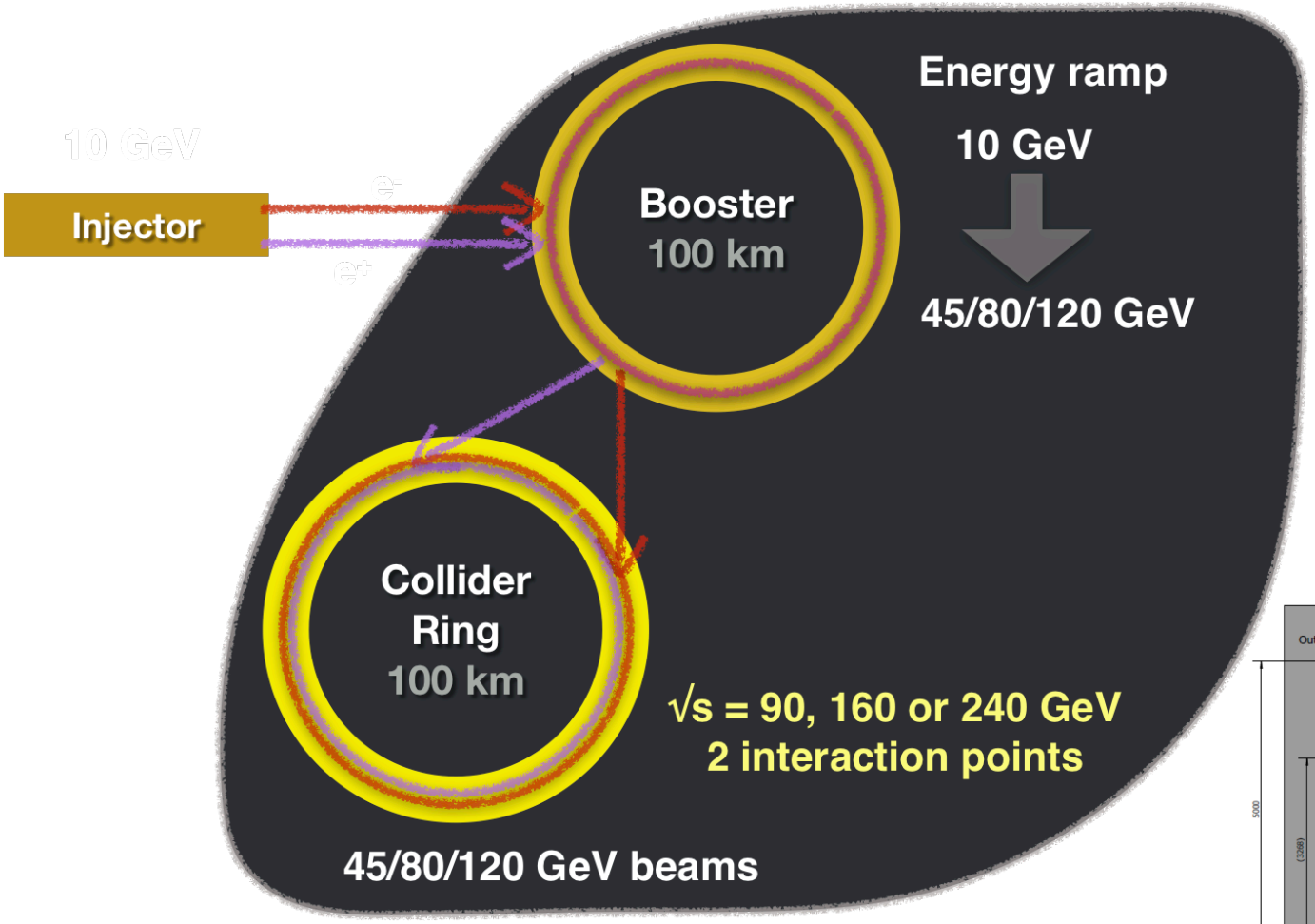
Model-dependent fit:



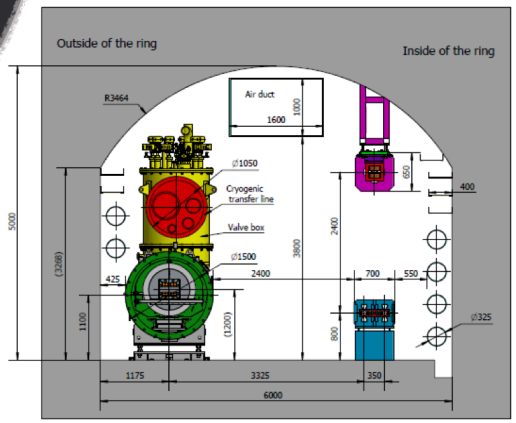
Model-independent fit:



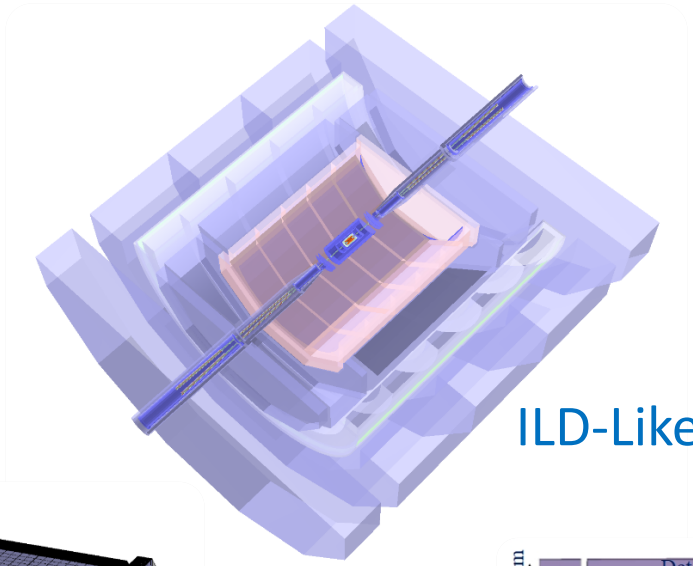
Machine Conceptual Design



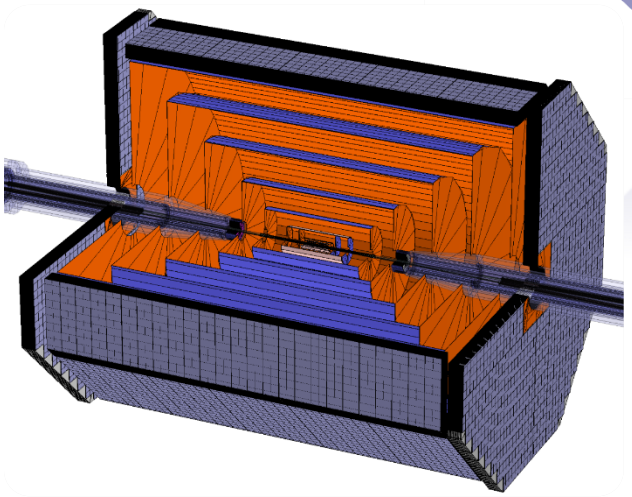
TUNNEL CROSS SECTION OF THE ARC AREA



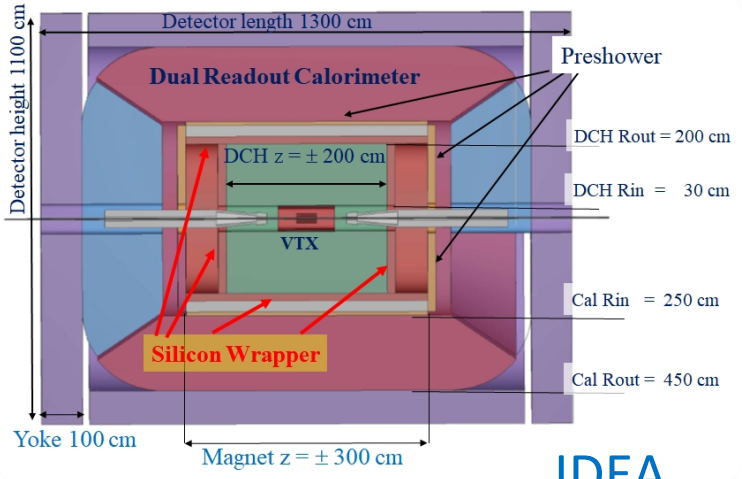
Detector Conceptual Designs



ILD-Like, Baseline design

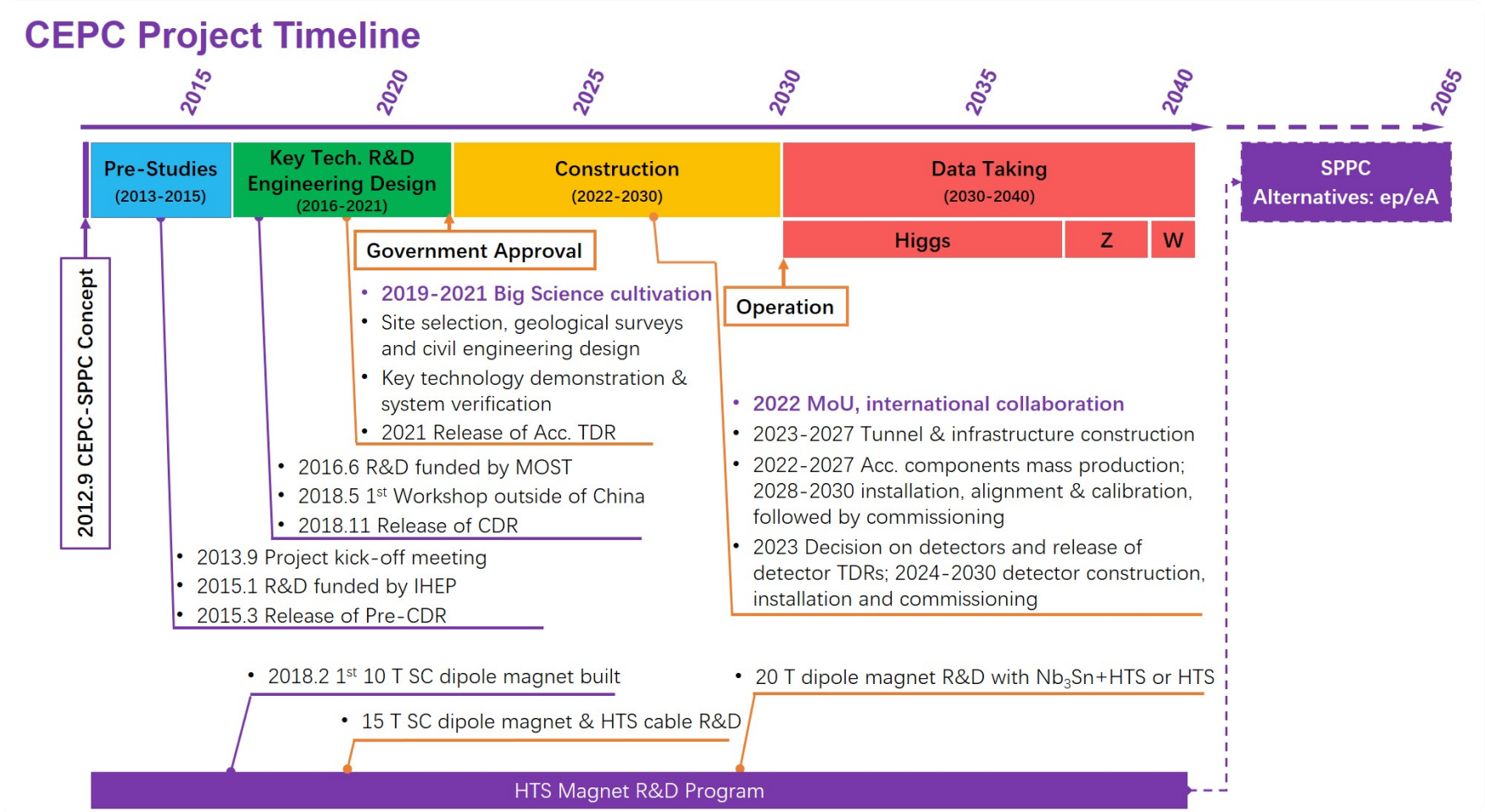


Full silicon

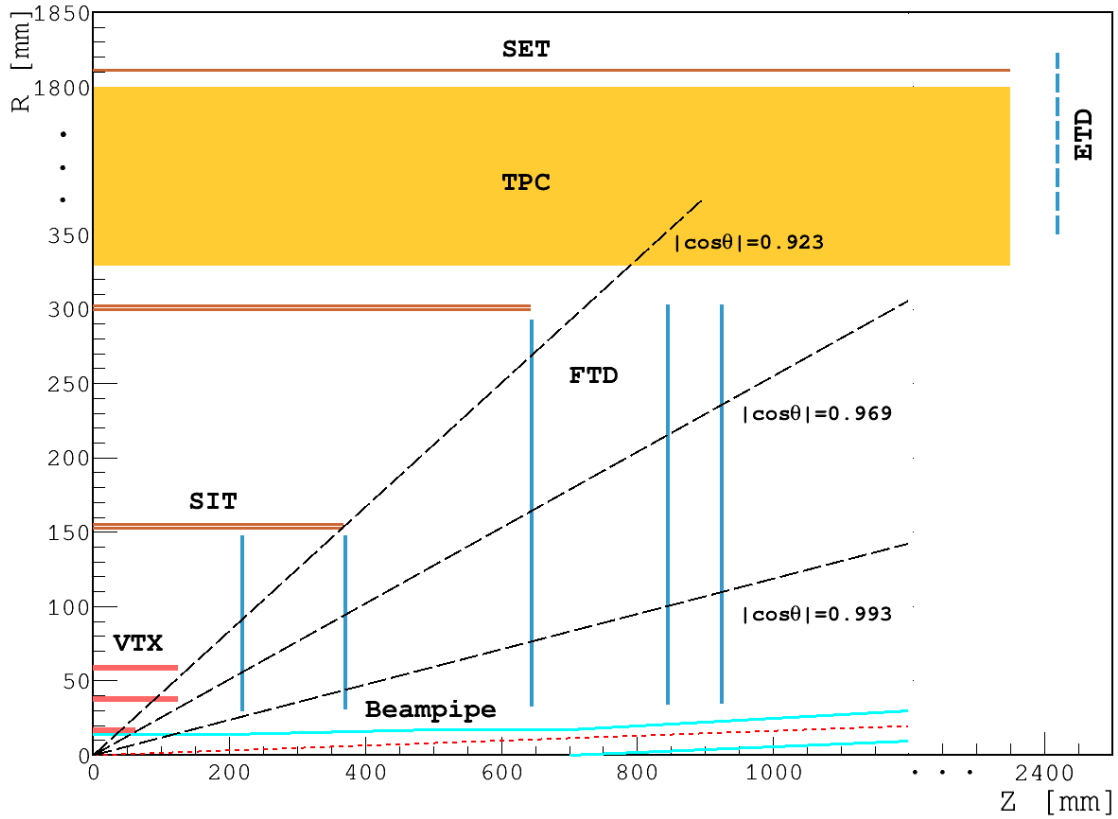


IDEA

PROJECT TIMELINE



VERTEX & TRACKER LAYOUT



- **Baseline**: Time Projection Chamber (TPC) +"Silicon Envelope" *from ILD*
- **Optional**: Full silicon tracker, more suitable to handle high event rates

Vertex Detector Requirements

- High precision vertex detector essential for heavy-flavor and τ-lepton identification; designed to achieve

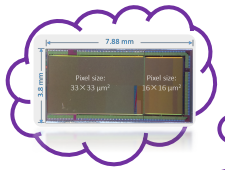
$$\sigma_{r\varphi} = 5\ \mu m \oplus \frac{10\ \mu m}{p(\mathrm{GeV}) \cdot \sin^{3/2}\theta}$$

- With the baseline design, this implies:
  - Single point resolution < 3 μm → small pixel pitch, e.g. 16 μm
  - Material budget 0.15%X_0 per layer→ thin & low power 50 mW/cm^2
  - Detector occupancy below 0.5% → small pixel & fast readout
  - Radiation tolerance **(per year):** 1 MRad &2×10^{12} 1 MeV n_{eq}/cm^2

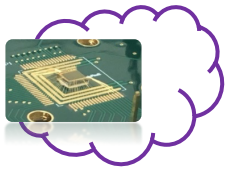
PIXEL SENSOR R&D

CEPC Pixel Sensor R&D

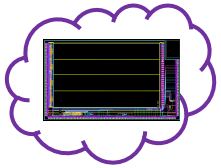
- **JadePix-1**：Diode optimization; design & characterization



- **JadePix-2**：Compact pixel design, in-pixel amplification, digital readout

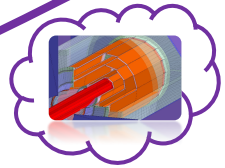


- **JadePix-3**：bug-fix and improved design (submitted)



- **Taichu-1**： Column Drained readout (FE-I3), two-stage FIFO (submitted)

Ultimate Pixel Sensor

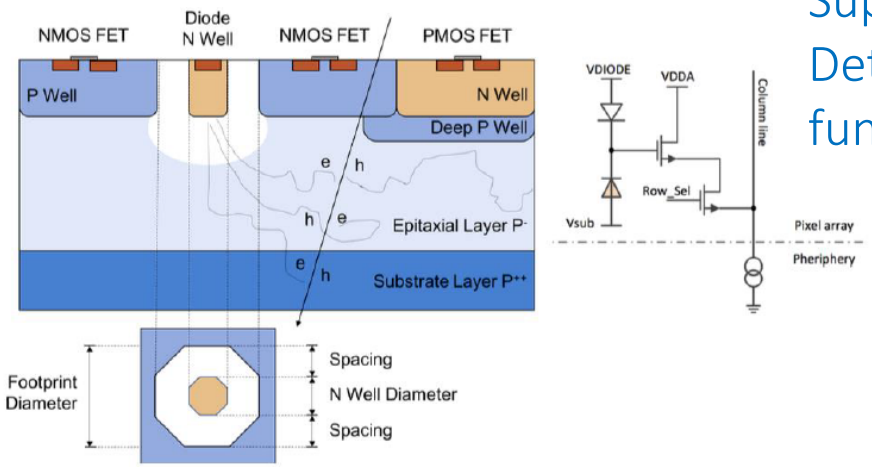


- **Specifications:** spatial resolution~3 μm, power consumption<50 mW/cm^2, radiation tolerance 10 MRad (TID)；

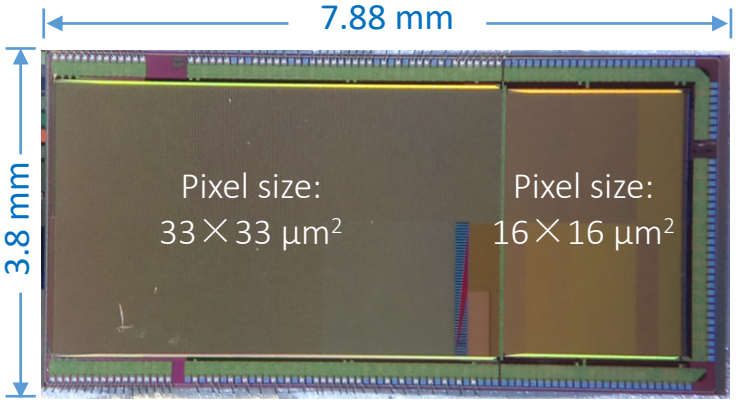
2015 2016 2017 2018 2019 2020 2021 2022 2023 2024

JADEPIX-1 PIXEL DESIGN

- 1st prototype sensor developed with TJ 0.18 µm CIS process
- Primary goal: diode geometry optimization



Supported by the State Key Lab of Particle Detection and Electronics & IHEP Innovation fund, **with lots of helps from IPHC**



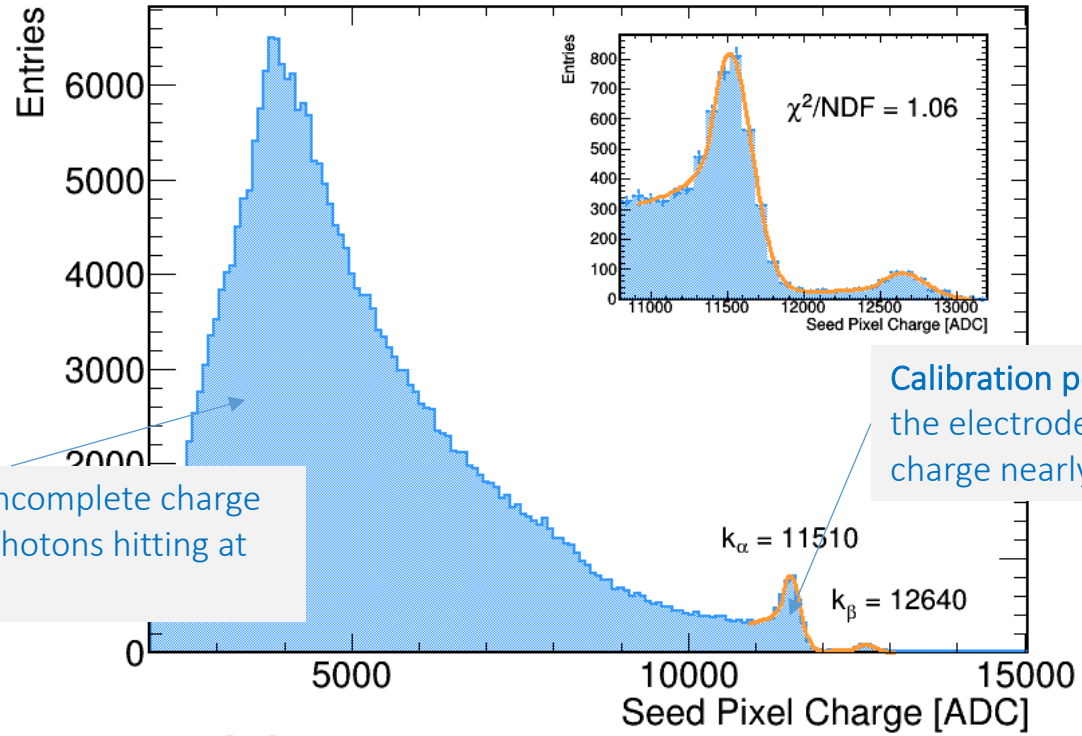
Impacts of electrode size and footprint on charge collection performance

- Submission in November 2015, test system developed and verified in 2016; detailed performance characterization in 2017& 2018

Response to ^{55}Fe

- Response to low energy X-ray photons for calibration

Seed Pixel



Collection peak, incomplete charge collection when photons hitting at other positions

Calibration peak, X-ray photons hitting the electrode area and generated charge nearly 100% collected

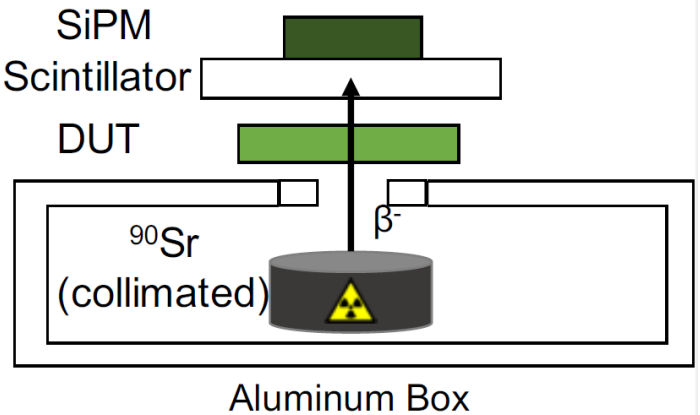
$$V_{\text{calib}} = k_\alpha \ [\text{ADC}] \times \frac{2.5\ [V]}{2^N - 1} \times \frac{1}{g_a}$$

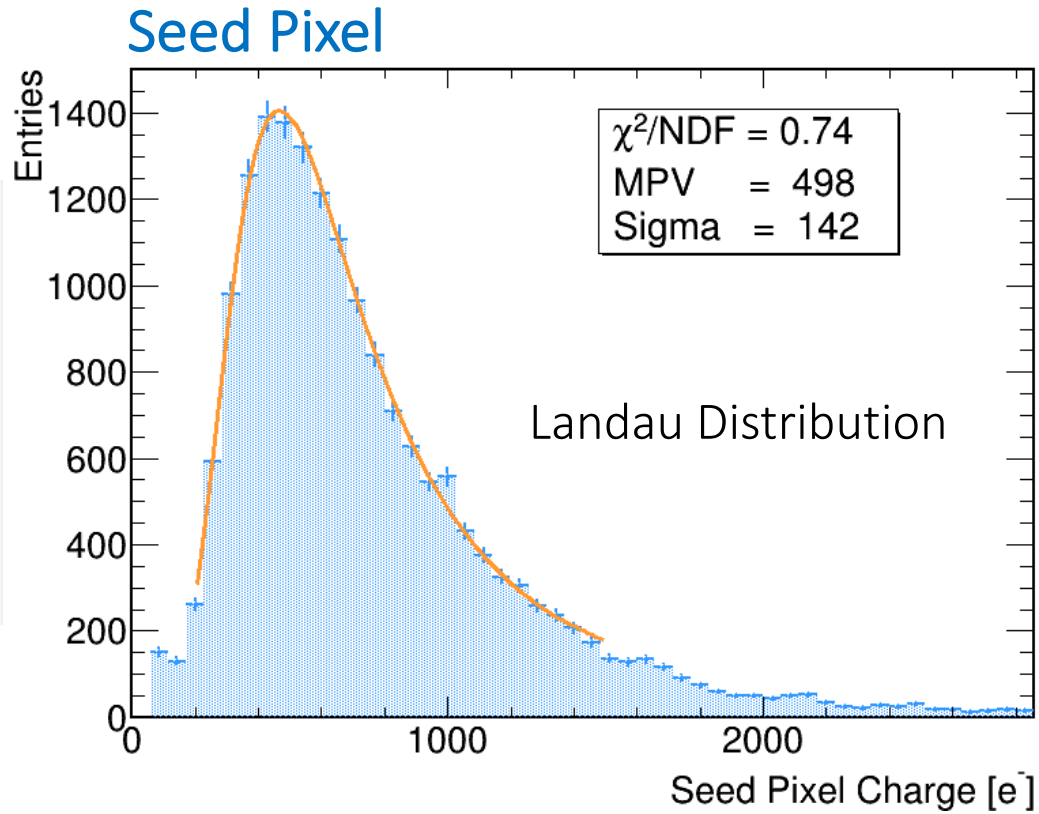
$$\text{Conversion Gain } [\mu V/e^-] = \frac{V_{\text{calib}}\ [V] \times 10^6}{1640\ e^-}$$

5.9 keV photon generates ~1640 eh pairs

Response to MIPs

- Experimental setup to evaluate performance with ^{90}Sr
- Scintillator read out with **SiPM** to provide trigger signal

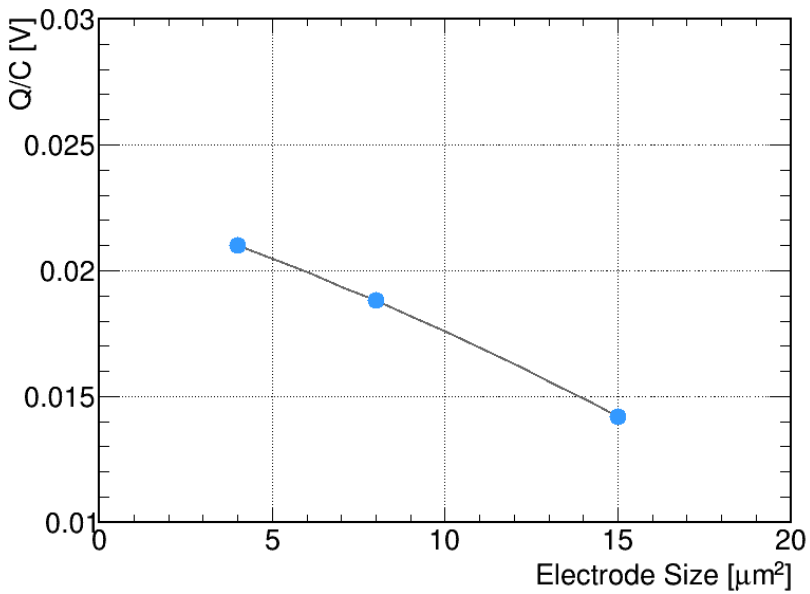


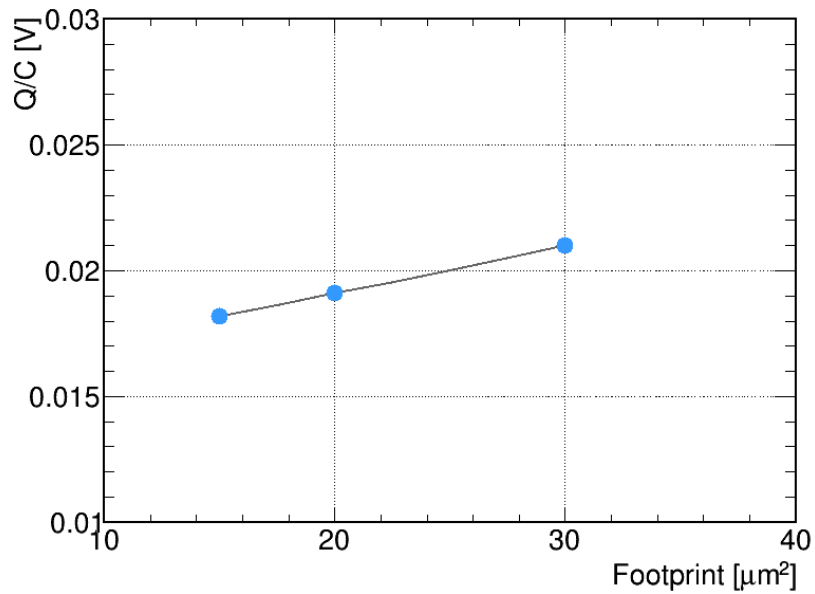


Charge-over-Capacitance

$$C\ [fF] = \frac{1640\ [e] \times 1.6 \times 10^{-19}\ [C/e]}{V_{\text{calib}}\ [V]/g_b} \times 10^{15}$$

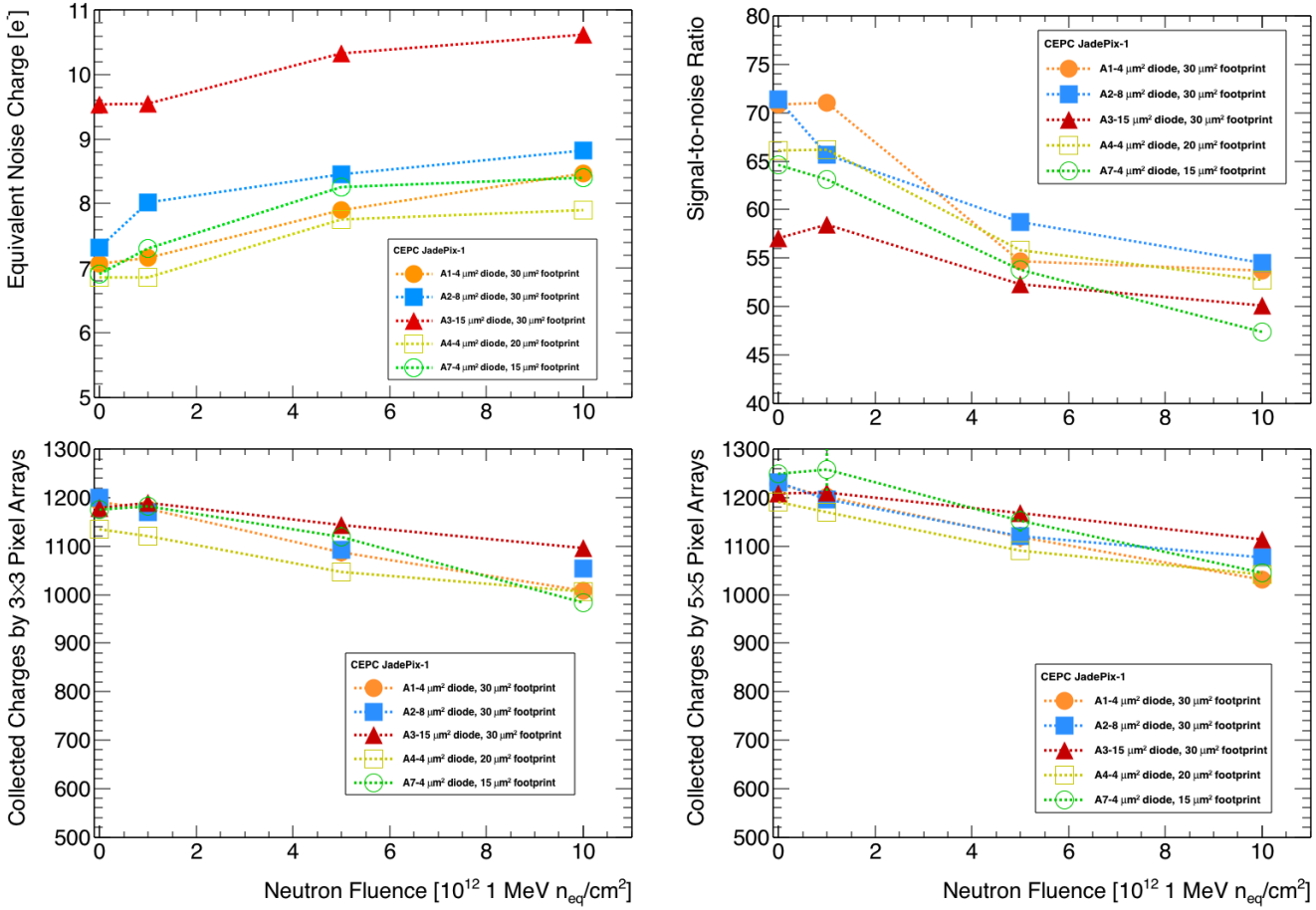
- Small electrode and large footprint preferred to achieve high Q/C ratio → reduction in analog power consumption





Performance Irradiation

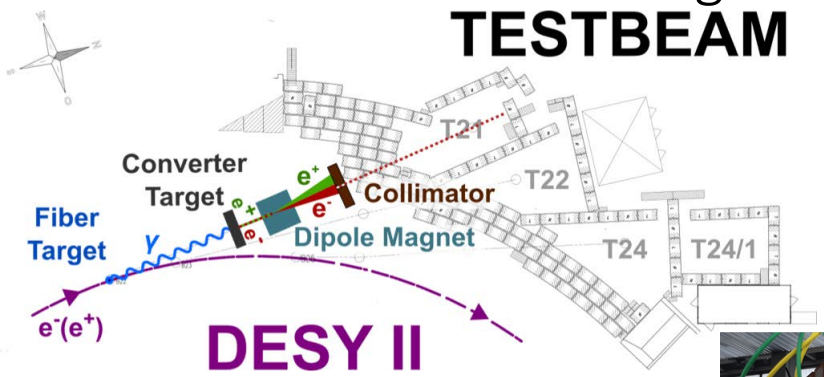
- Neutron irradiation at 10^{12}, 5×10^{12} and 10^{13} 1MeV n_{eq}/cm^2
- Larger diode size ($A1 > A2 > A3$) more radiation hard

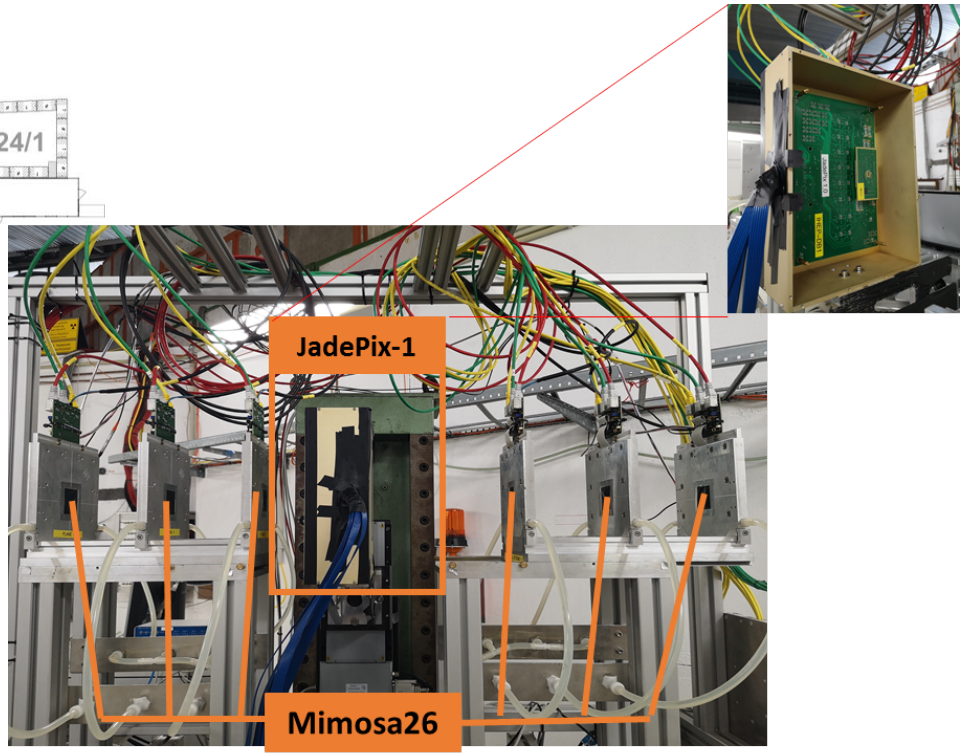


BEAM TEST @ DESY

Special acknowledgements to the DESY Test Beam Facility

- JadePix-1 sensors brought to DESY for beam tests last Sept.



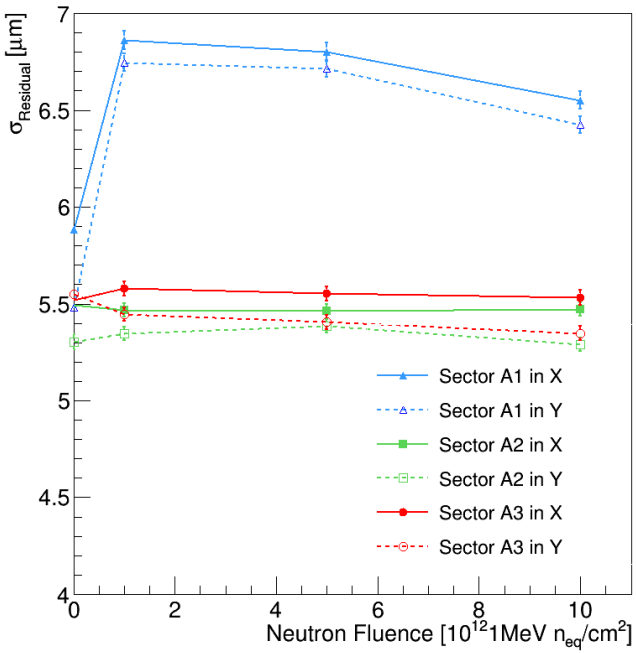


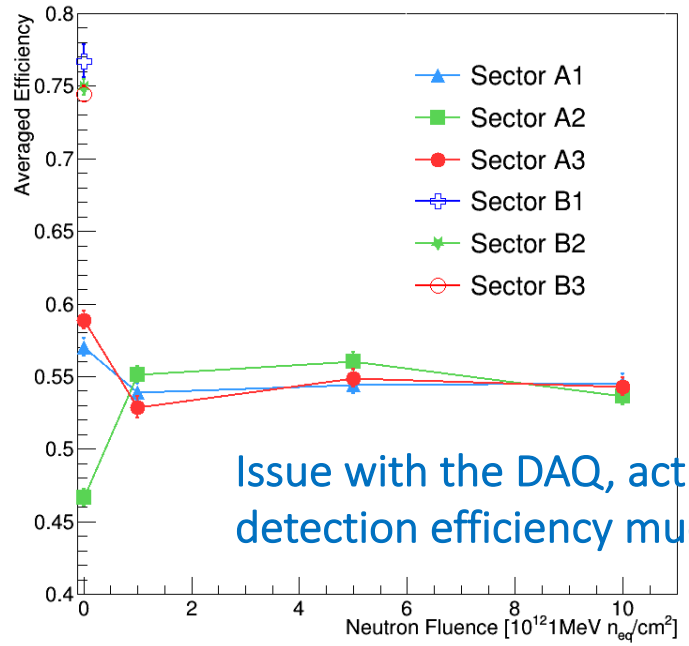
Beam energy 4.4 GeV

- Offline track reconstruction with EUTelescope

JadePix-1 Resolutions & Efficiencies

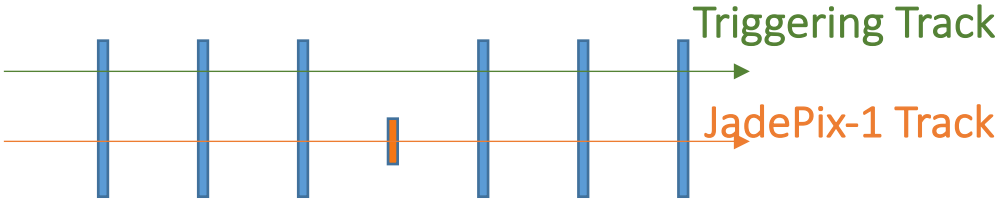
- Resolutions & efficiencies derived for different diode geometries before and after neutron irradiation





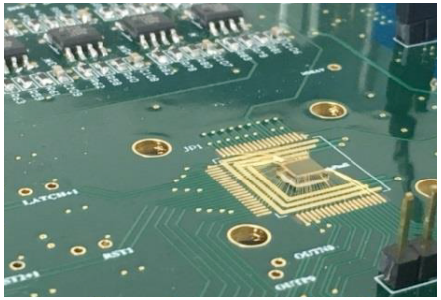
Issue with the DAQ, actual detection efficiency much higher

Beam telescope resolution to extracted to derive pixel resolutions

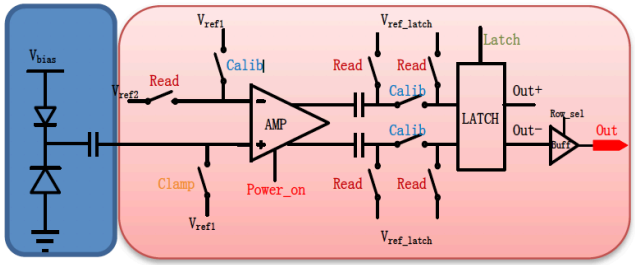


Funded by MOST 1

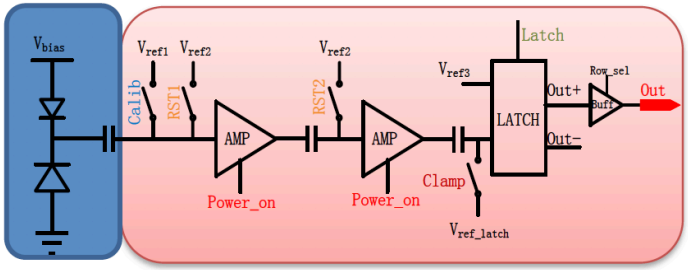
JADEPIX-2 DESIGN & CHARACTERIZATION



- **Basic specifications** (sensor prototype design):
  - Spatial resolution 3-5 μm
  - Power consumption <100 mW/cm2
  - Integration time 100 μs
- Pixel size 22×22 μm^2, chip size3×3.3 mm2, 96×112 pixels with 8 sub-matrices, rolling shutter readout mode



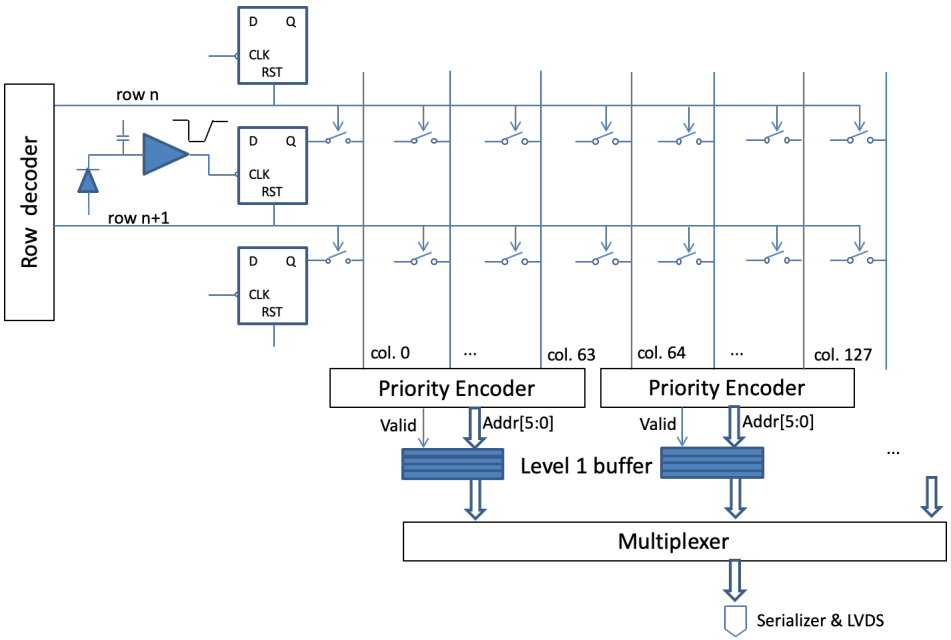
Differential amplifier + dynamic latch

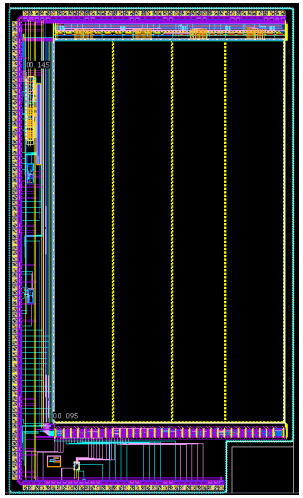


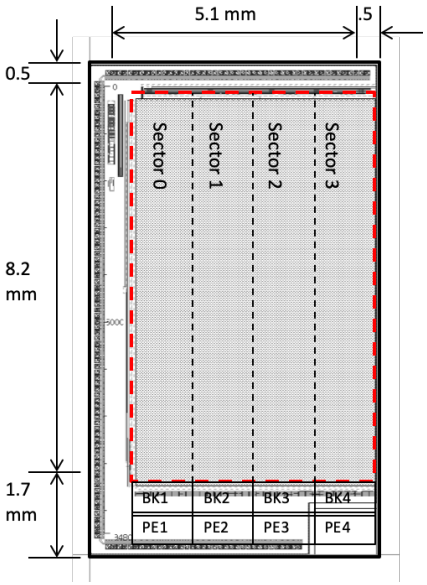
cascaded amplifier (single-ended) + dynamic latch

- Measured **noise performance** measured via S-curve scan
  - TN ~ 11 e$^-$, FPN ~29 e$^-$ → ENC ~31 e$^-$

JADEPIX-3 DESIGN



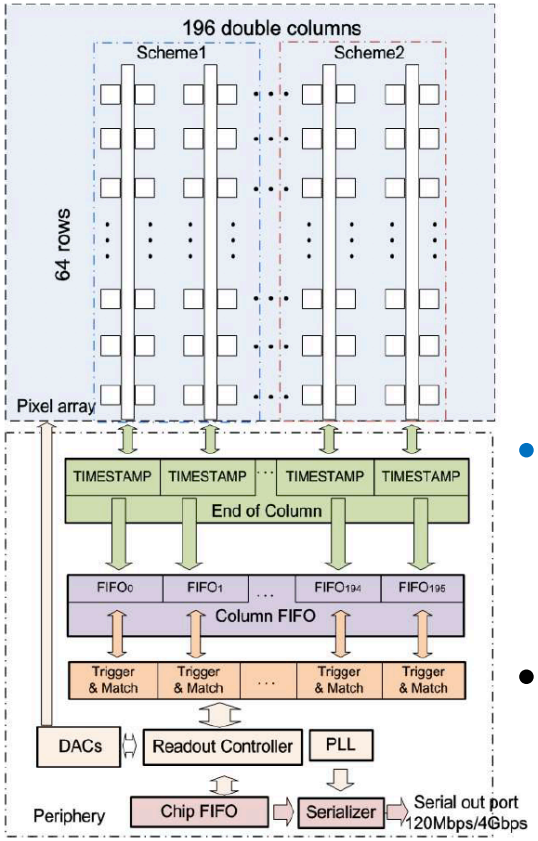


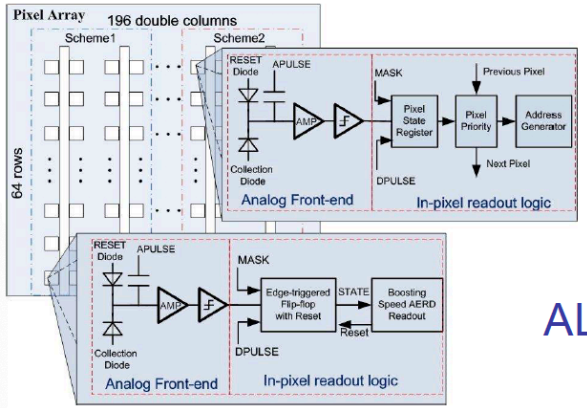


- D flip-flop to register a hit, shared column lines
- End of column priority encoder; zero suppression, 64 columns processed during readout of one row
- Multiplexer controlled by FPGA, flexible readout control
- Submission made in September

Funded by MOST 2

TAICHU-1: TOWARD FULL FUNCTIONALITIES



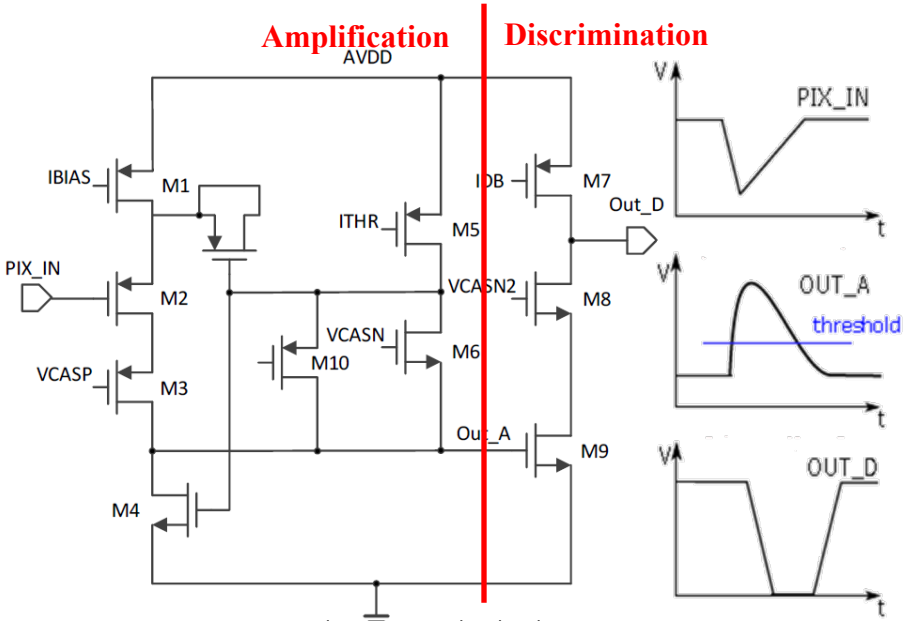


FE-I3-like Pixel

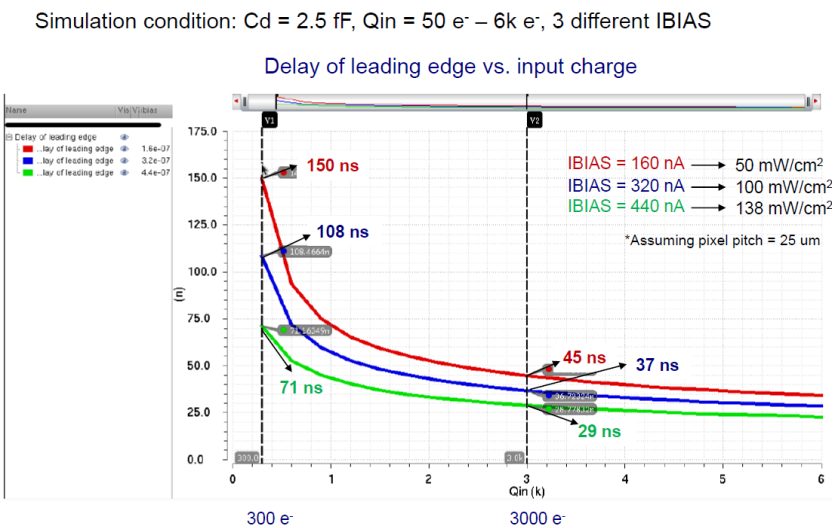
ALPIDE-like Pixel

- Column-drain readout
  - Priority based data driven readout; time stamp at EOC
  - Dead time: 2 CLK for each pixel (50ns @40MHz CLK)
- 2-level FIFO architecture
  - L1: column level, to de-randomize injecting charge
  - L2: chip level, to match in/out data rate between core and interface
- Trigger readout:
  - Coincidence by time stamp, matched event read out

TAICHU-1: IN-PIXEL ELECTRONICS

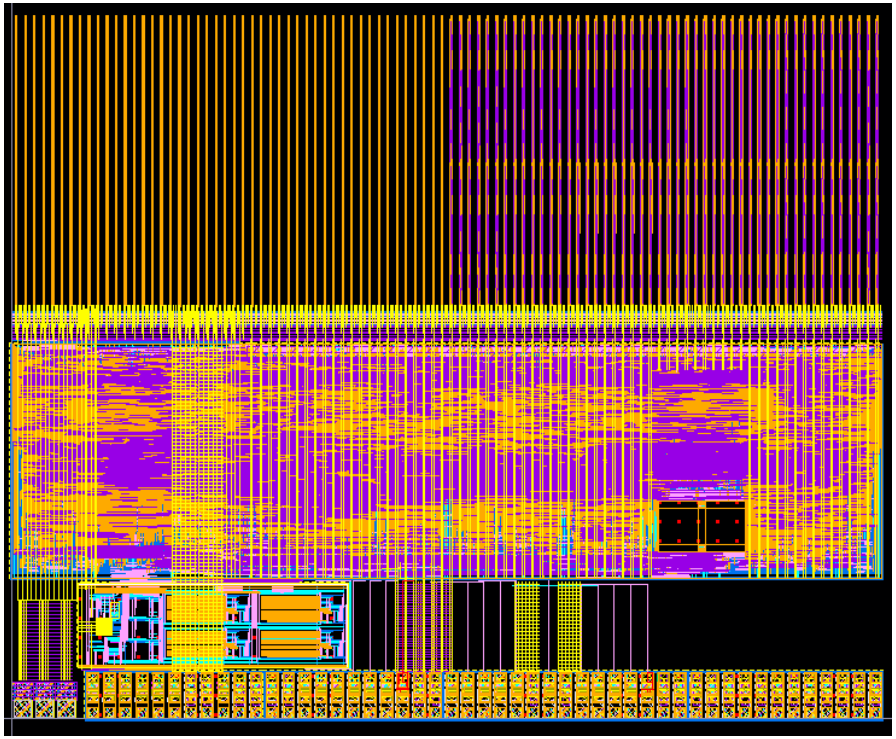


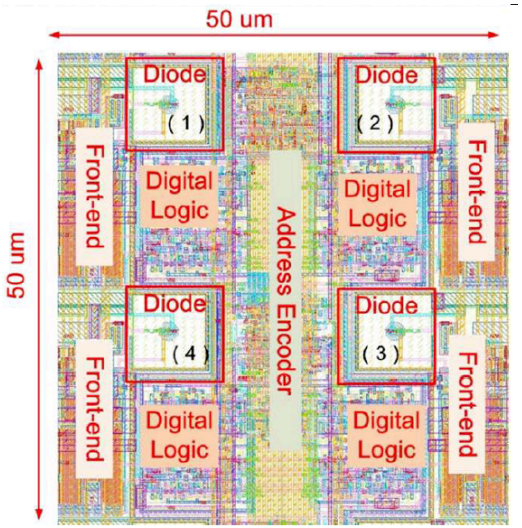
D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042



- Analog design derived from ALPIDE (structure tested in the MIC4 design supported by MOST1)
- Biasing current increased for short peaking time of ~25ns
  - Increased power consumption
  - Awaiting for the **modified TJ process** to achieve fast charge collection
- Digital-in-Pixel scheme: in pixel discrimination & register

TAICHU-1 SUBMISSION



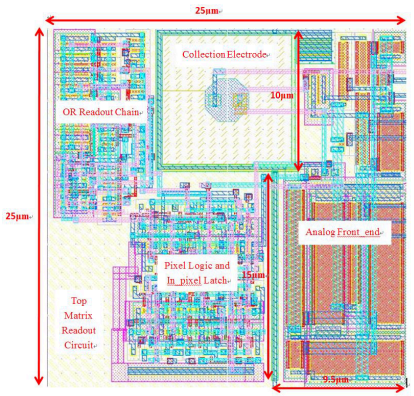


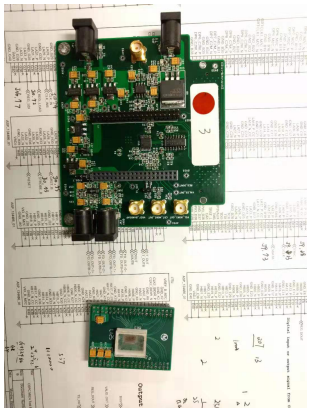
Chip size: 5mm×5mm
Pixel size: 25μm×25μm

- Pixel: 25×25 μm^2, 64×192 Pixel array + Periphery + PLL + Serializer
- Submission made in May, chips expected to be back soon;
- Test boards being designed, detailed characterization later

Other Variants

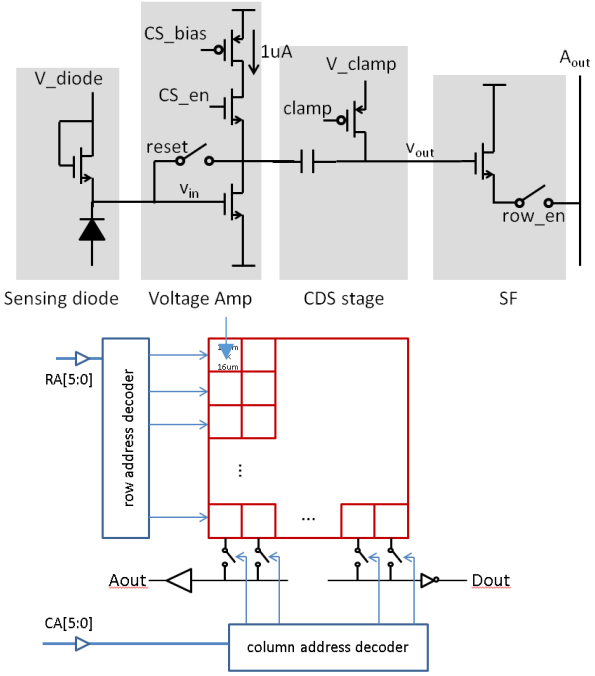
- MIC4 (MAPS In CCNU4)
- Pixel size: 25 × 25 μm2
- Matrix: 128 rows × 64 columns
- Zero suppression in columns
- High speed data link 1.2 Gbps





- Front end design: ALPIDE / CSA
- Fast readout: AERD (Address-Encoder and Reset-Decoder) to

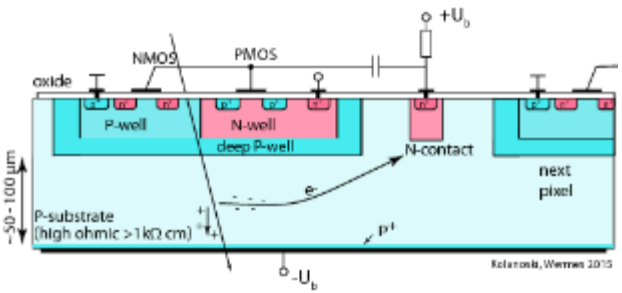
- CPV2 (Compact Pixel for Vertex)
- SOI Process: full depletion→ large signal→ simplified in-pixel circuit→small pixel (16×16 μm^2)
- Matrix: 64 rows × 64 columns



CMOS Tracker

- Large tracking area to be covered with silicon sensors
- Not intended to start sensor design from scratch → limited R&D time and no need to re-invent the wheel
- CMOS pixel sensors proposed for the ATLAS outer most pixel layer (and strip) but not matured enough for construction → opportunity for the CEPC tracker

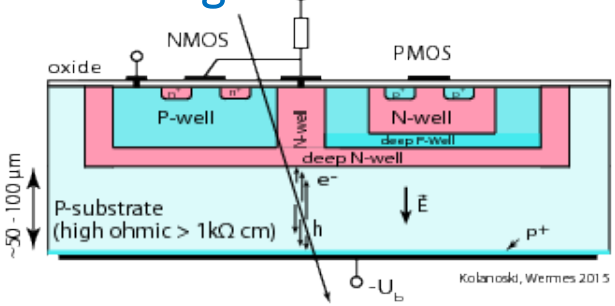
Small fill factor



TJ MALTA/MonoPix (TJ HR-CMOS 0.18 um)

OverMOS (TJ HR-CMOS 0.18 um)

Large fill factor



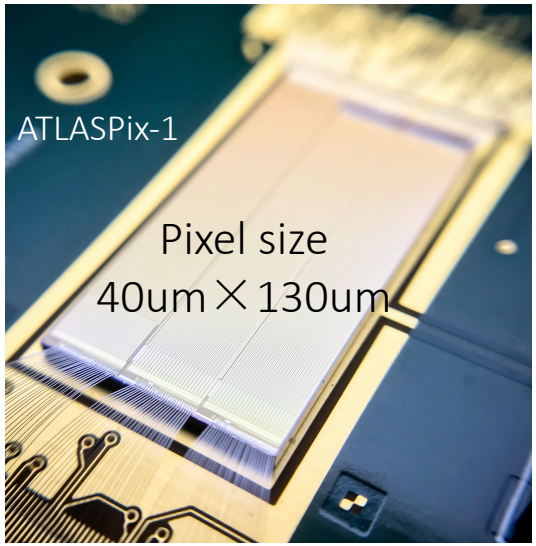
ATLASPix (AMS/TSI HV-CMOS 0.18 um)

LF-MonoPix (LFoundry HV-CMOS 0.15 um)

CHESS 2 (AMS HV-CMOS 0.35 um)

ATLASPIX PERFORMANCE

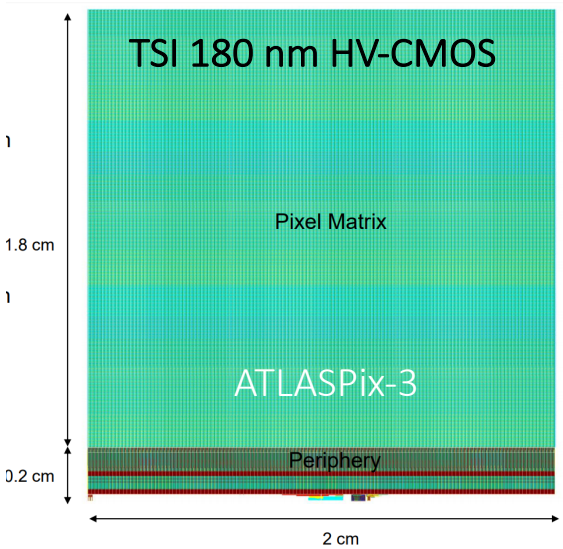
- Fully integrated readout
- Fast charge collection
- Low material budget



AMS 180 nm HV-CMOS, substrate resistivity 20 – 1000 Ω, 100 um thick (can be thinned to 50 um)

ATLASPix-1

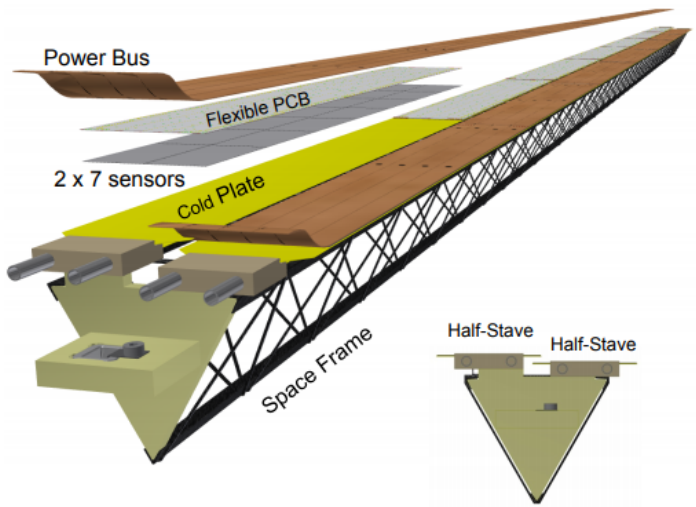
Parameter	Measured	Requirement
Material budget	100 um (50 um possible)	100 um
Spatial resolution	$\sigma_{x/y}$ = 11.3/37.0 um	7/X um
Time resolution	6.8 ns	10 ns
Efficiency	>99.7%	99.5% or higher
Power consumption	2-300 mW/cm^2	200 mW/cm^2



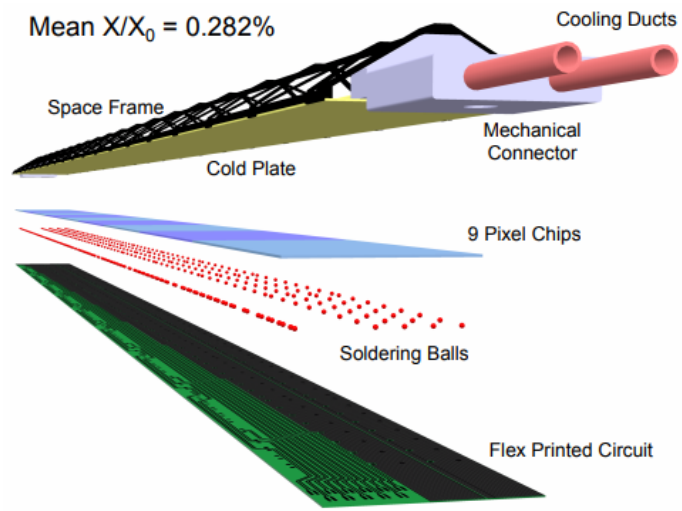
Supporting Structure

More discussion in Daniel Muenstermann's talk at the Oxford CEPC workshop

ALICE Outer Layer Stave ~0.8% X_0

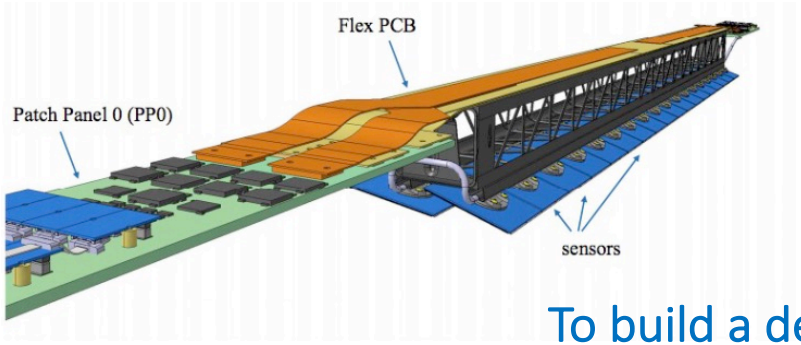


ALICE Inner Layer Stave ~0.3% X_0



ATLAS-ITK: 0.5% X_0 ITK alpine stave (+module)

ATLAS IBL: 0.7% X_0 IBL stave, (+module)



CEPC design target:

0.65% X_0 for stave + modules

Crucial elements:

- Light-weighted carbon truss structure
- Al based flex (prototype with Cu)

To build a demonstrator with components "at hand"

Beyond Demonstrator

- Pixel sensor design optimization toward the requirements of the CEPC silicon tracker
  - Pixel size: 50×150 → 25×300
  - Lower power consumption: less demanding if active cooling applied
  - Powering scheme: serial powering to save material budget ?
  - Other functionalities to be discussed
  - Migrate to SMIC or other foundry that we have access to
- Light weighted support structure (stave core)
  - Improved design inspired by ALICE/ATLAS truss structure, longer extension and higher rigidity/stability (challenging to align detector elements with less tracks)
- Tracking system design
  - Not much discussed yet but definitely needed

Initiated by UK institutions, but needs to involve more partners

Summary & Outlook

- Circular Electron Positron Collider (CEPC) proposed for Higgs and electroweak precision measurements

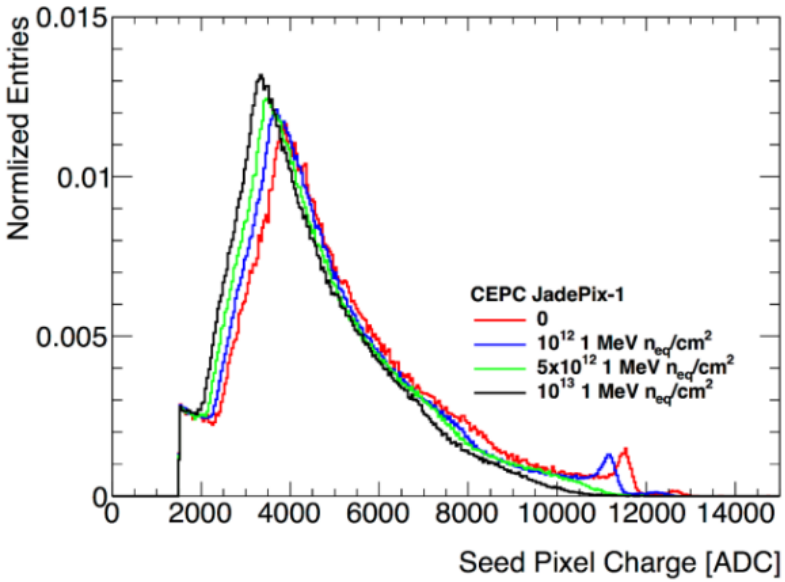
- Baseline tracker layout derived from ILD but subject to optimization and/or re-design toward TDR

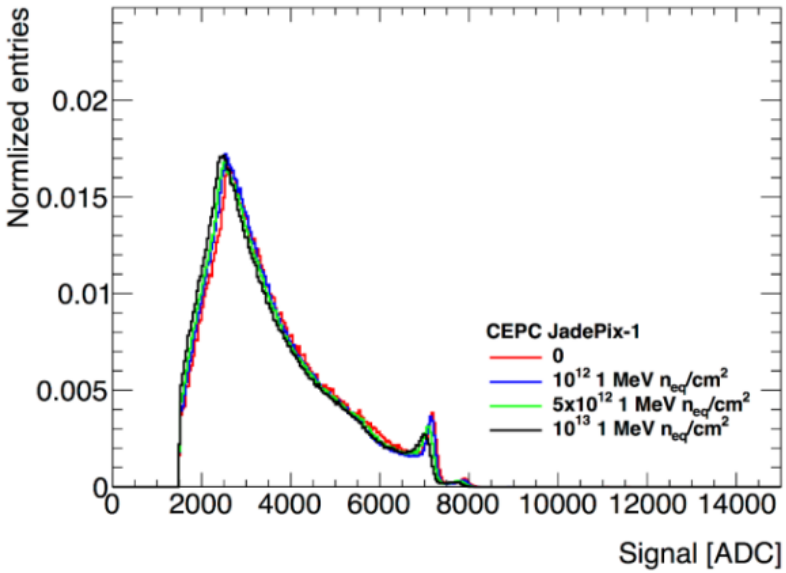
- Vertex: R&D carried out on CMOS pixel sensors to achieve high spatial resolution, fast readout, low power consumption …
  - Prototype sensors: JadePix-1/2/3, MIC4, Taichu-1
- Tracker: effort started on the CMOS tracker
  - To build small stave demonstrator with available components

Thank You Very Much for Your Attention!

Performance after Neutron Irradiation

- Samples sent to a pulsed reactor for neutron irradiation to the fluence levels of 10^{12}, 5×10^{12} and 10^{13} 1MeV n_{eq}/cm^2





- Larger diode size $(A1 > A2 > A3)$ more radiation hard

Resolution Calculation

- JadePix-1 resolution derived as follows:

$$Residual(z) = Unbiased\_Trk(z) - Local\_Local(z)$$

$$\sigma^2_{residual(z)} = \sigma^2_{unbiased\_Trk} + \sigma^2_{local\_hit(z)}$$

$$\sigma_{local\_hit(z)} = \sqrt{\sigma^2_{residual(z)} - \sigma^2_{local\_hit(z)}}$$

Derived from unbiased track fit with EUTelescope track reconstruction

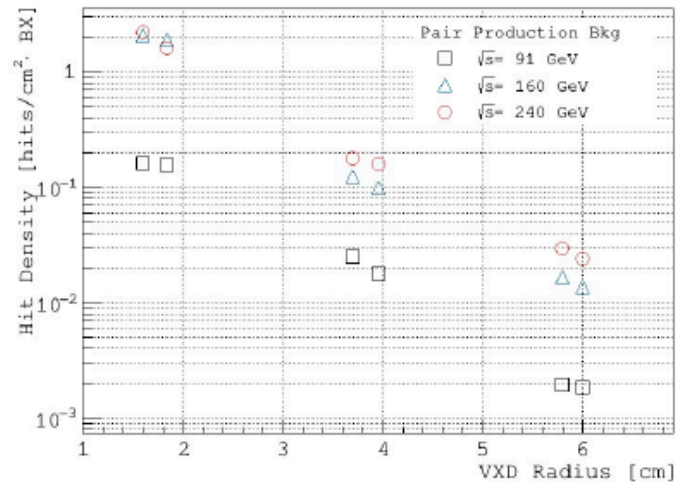
Taken from the resolution estimator developed by S. Spannagel and H. Jansen
https://github.com/simonspa/resolution-simulator
Or http://skulis.web.cern.ch/skulis/telescope/

TAICHU-1

Main specs of the full size chip for high rate vertex detector

- **Bunch spacing**
  - **Higgs: 680ns; W: 210ns; Z: 25ns**
  - **Meaning 40M/s bunches (same as the ATLAS Vertex)**
- **Hit density**
  - **2.5hits/bunch/cm^2 for Higgs/W; 0.2hits/bunch/cm^2 for Z**
- **Cluster size: 3pixels/hit**
  - **Epi- layer thickness：~18μm**
  - **Pixel size：25μm×25μm**

From the CDR of CEPC



For Vertex	Specs	For High rate Vertex	Specs	For Ladder Prototype	Specs
Pixel pitch	<25μm	Hit rate	120MHz/chip	Pixel array	512row×1024col
TID	>1Mrad	Date rate	3.84Gbps --triggerless ~110Mbps --trigger	Power Density	< 200mW/cm^2 (air cooling)
		Dead time	<500ns --for 98% efficiency	Chip size	~1.4cm×2.56cm

ACCESSIBLE CMOS TECHNOLOGIES

1. TowerJazz 0.18 um CIS (already used for JadePix, modified process required for fast charge collection)
2. LFoundry 0.15 um HV-CMOS (NDA signed)
3. SMIC HV-CMOS processes New

LFOUNDRY Solutions for great visions | A SMIC COMPANY

NON-DISCLOSURE AND RESTRICTED USE AGREEMENT
("Agreement")

Between

Institute of High Energy Physics

18B Yuquan Road, Shijingshan District, Beijing 100049, China

and

LFoundry S.r.l.

Via Pacinotti 7– 67051 Avezzano, AQ (Italy)

- all hereinafter referred to as "Party" or "Parties" -

Effective Date: March 25, 2019
Expiration Date: March 24, 2024

SMIC

Semiconductor Manufacturing International Corporation
中芯國際集成電路製造有限公司*

(incorporated in the Cayman Islands with limited liability)
(Stock Code: 981)

DISCLOSEABLE TRANSACTION
DISPOSAL OF SUBSIDIARY

On 29 March 2019 (after trading hours), the Vendor and the Target Company entered into the Share Purchase Agreement with the Purchaser, pursuant to which, among other things, the Vendor agreed to sell and the Purchaser agreed to purchase the Sale Shares at the Consideration in accordance with the terms and conditions of the Share Purchase Agreement.

As certain of the applicable percentage ratios under Chapter 14 of the Listing Rules for the Transaction exceed 5% but are less than 25%, the Transaction constitutes as a discloseable transaction of the Company, and is therefore subject to the relevant reporting and announcement requirements under Chapter 14 of the Listing Rules.

As the Closing is subject to the satisfaction and/or of terms and conditions set out in the Share Purchase Agreement, the Transaction may or may not proceed. Shareholders and potential investors should exercise caution when dealing in the Shares.

SMIC sold LFoundry to JIANGSU CAS-IGBT Co. LTD.

SMIC HV-CMOS Processes

Tech Node	IO Voltage/Tech Type/Char	RF	2019 MPW Booking Cut-Off Date											
			Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
28nm	IO=1.8V | IO=2.5V **CMOS Logic (HP)**	Y	8 Q4S (Fab8)		5 Q58 (Fab2)			18 Q5K (Fab2)			3 Q5Q (Fab2)			
40nm	IO=1.8/2.5V| IO=1.8V| IO=2.5V **CMOS Logic (LL|UP)**	Y		12 Q55 (Fab2)		2 Q62 (Fab2)		4 Q5J (Fab2)			10 Q5R (Fab2)			10 Q5Z (Fab2)
	IO=8/32V **CMOS High Voltage (HV) ***													
55nm	IO=2.5/5V | IO=2.5V **Adv. Emb-Flash (Cu-BEOL) (LL)**						14 Q5G (Fab2)						19 Q5X (Fab2)	
	IO=1.8/2.5V | IO=1.8V| IO=2.5V **CMOS Logic (LL)**	Y		19 Q56 (Fab2)		2 Q5E (Fab2)			16 Q5M (Fab2)			22 Q5W (Fab2)		
	IO=6/32V | IO=8/32V **CMOS High Voltage (HV) ***													
0.11/0.13um	IO=3.3V **CMOS Logic (GE)|Mixed Signal (GE)**	Y	15 Q54 (Fab1)		19 Q59 (Fab1)		28 Q5H (Fab1)			6 Q5N (Fab1)		15 Q5V (Fab1)		17 Q5Y (Fab1)
0.13um	IO=3.3/5V| IO=5V **Adv. Emb-EEPROM (Cu-BEOL) (LL)**			26 Q57 (Fab1)						27 Q5P (Fab1)				
0.15um	IO=18V **CMOS High Voltage (HV) ***												5 Q61 (Fab1)	
0.153um	IO=3.3V **CMOS Logic (GE)|Mixed Signal (GE)**	Y			12 Q5C (Fab1)									
0.18um	IO=5/6/9/12/16/20/24/30/35/40 **BCD V3E (EP) ***	Y									10 Q5T (Fab1)			
0.18um	IO=3.3V **CMOS Logic (GE)|Mixed Signal (GE)**	Y	8 Q53 (Fab1)				7 Q5F (Fab1)				3 Q5S (Fab1)			
	IO=3.3V **CMOS Logic (GE)|Mixed Signal (GE)** IO=5/6/9/12/16/20/24/30/35/40V **BCDM***	Y			5 Q5B (Fab7)				9 Q5L (Fab7)				12 Q60 (Fab1)	
	IO=3.3/5V| IO=5V **EEPROM Embedded (GE)**					9 Q5D (Fab1)						8 Q5U (Fab7)		

* 2019 new offered feature: 40nm/55nm/0.15um HV & 0.18um BCD

Version: 4.3 Update Date: 2019-1-21

Note: Please login SMIC-Now to find the most updated MPW schedule. (请登录Smic-Now以查阅最新MPW Schedule.)

New processes to be tried out (test structures to be submitted) …