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## The ALICE ITS Upgrade Readout and Power System

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For the CERN LHC Run 3, the ALICE experiment completely redesigned the Inner Tracking System, now consisting of seven cylindrical layers instrumented with 24120 Monolithic Active Pixel Sensors (MAPS), covering a total surface area of 10 m<sup>2</sup>. The readout and powering systems are composed of 192 identical Readout Units (RUs) and 142 Power Boards (PBs), respectively, and have complete control over all sensor operations, including power management, triggering, data readout and slow control. In the novel ITS the MAPS sensors directly drive the differential high-speed links connecting them to the Readout Units, making it mandatory to place the readout system as close as possible to the detector to ensure reliable connection up to the design bitrate of 1.2 Gb/s. The power system is similarly located as close as possible to the detector in order to minimize the power loss due to the cables, and actually shares the same crates with the readout system within the magnet yoke. The ITS readout system is connected to the counting room and to the Central Trigger Processor network through 960 Versatile Link optical channels, which allow sustaining a total data rate in excess of 1 Tb/s upstream. This ensures the necessary operational margins to cope with interaction rates of 100 kHz. As the entire system relies on the optical links for both data acquisition and detector control, a CAN-bus network ensures that there is a backup control path should the optical links fail. The Power Boards also implement several hard-wired automatic threshold switches to selectively cut-off power to sensors in case of anomalous supply conditions.

Due to their installation location, the Readout Units and the Power Boards will both operate at about five meters from the interaction point along the beam axis, and at a radial distance of about one meter. The expected TID at this location, for the entire detector life cycle, is about 10 kRad (safety factor of 10), while the expected flux of particles with sufficient energy (>20 MeV) to induce Single-Event Effects (SEEs) is of the order of 10<sup>3</sup> cm<sup>-2</sup> s<sup>-1</sup>. Despite having to operate in such hostile radiation environment, the Readout Unit uses a commercial SRAM FPGA as main logic core, as well as commercial DC-DC converters for the power supply. All components were extensively tested for TID, while specific design solutions were adopted against SEE, which actually represent the major concern for the operational reliability of the system.

This contribution describes the design of the system, focusing on the key requirements and how they have been addressed, and discuss the overall performance achieved. Solutions adopted to ensure the system radiation hardness and reliability, for both the hardware and firmware part, as well as the lessons learnt during the system design, testing and integration will be highlighted.

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