Optical Links for High Energy Physics Experiments in the Next Decade

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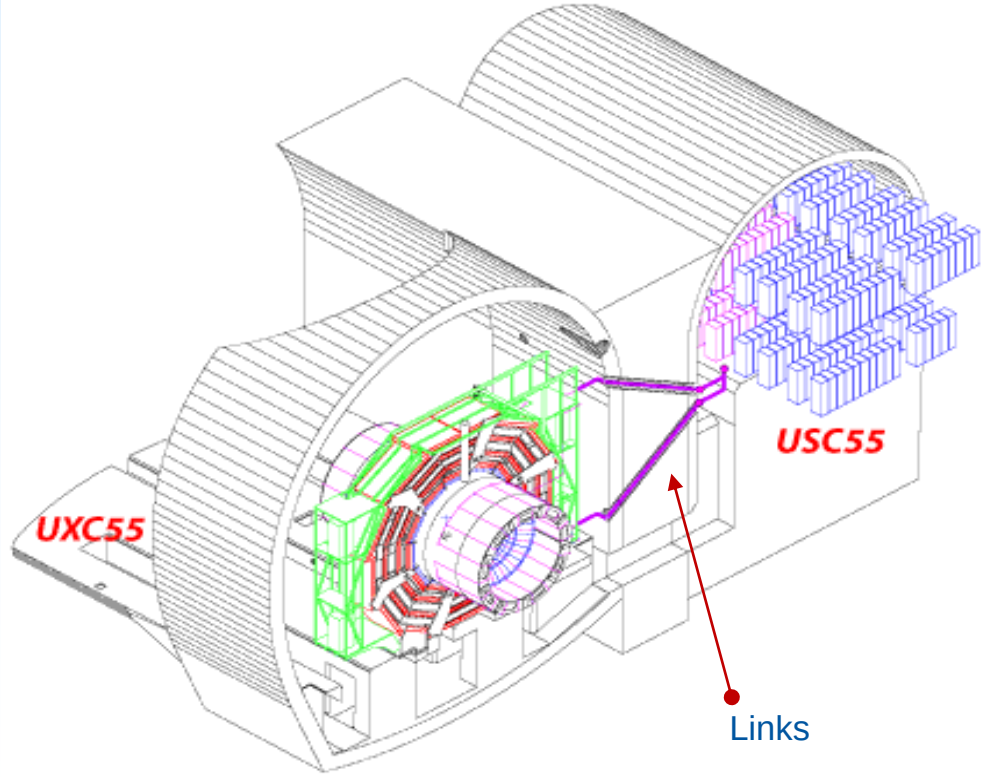
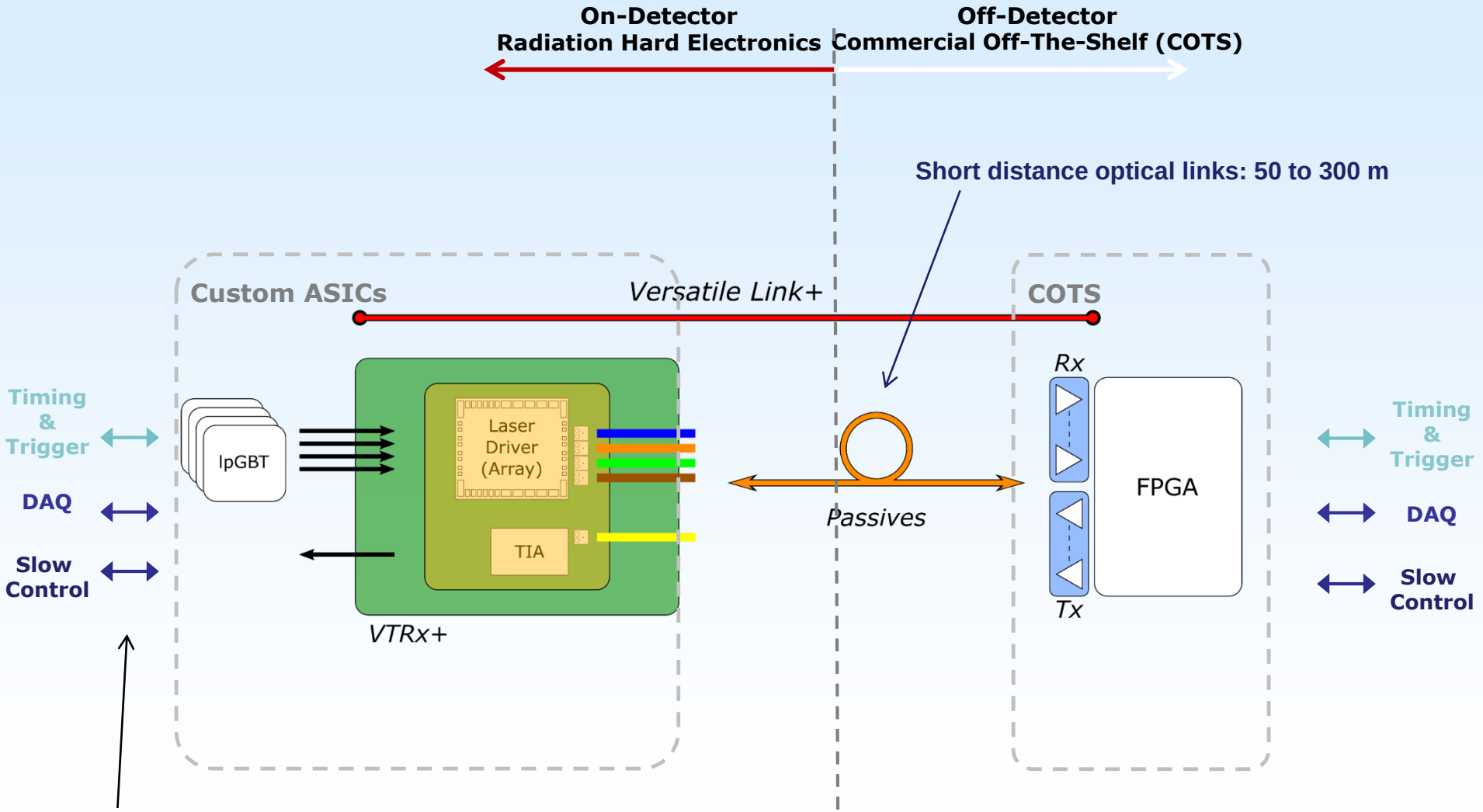
Many thanks to S. Baron, , A. Kraxner, S. Kulis, P. Moreira, C. Scarcella , J. Troska and many others for providing material for this presentation.

Outline

- Performance and limitations of optical links for HL-LHC
- Trends and options for future developments
- Silicon photonics
- Outlook



The GBT and Versatile Link Projects



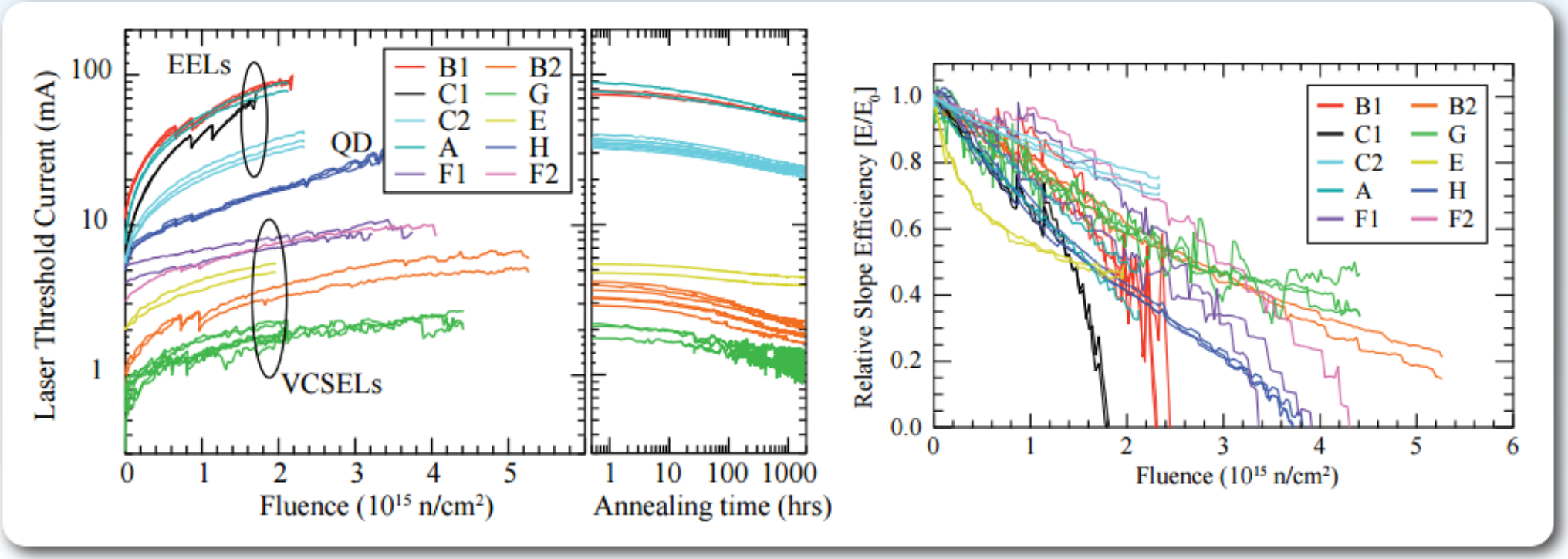
Performance of HL-LHC Links

	Versatile Link	Versatile Link PLUS
Upgrade phase	Phase I	Phase II
Optical mode	Single- and multi-mode	Multi-mode
Flavours	1Tx+1Rx, 2Tx	up to 4Tx (+1Rx)
Radiation resistance	Up to Calorimeter grade	Up to Tracker grade
Form factor	SFP+	Custom miniature
Data rate	Tx/Rx: 5 Gb/s	Up: 5/10 Gb/s, Down: 2.5 Gb/s

	Tolerance level	Dose and fluence
	Calorimeter Grade	1 MGy 1.7×10^{14} neutrons/cm^2 1.7×10^{14} hadrons/cm^2
	Tracker Grade	1 MGy 1×10^{15} neutrons/cm^2 1×10^{15} hadrons/cm^2

Limitations of HL-LHC Links

- Datarate limited by serdes design and qualified technology (65nm)
- Density and scalability limited by active opto array sizes
- Power supply rails limited by VCSEL technology (3.3V down to 2.5V)
- Distance limited by dispersion at 850 nm MM
- Radiation hardness limited by active opto



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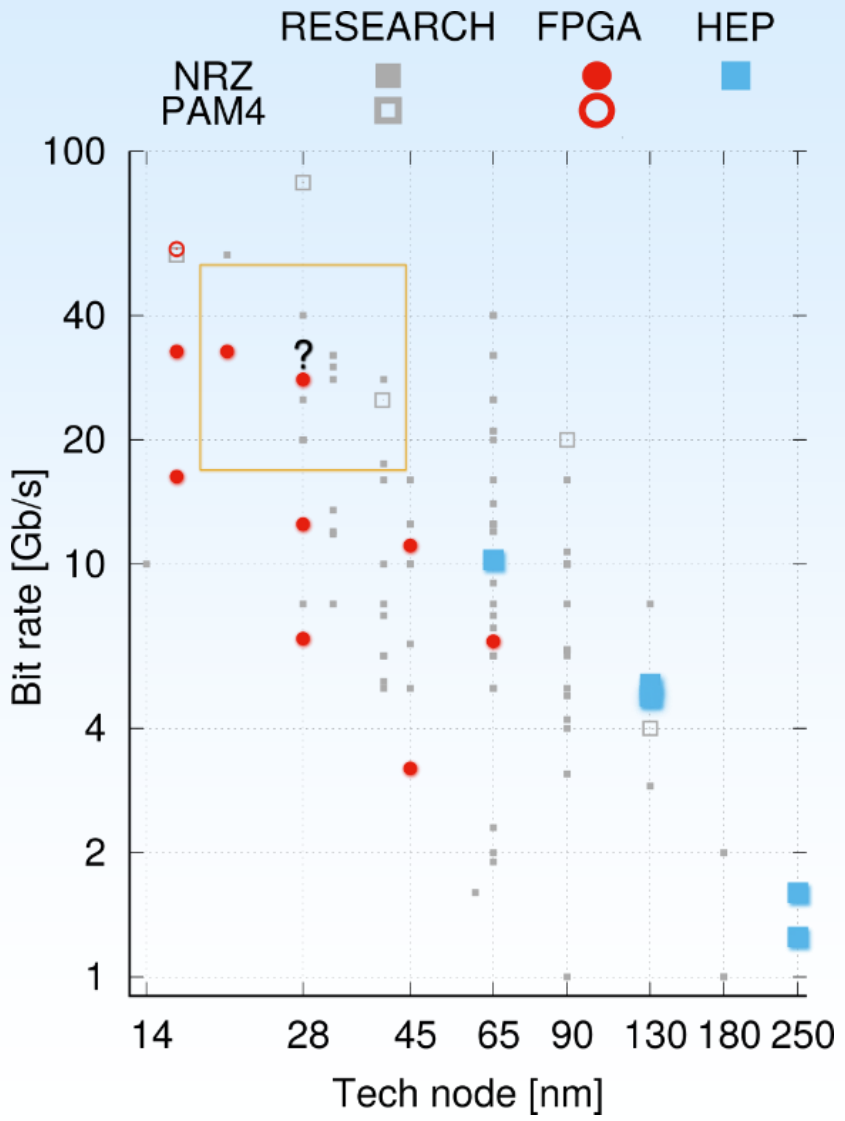
ASICs Technology Trend : Technology Nodes

- **Data rates are highly correlated with the technology nodes**
- **Shift in modulation format** (not technology) can be seen **for highest data rates**
  (NRZ -> PAM4)
- Research papers demonstrate 40 Gb/s NRZ to be possible for technology nodes ≤ 65 nm
- Commercial systems (FPGAs) introduced 30Gb/s + data rates for the 28 nm node and below



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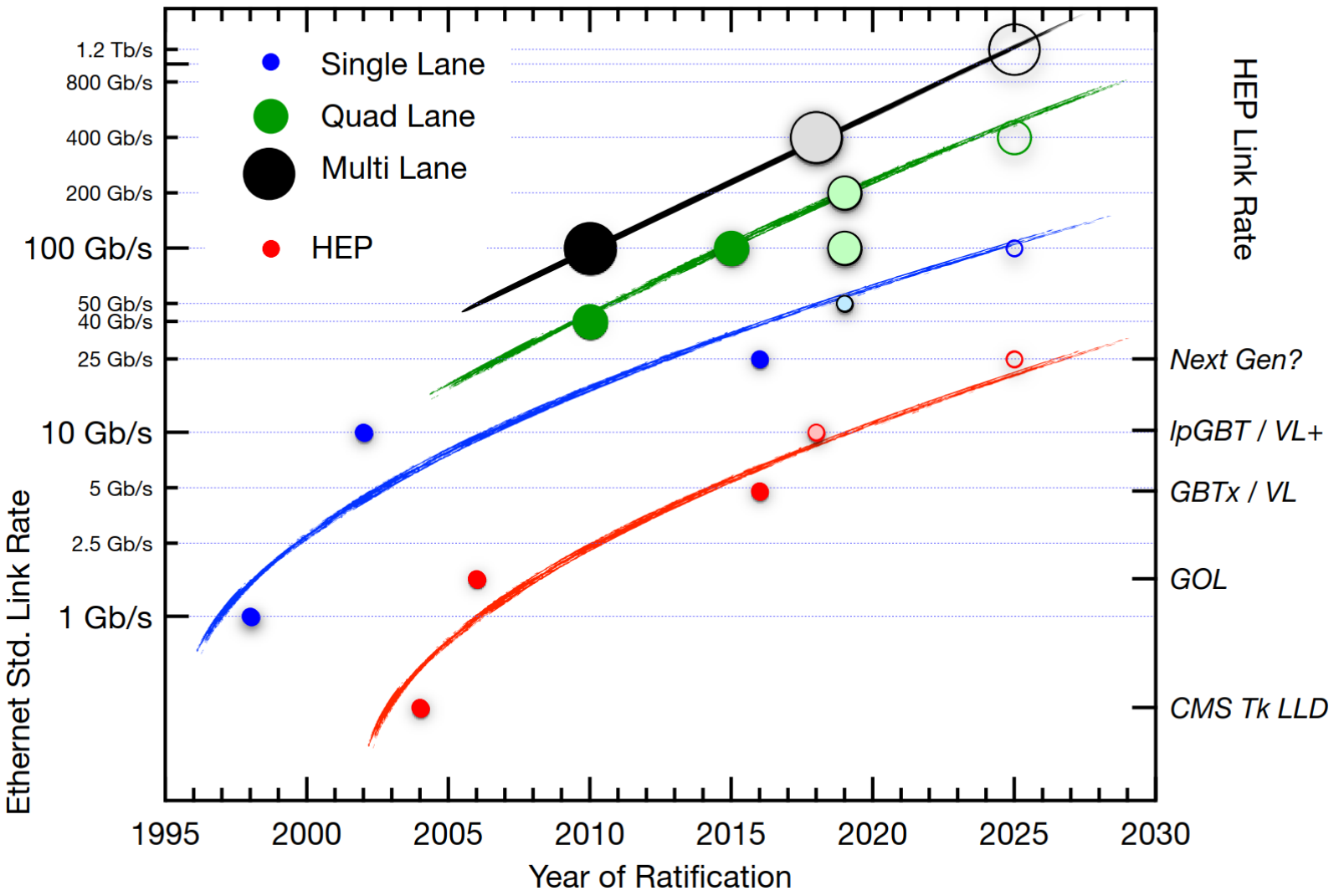
Optoelectronics Technology Trend



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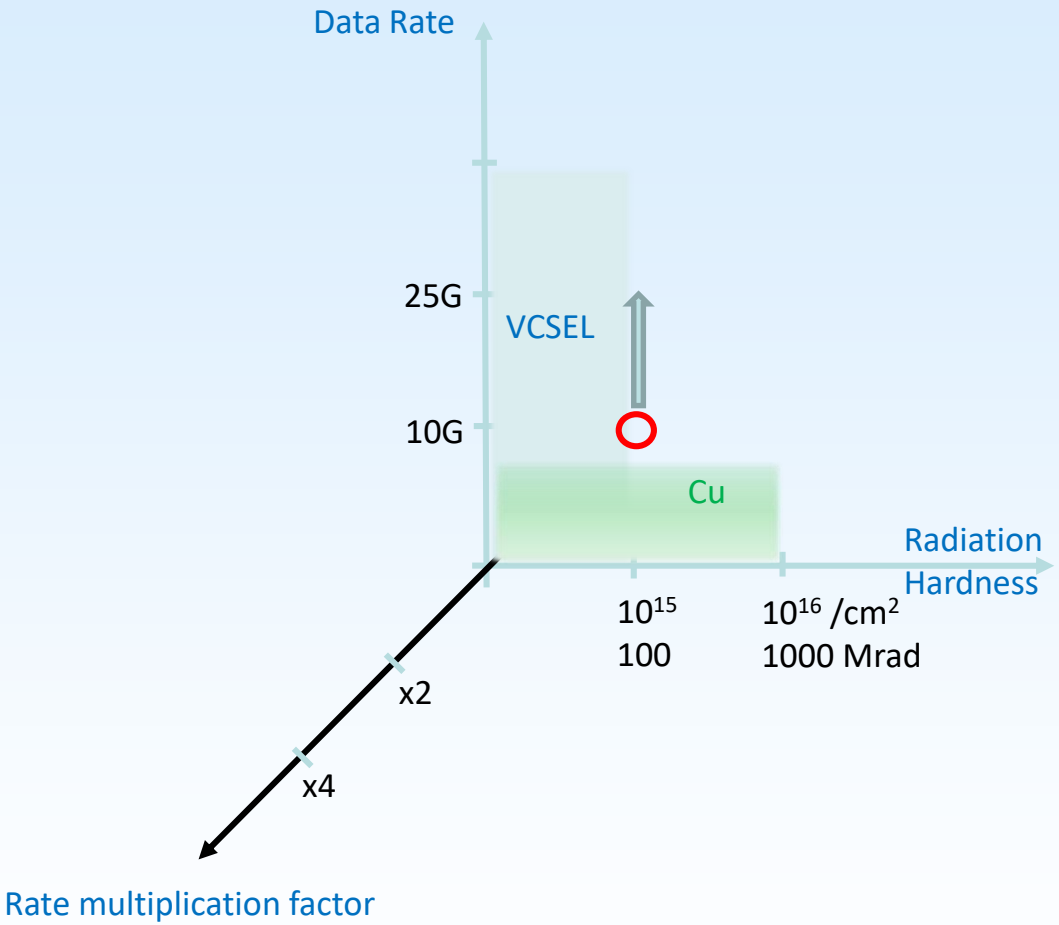
Development Space

Future developments: Higher Data rates

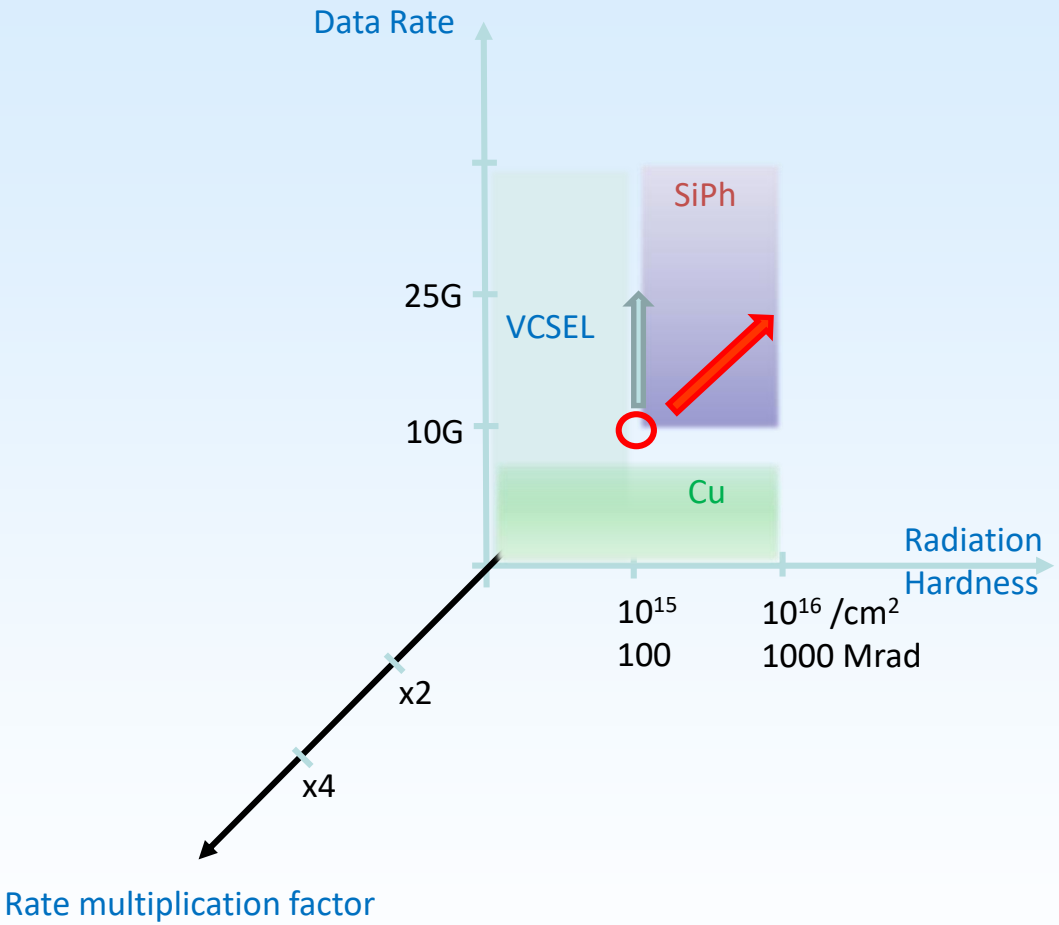


Ongoing development:
LpGBT-VL+ project
HL-LHC, 2020

Future developments:

1. Higher Data rates

Future developments: Si-Photonics



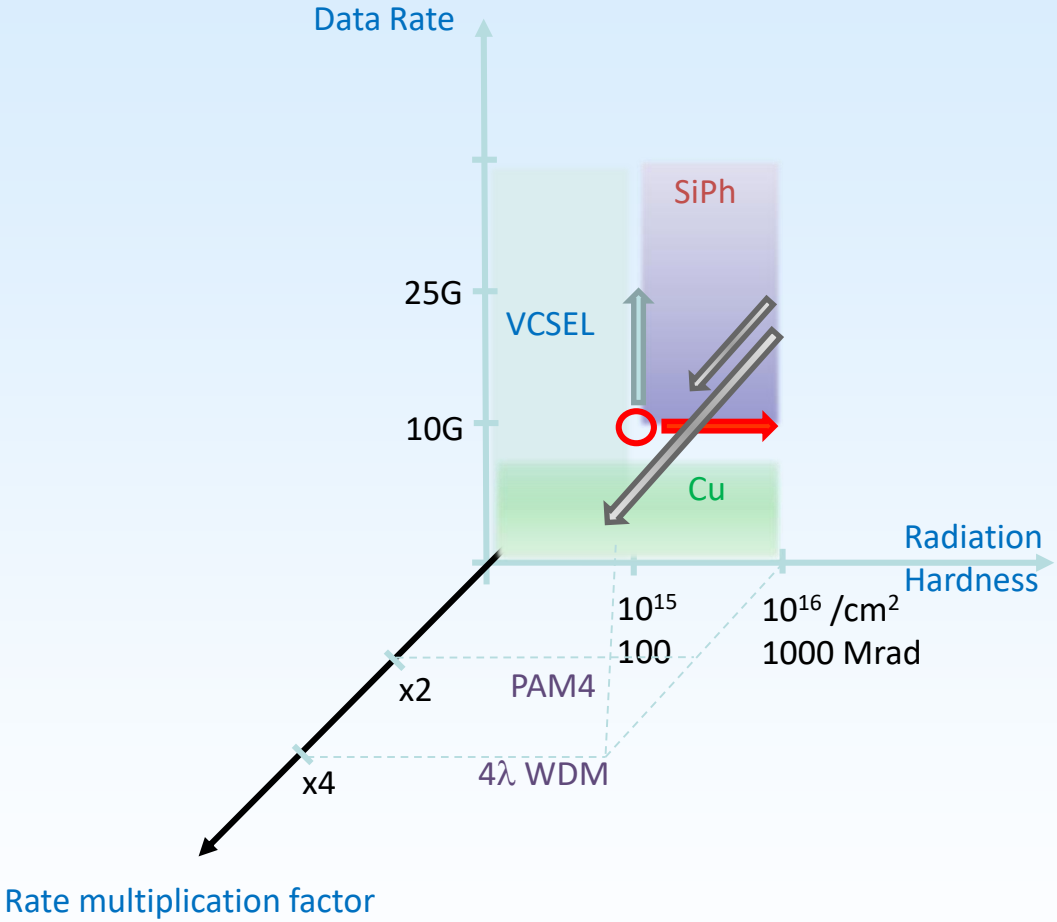
Ongoing development:
LpGBT-VL+ project
HL-LHC, 2020

Future developments:

1. Higher Data rates

2. Si Photonics:

Future developments: Si-Photonics & λ - Muxing & PAM4



Ongoing development:
LpGBT-VL+ project
HL-LHC, 2020

Future developments:

1. Higher Data rates
2. Si Photonics
3. λ Multiplexing and multi-level signalling (PAM)

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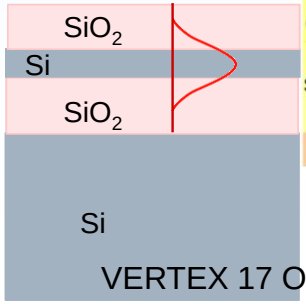
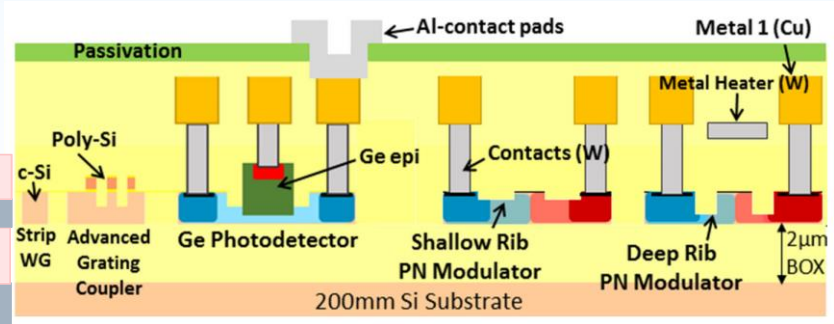
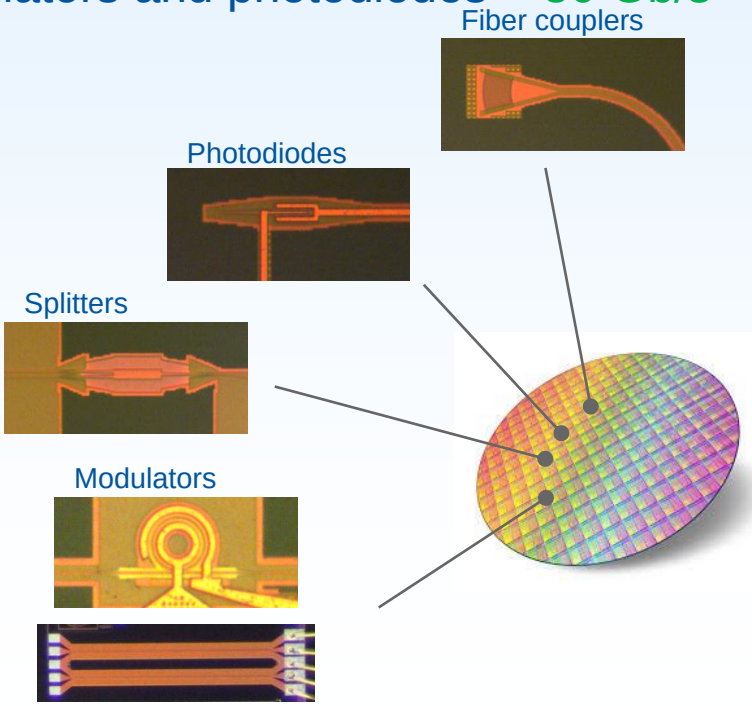
Silicon Photonics: pros

- Leverage existing CMOS infrastructure for Photonic Integration
- The Silicon waveguide embedded into silica cladding medium
- Silicon is patterned (deep UV lithography) with sub-micron precision
- Fabricated in standard CMOS fabs using Silicon SOI wafers
- Large Si/SiO_2 refractive index contrast (~2) allows high device scalability
- Several silicon doping concentrations for high-speed modulators and photodiodes ~ 50 Gb/s
- Ge epitaxy for photodetectors
- Complete platform for optical data links





Pantouvaki et al. IEEE JLT, VOL. 35, NO. 4, FEBRUARY 15, 2017

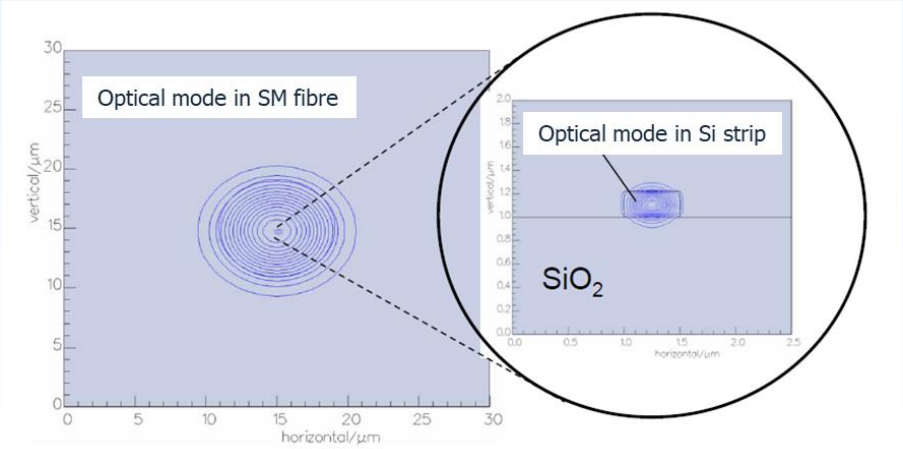


Silicon Photonics: pros and cons

- Leverage existing CMOS infrastructure for Photonic Integration
- The Silicon waveguide embedded into silica cladding medium
- Silicon is patterned (deep UV lithography) with sub-micron precision
- Fabricated in standard CMOS fabs using Silicon SOI wafers
- Large Si/SiO_2 refractive index contrast (~2) allows high device scalability
- Several silicon doping concentrations for high-speed modulators and photodiodes ~ 50 Gb/s
- Ge epitaxy for photodetectors
- Complete platform for optical data links
- Indirect bandgap material

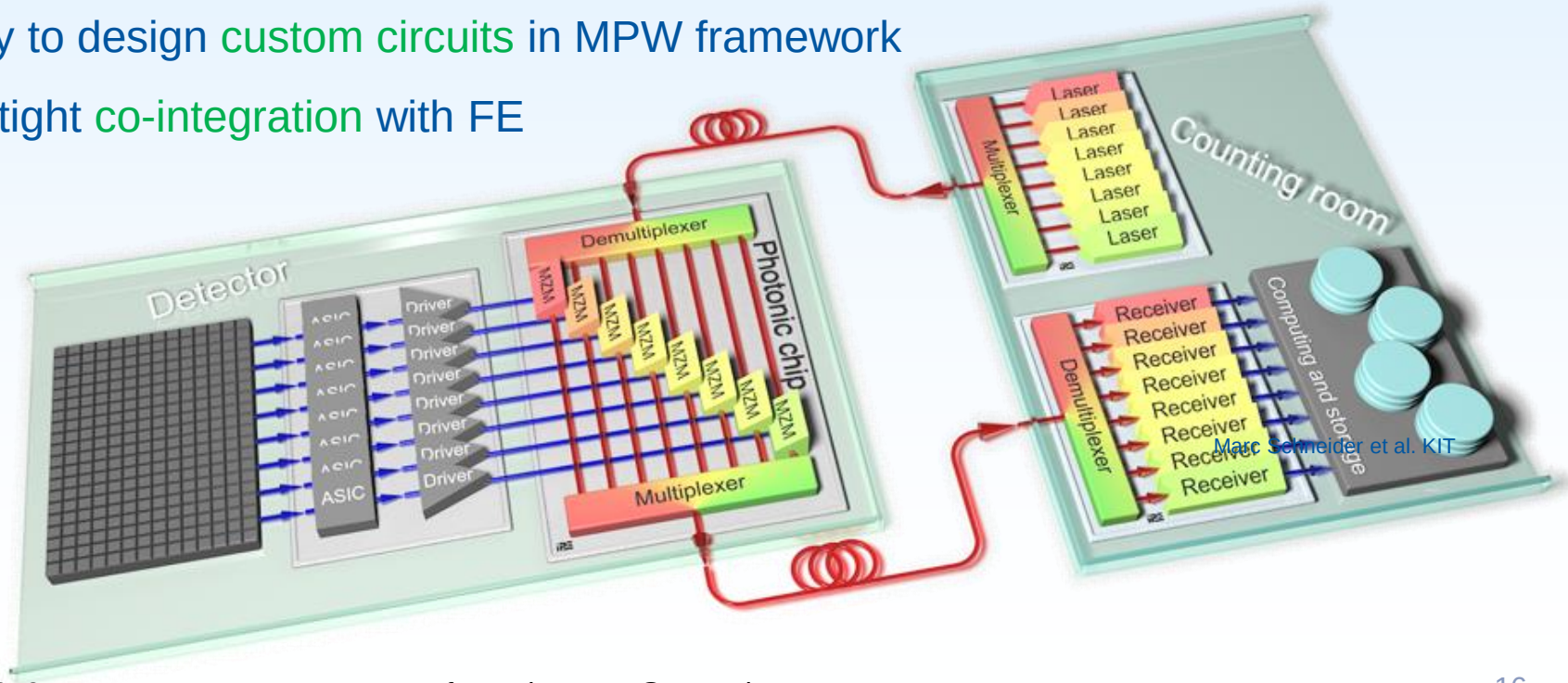
  no monolithic laser integration
- Large Si/SiO_2 refractive index

  large mode mismatch with fiber

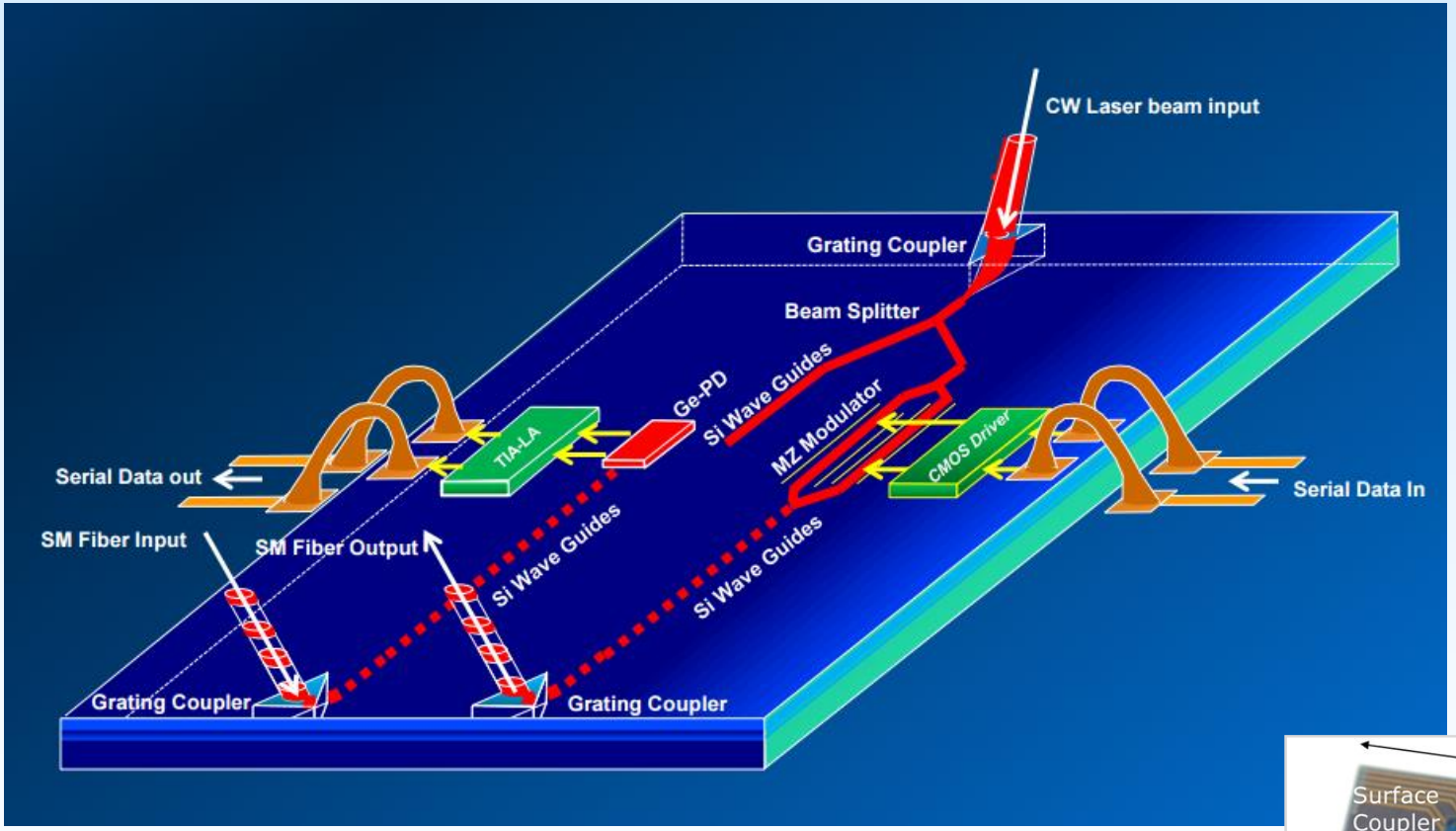


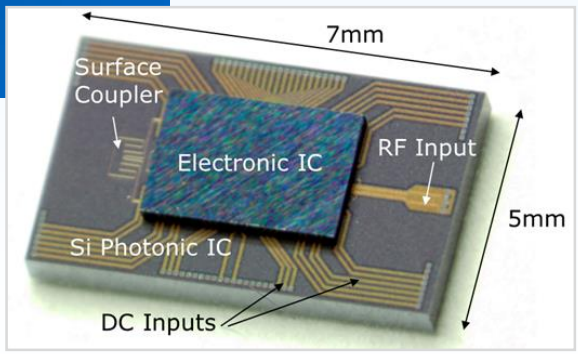
Silicon Photonics: Opportunity for HEP

- Why exploring Silicon Photonics?
  - DC Laser kept out of extreme radiation environments
  - Low power consumption (excl. laser)
  - Single Mode data transfer without dispersion penalty
  - Potential for: > 25 Gb/s NRZ lane rate, Wavelength division multiplexing
  - Possibility to design custom circuits in MPW framework
  - Possible tight co-integration with FE



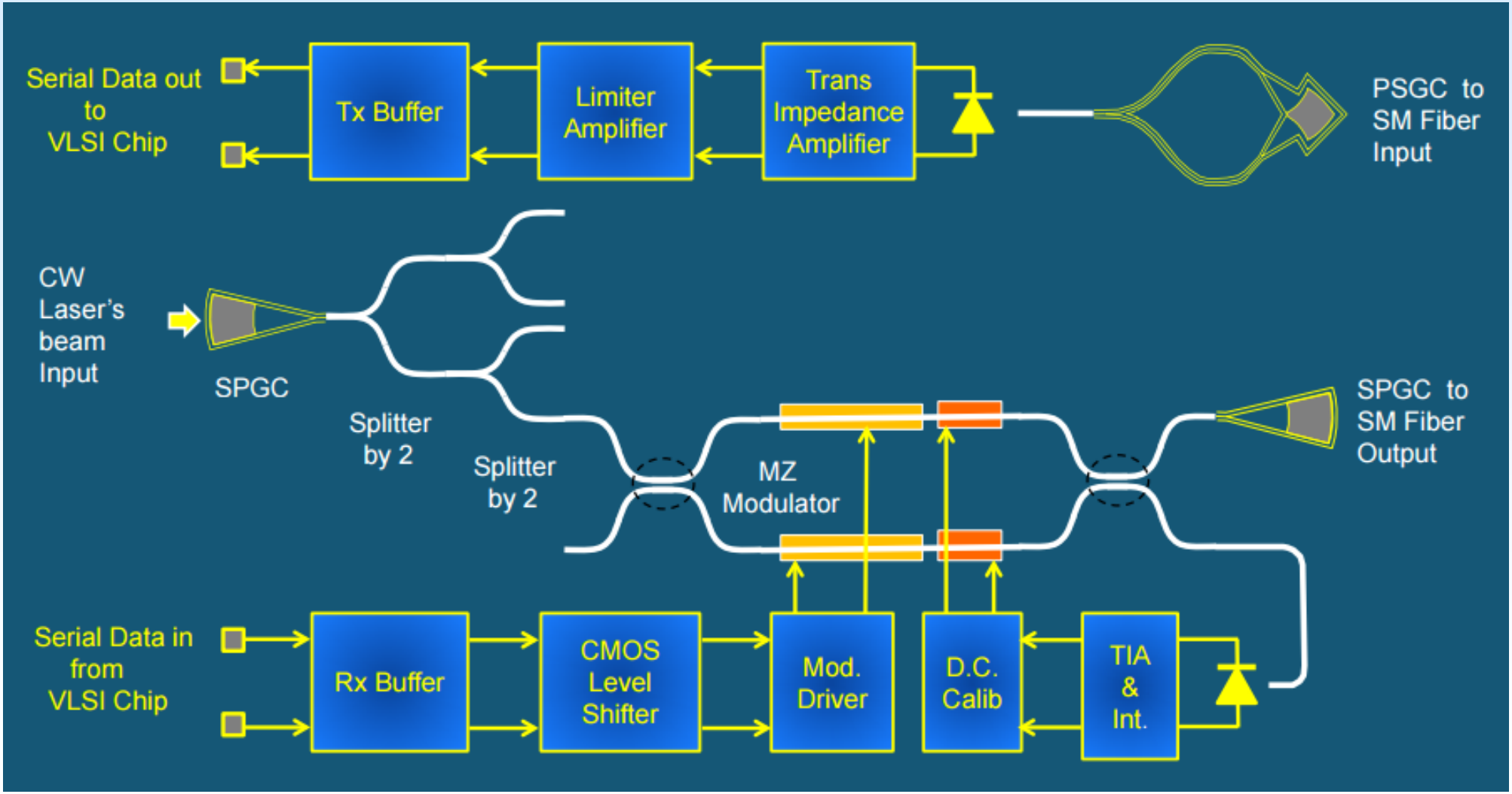
Silicon Photonics Circuit: an Artist Dream





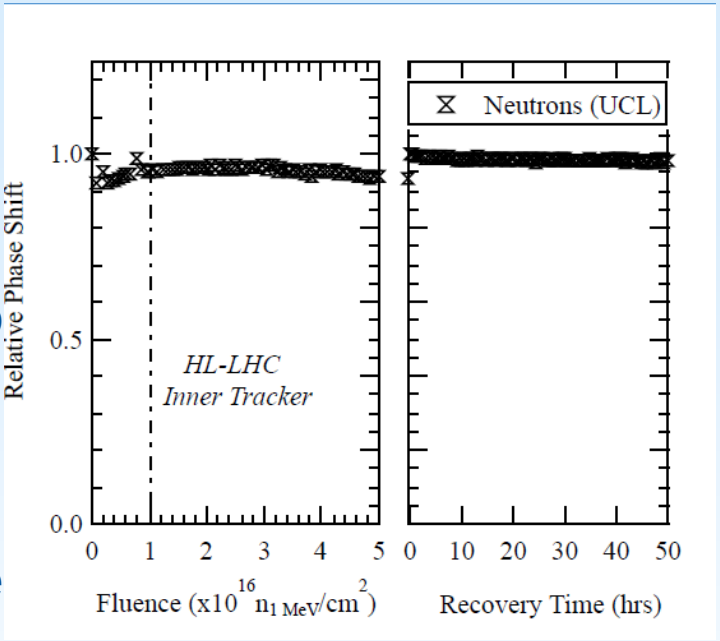
Source: "Silicon Photonics and FDMA PON: Insights from the EU FP7 FABULOUS Project" S. Abrate et all.

Silicon Photonics Circuit: an Engineer Nightmare

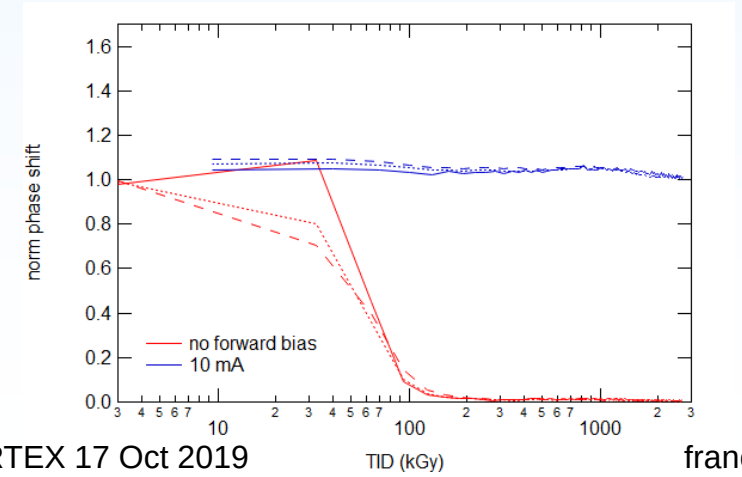


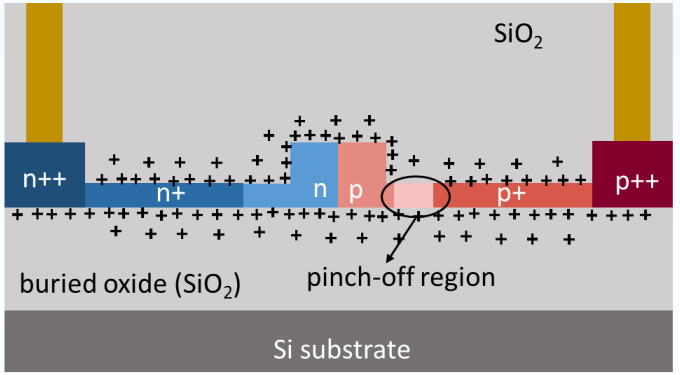
SiPh Modulator Radiation Tolerance

- Silicon Photonics is tolerant to displacement damage



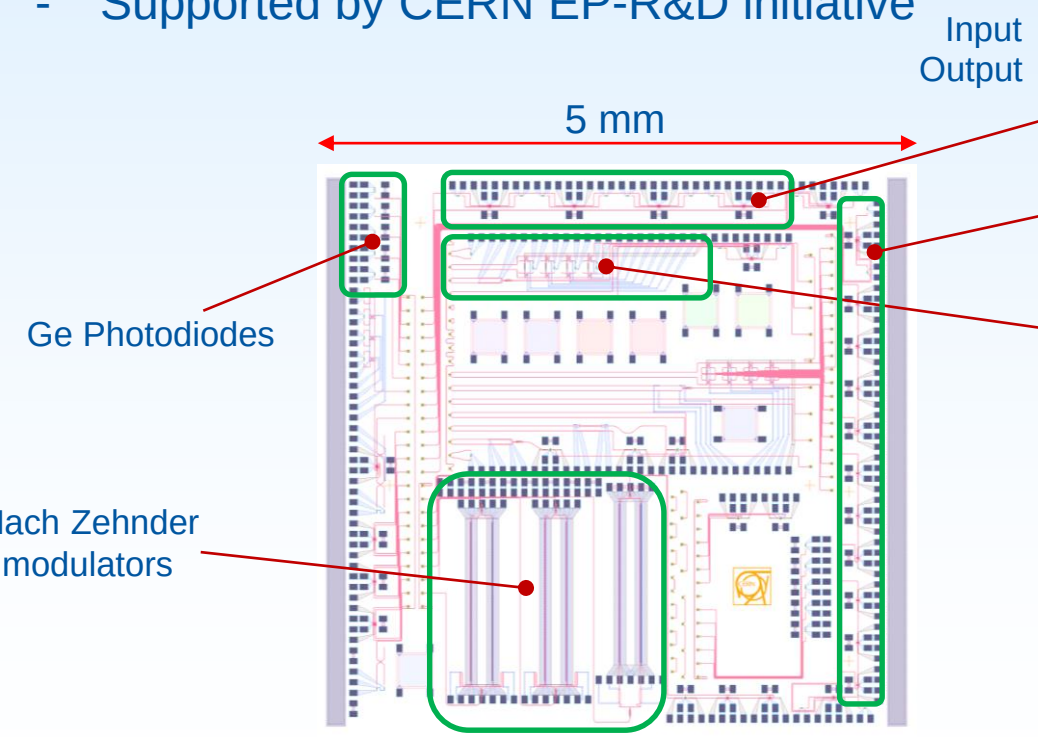
- Like for CMOS electronics, Si modulators are sensitive to TID
  - Optical modulators are based on Silicon p-n junctions embedded in SiO_2 cladding layers
  - TID generates fix positive charge at the Si/SiO_2 interface that pinches-off the junction in the waveguide core

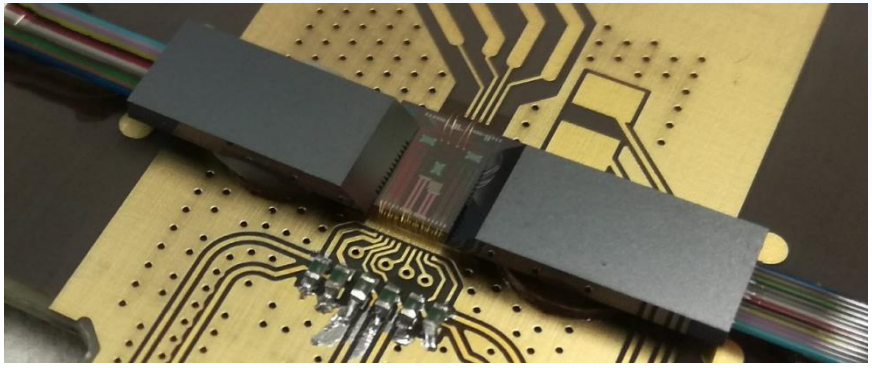




A Silicon Photonics Test Chip

- IMEC MPW (iSiPP50G)
- Instantiates IP building blocks from CERN and IMEC
- Tape-out in June 2019
- Turn around time: 9 months
- Supported by CERN EP-R&D initiative



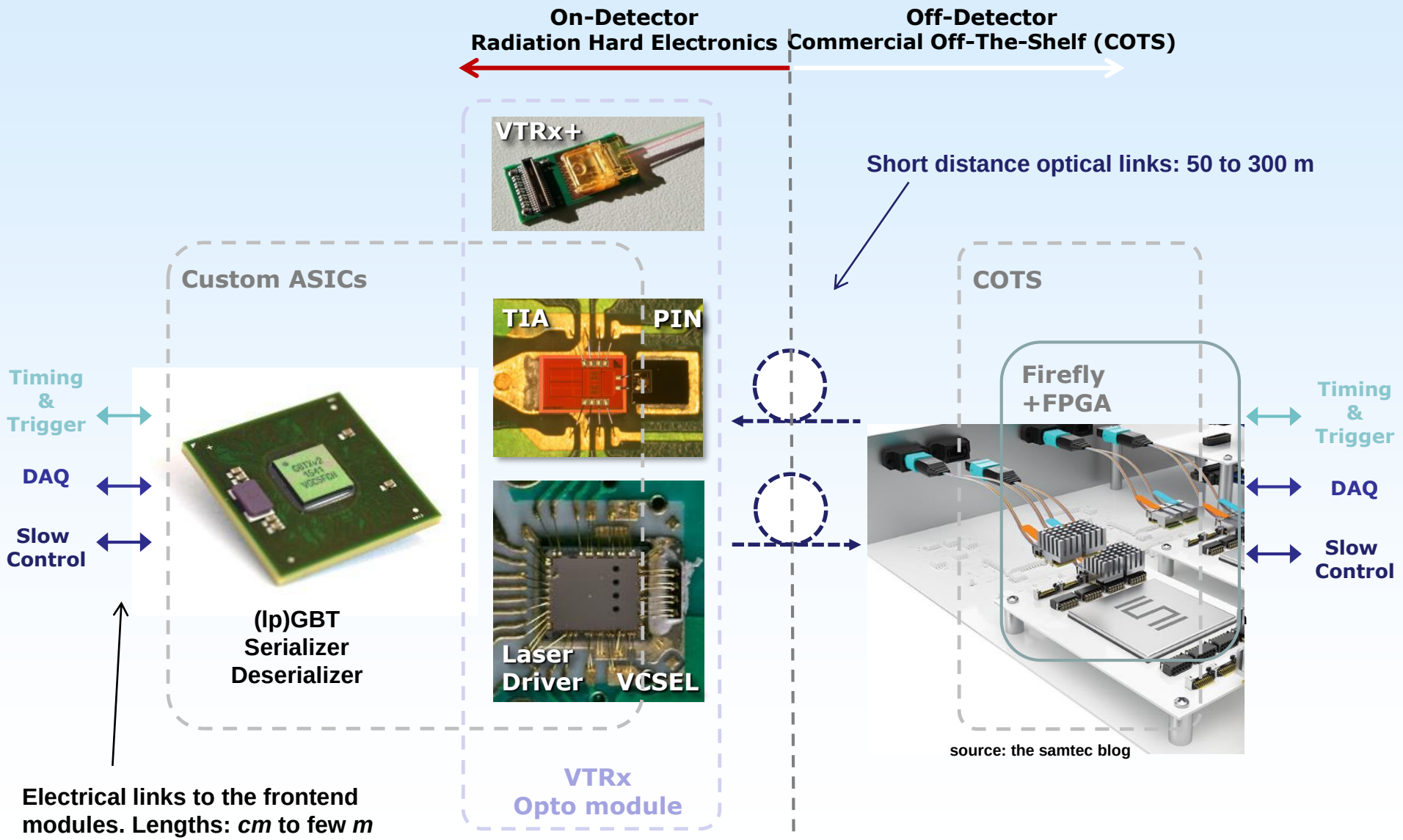


Conclusions

- Optical Links developed for HL-LHC have reached the limits of the used technologies
  - Active optoelectronics not hard enough for pixels and forward calorimeters
- Technology trends point towards
  - Migration to 28 nm CMOS
  - Development of 25 Gb/s links
  - PAM-4 and λ-WDM for more capacity
- Radiation hardness can only be improved by changing technology
  - Silicon Photonics may be the solution
  - Promising results have been reported
  - R&D must be launched now to thoroughly qualify the technology (or not)
  - Hybrid integration with sensor and electronics will come as a bonus

Backups

High Speed Links in HEP

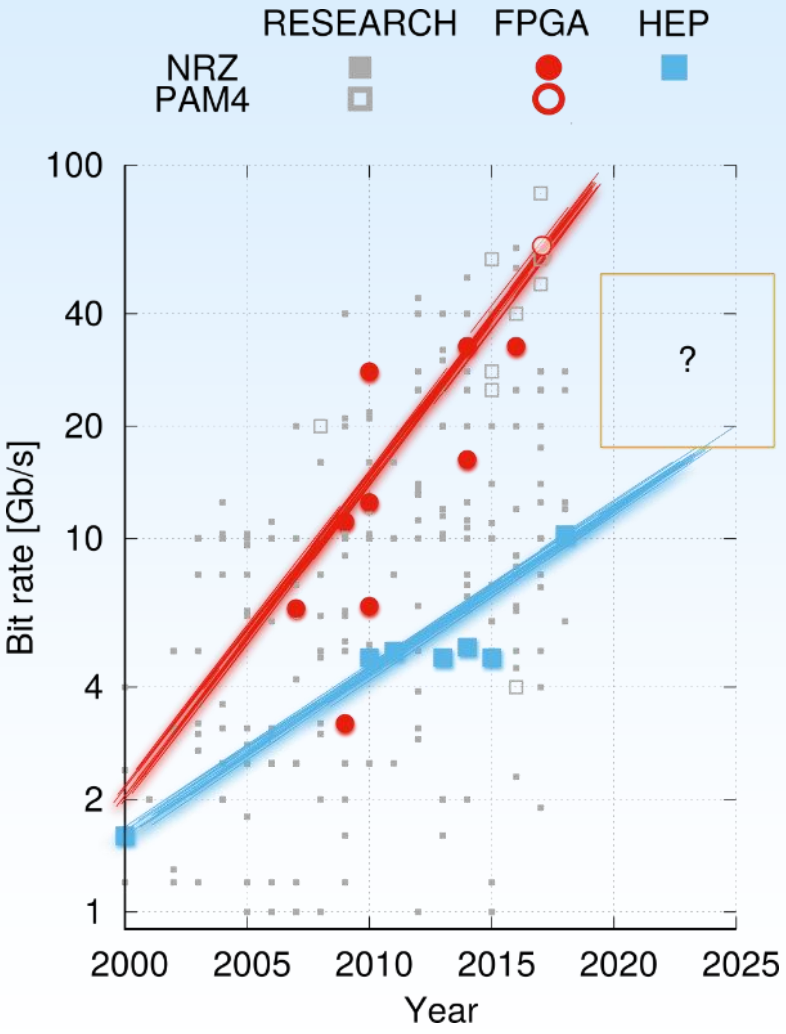


ASICs Technology Trend : Serializer line rate

- **HEP systems are certainly lagging** behind research papers (for which the main aim is to demonstrate peak performance) and commercial systems (FPGAs)

- HEP ASIC **performance** tends to be **limited by**:
  - Long development cycles: **radiation qualification and reduced resources**
  - Use of relatively old technology nodes: **radiation qualification and prototyping cost**
  - Circuit techniques: **increasing radiation tolerance** to TID and SEU

- If a projection can be made in the horizon of 2020 to 2025 the HEP systems **should be targeting 20 - 40 Gb/s systems**:
  - Well within the capability of today's FPGAs



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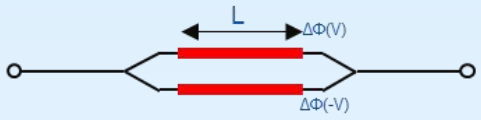
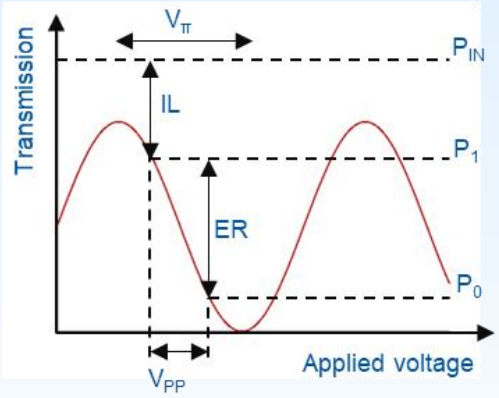
Silicon photonics modulators

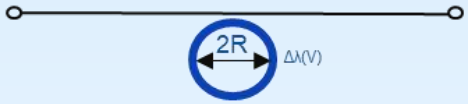
Si Mach Zehnder Modulator

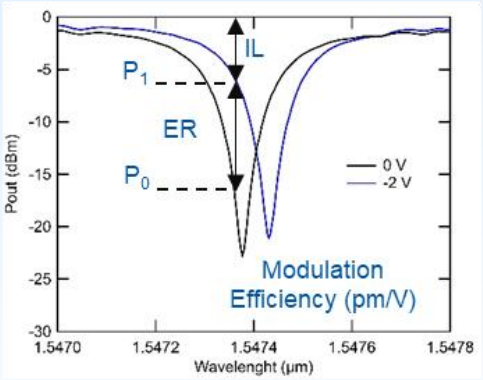




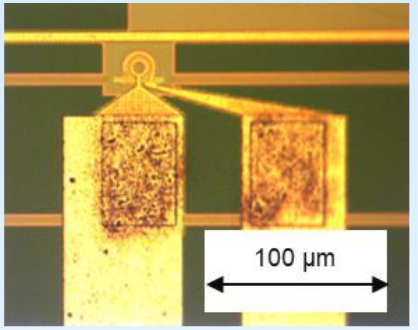
- Optically broadband
- Thermally robust
- Large footprint (L~1mm)
- High driving voltage amplitude

Si Ring Modulator

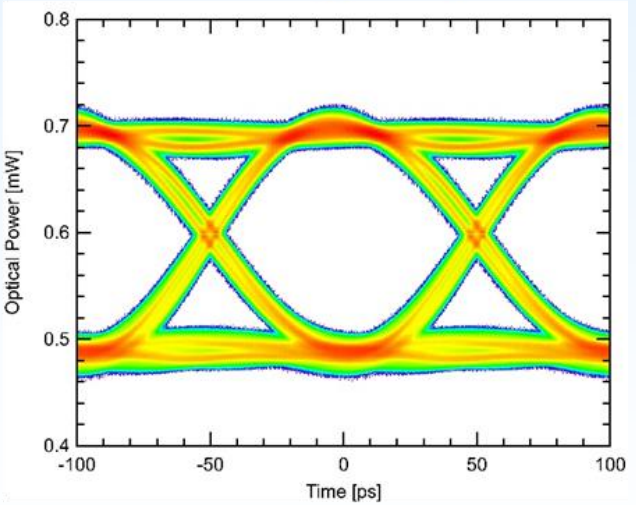




- Optically narrowband (<1nm)
- Thermally sensitive (<1K)
- Small footprint (R~5μm)
- Small driving voltage amplitude (1Vpp)



10 Gb/s eye diagram



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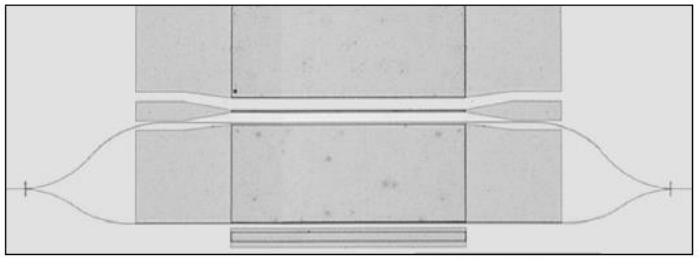
SiPh Modulator Power Efficiency

40 Gbit/s Mach Zehnder modulator



L=1.8mm => C ~0.5 pF

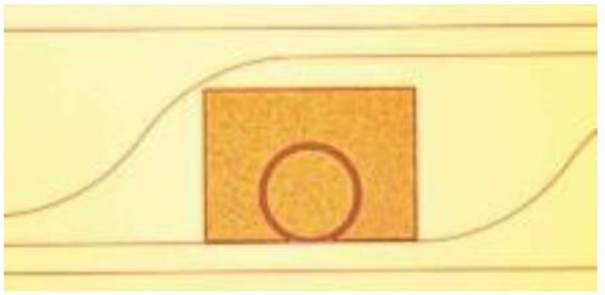
V_{pp} = 7 V

Laser excluded

Energy/bit ~ 6 pJ/bit

1pJ/bit = 1mW/Gbps

10 Gbit/s ring modulator



Ring radius of 50 µm => C ~0.08 pF

Energy/bit ~ 0.7 pJ/bit

Optical wavelength-division multiplexed (WDM) links in internet
- ~ 10 nJ/bit (total) (Tucker, 2008)

Reading from DRAM
- ~ 30 pJ/bit (Dally, 2009)

Communicating a bit off chip
- Several to 10's pJ/bit

Floating point operation (FLOP)
- ~ 1pJ/bit (50 pJ for double precision (64b) operation) (Dally, 2009)

Energy stored in DRAM cell
- ~ 10 fJ

Switching one CMOS gate
- < 1 fJ

(1 electron at 1V, or one photon ~ 0.16 aJ)

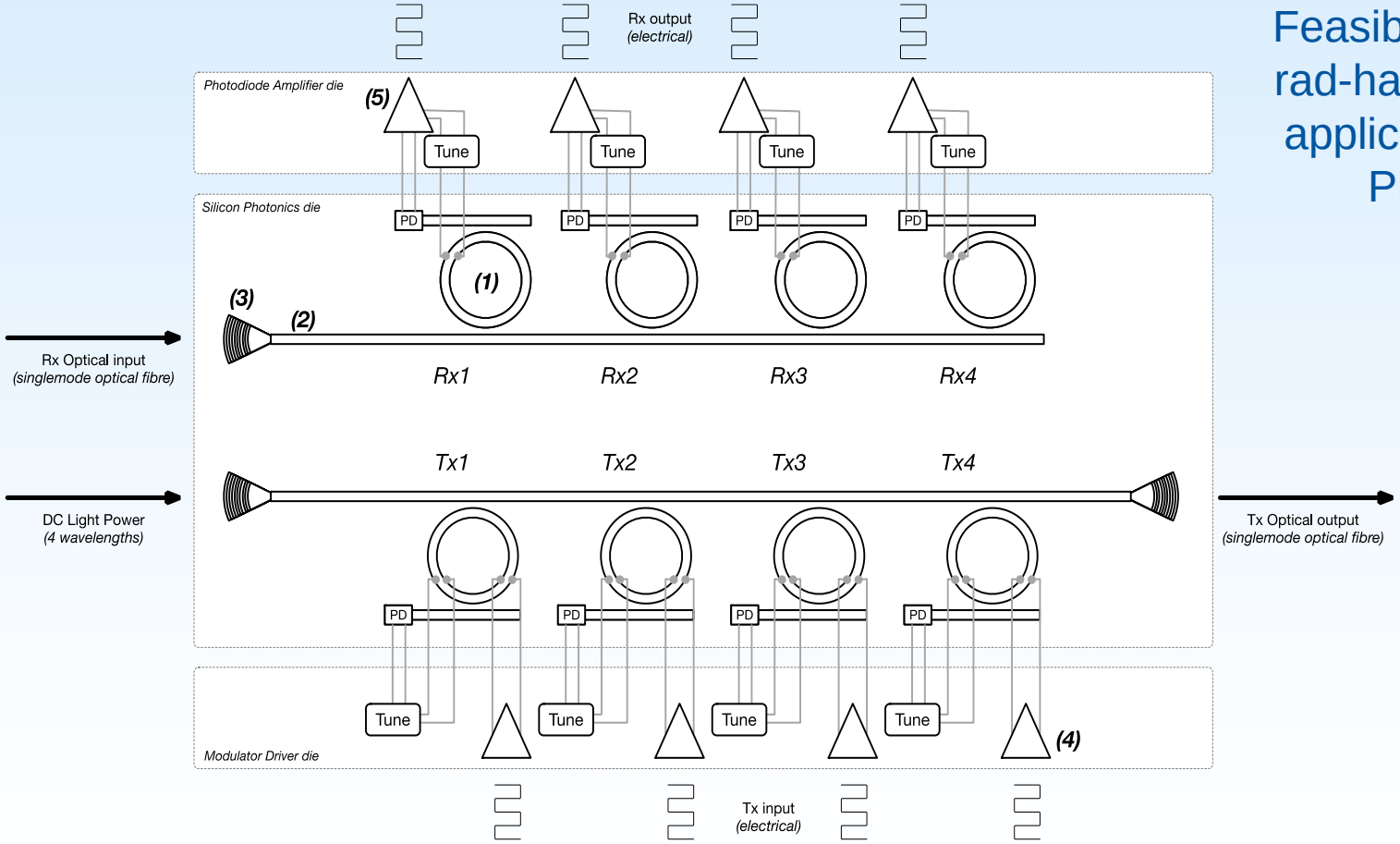
(one google search ~1kJ)

W. Dally, "Power Efficient Supercomputing," talk at ACS, 2009
R. S. Tucker, "Energy and the Internet," OECC '08, Sydney, Australia, July 2008; also J. Baliga, K. Hinton, and R. S. Tucker, "Energy Consumption of the Internet," Optical Internet, 2007 and the 2007 32nd Australian Conference on Optical Fibre Technology. COIN-ACOFT 2007. Joint International Conference on 24-27 June 2007, Page(s):1 – 3; K. Hinton et al., "Power Consumption and Energy Efficiency in the Internet," IEEE Network 25, 2, SI pp6-12 (Mar. Apr. 2011)

A Silicon Photonics Vision

ATTRACT SiPhoSpace

Feasibility study of a 100 Gb/s rad-hard transceiver for space applications based on Silicon Photonics micro-ring



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