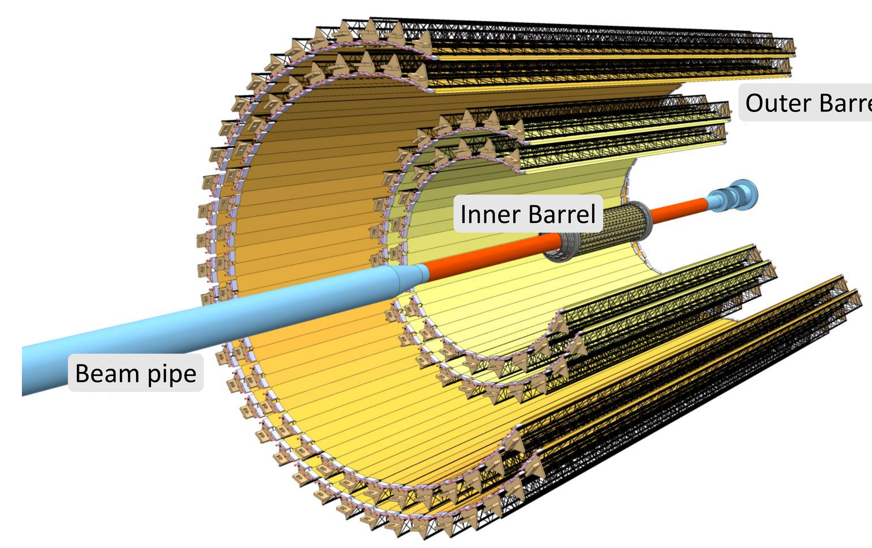
Ageing tests of the Hybrid Modules for the ALICE ITS Upgrade

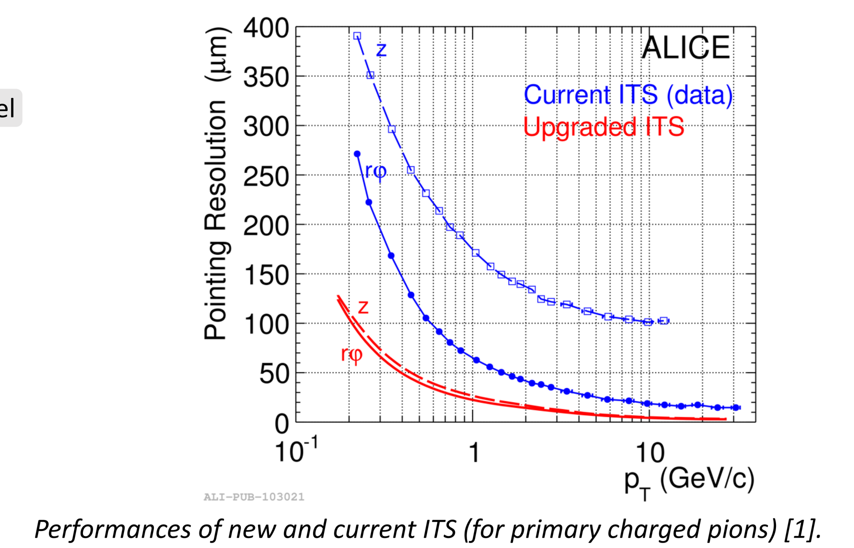
Nicolò Valle[1], for the ALICE Collaboration

[1]University and INFN, Pavia, Italy

UPGRADE OF THE ALICE INNER TRACKING SYSTEM

A key element of the ongoing ALICE experiment upgrade is the replacement of the Inner Tracking System (ITS) with a newly constructed silicon based detector. The new ALPIDE chips have already shown excellent performances in terms of power consumption ($39\ \mathrm{mW/cm^2}$) and spatial precision ($\sim 5\ \mu\mathrm{m}$). Once installed they will allow a remarkable improvement of the tracking and vertexing capabilities (see figure on the right). This will be possible thanks to the reduced material budget (0.35% x/X_0 in the innermost layers), the reduced pixel size ($29\mu\mathrm{m} \times 27\mu\mathrm{m}$), the increased number of layers and the reduced distance between the first layer and the interaction point (22 mm) [2].





Performances of new and current ITS (for primary charged pions) [1].

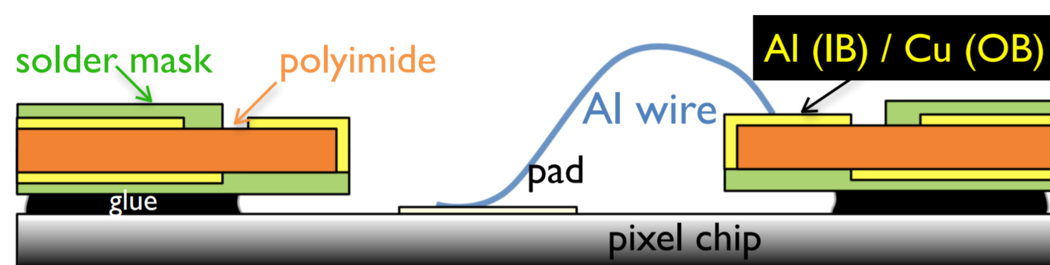
HYBRID INTEGRATED CIRCUIT (HIC) MODULES ASSEMBLY

✓ Pixel Chip (ALPIDE, ALICE PIxel DEtector), based on the TowerJazz 180 nm CMOS imaging process. A single chip contains half a million MAPS pixels (Monolithic Active Pixel Sensors, 50 μm or 100 μm thick for Inner and Outer Barrel, respectively).

✓ Polymide Flexible Printed Circuits (FPCs), with aluminium or copper as conductor for Inner Barrel and Outer Barrel HICs, respectively.

→ The chips are aligned (with < 5 μm precision) and glued onto FPCs.

→ The pads of the chips are then connected to the FPC for power supply and I/O with aluminium wire bonding. Three redundant connections are soldered on each pad.



OUTER BARREL HIC AGEING TESTS

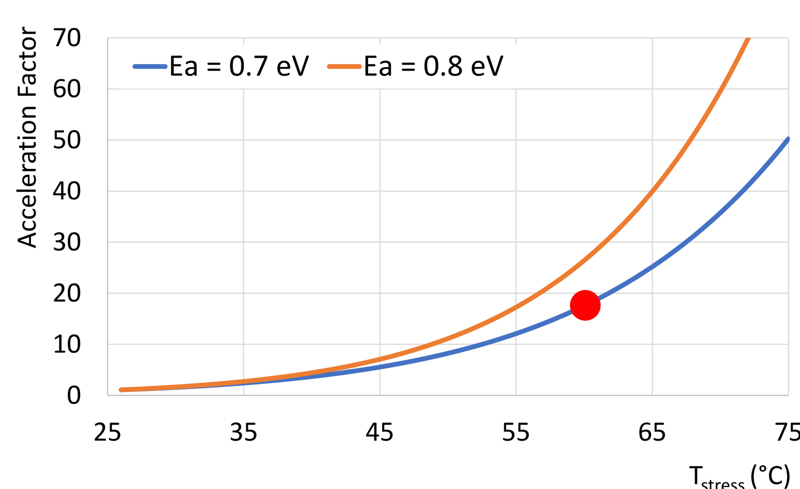
A sub-sample of HICs were kept in a temperature- and humidity-controlled environment in order to simulate their ageing in the ALICE cavern.

The Arrhenius relationship can be used to describe the effects of the temperature (and other factors, such as relative humidity RH) on the rate R of oxidation reactions [3]:

$$R = \gamma \exp(-E_a/kT)\ \exp\big(\,f(RH, E_a, T)\big)$$

where E_a is the activation energy. The acceleration factor (AF) induced by a temperature T_{stress} is:

$$AF = R(T_{stress})/R(T) = \exp\left[\frac{E_a}{k}\left(\frac{1}{T} - \frac{1}{T_{stress}}\right)\right]$$



● Working point chosen fot the test:

$$T_{stress} = 60\ °\mathrm{C}$$
$$RH = 15\%$$

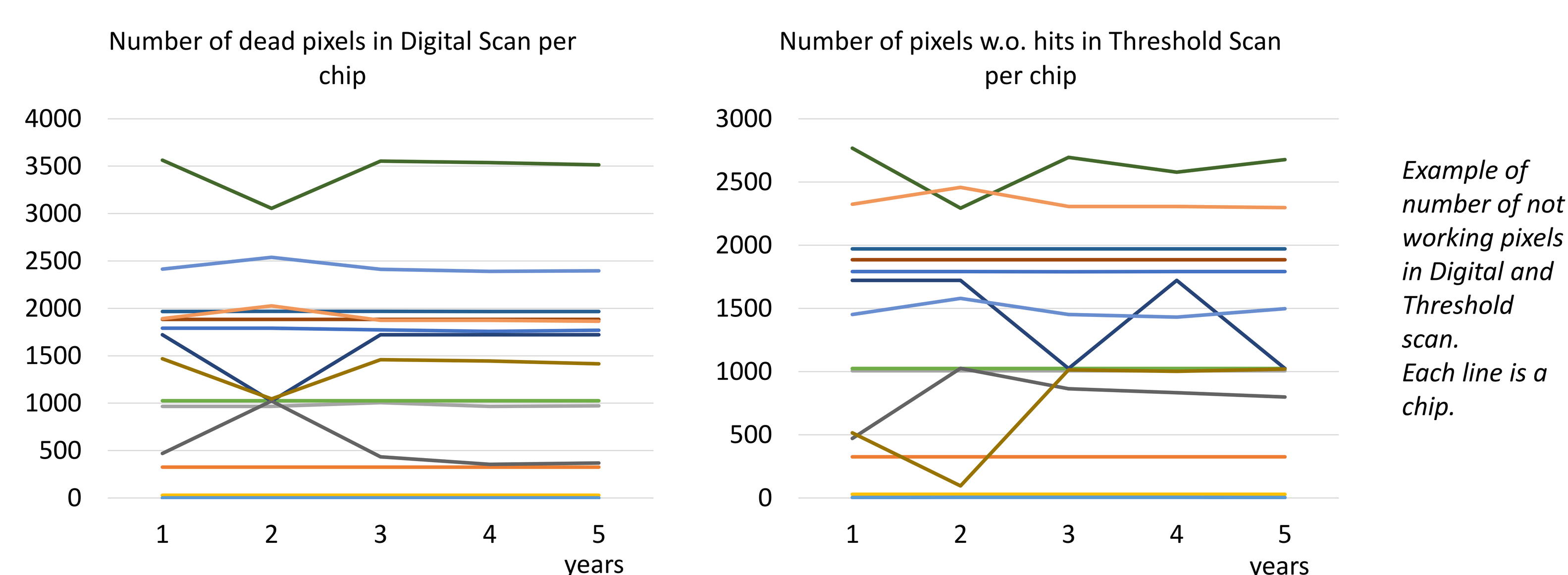
→ Keeping the HIC in a climate chamber at these conditions for 30 days, a period of one year of real operation can be simulated.

→ HICs were tested over a period of 5 equivalent years of ageing.

After each one-year equivalent cycle the HICs were tested, both mechanically (**pull-test**) and electrically (**qualification test**).

RESULTS OF THE QUALIFICATION TEST

The comparison of the HIC performances before and after each cycle was done on both the entire HIC and the single chips. The number of bad pixels in digital scan or threshold scan and the pixel noise are the parameters of interest which were measured.

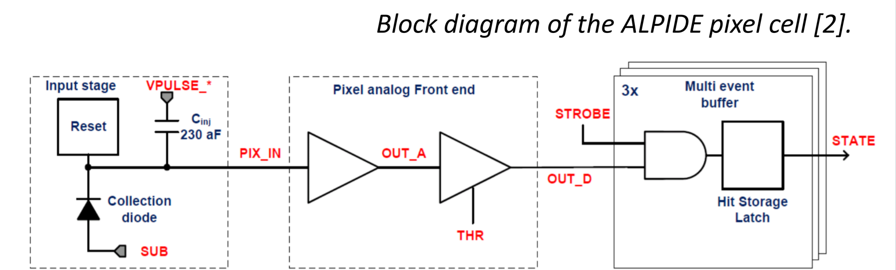


Example of number of not working pixels in Digital and Threshold scan. Each line is a chip.

The results didn't show any systematic effect due to ageing. The number of working pixels as well as the noisy pixels and threshold values showed a good stability over time.

OUTER BARREL HIC QUALIFICATION

Electrical and Performance Tests



Block diagram of the ALPIDE pixel cell [2].

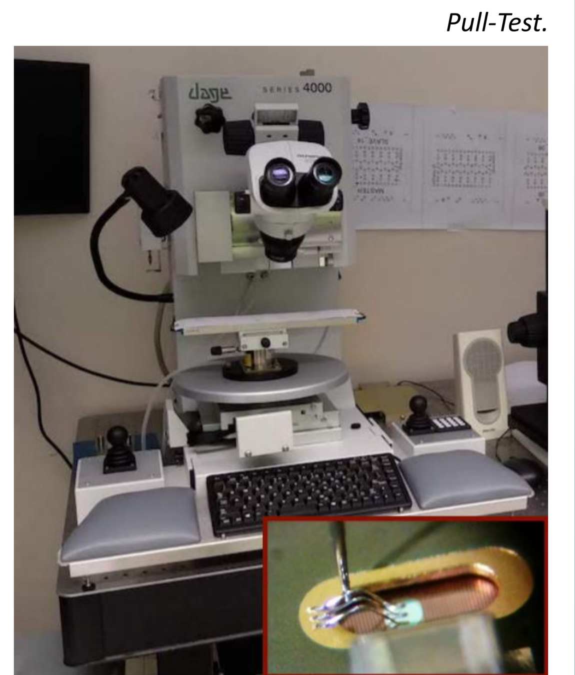
In the **Qualification Test** a series of scans are performed and cuts to different parameters applied in order to classify the HIC.

- In the **Digital Scan** digital pulses are injected into the digital logic of the pixel cells. They are then read out and the number of pixels not registering hits is measured.
- In the **Threshold Scan** a charge is induced in the front-end circuit of the chips. By sweeping over the induced charge, the charge threshold and noise is determined.

Mechanical Tests

Some HICs undergo more destructive tests designed to check their mechanical strength (e.g. the strength of the soldering or the chip-FPC glue adhesion).

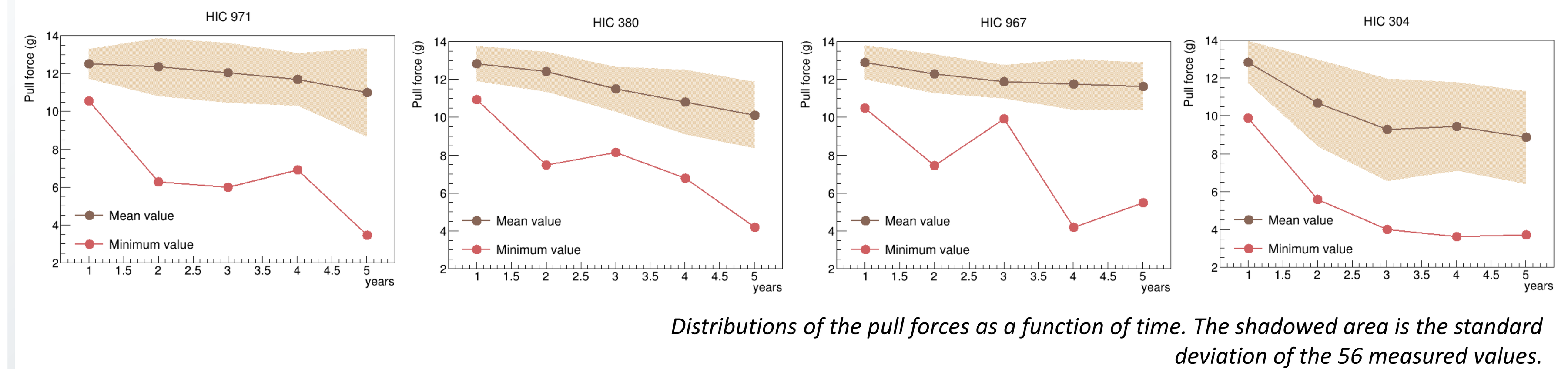
- **Pull-Test**: the wired bonds are pulled out for a selected number of pads on the HIC. The distribution of the breaking force is measured.



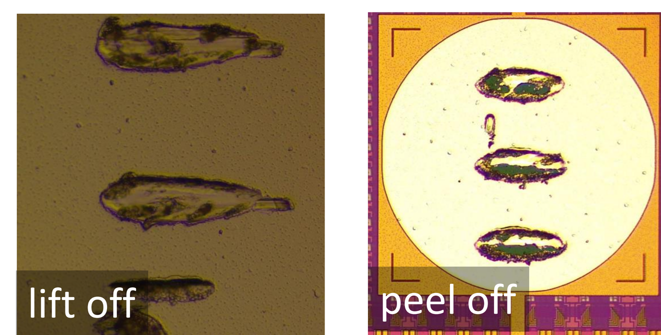
Pull-Test.

RESULTS OF THE PULL-TEST

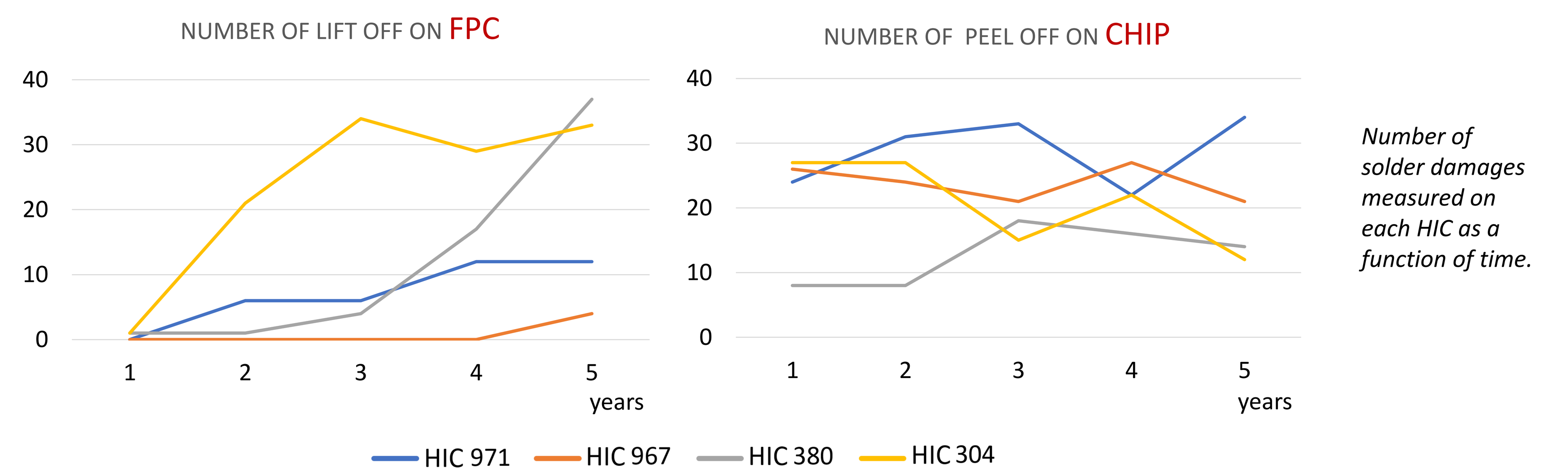
After each ageing cycle some wired bonds were pulled out on each chip (56 connections per HIC) and the distributions of the pull forces were compared to those obtained before the cycle.



Distributions of the pull forces as a function of time. The shadowed area is the standard deviation of the 56 measured values.



The bonding damages are quantified by the number of peel-off and lift-off events (detachment of the solder with or without removal of the metallization).



Number of solder damages measured on each HIC as a function of time.

CONCLUSIONS

✓ The electrical tests demonstrated no difference in the performances of the pixels after each cycle.

✓ A worsening of the soldering strength is expected and a decrease in the mean value of the pull force was measured. The deterioration of the soldering in the copper FPC is more evident than the one on the chip pads. However, the average value (> 10 gr) and the minimum value (> 4 gr) after 5 years, combined with the three-bond connections per pad, make the system realiable.

✓ The results of the ageing tests verified the assembly procedure and validated the use of the appropriate components.

[1] B. Abelev et al. (ALICE Collaboration). Technical Design Report for the Upgrade of the ALICE Inner Tracking System. *J. Phys.G 41 (2014) 087002*

[2] G. Aglieri Rinella, on behalf of the ALICE Collaboration. The ALPIDE pixel sensor chip for the upgrade of the ALICE Inner Tracking System. *Nuclear Inst. and Methods in Physics Research, 2017*

[3] L. A. Escobar, W. Q. Meeker. A Review of Accelerated Test Models. *Statist. Sci. 21, 4 (2006)*

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