ALICE

CERN

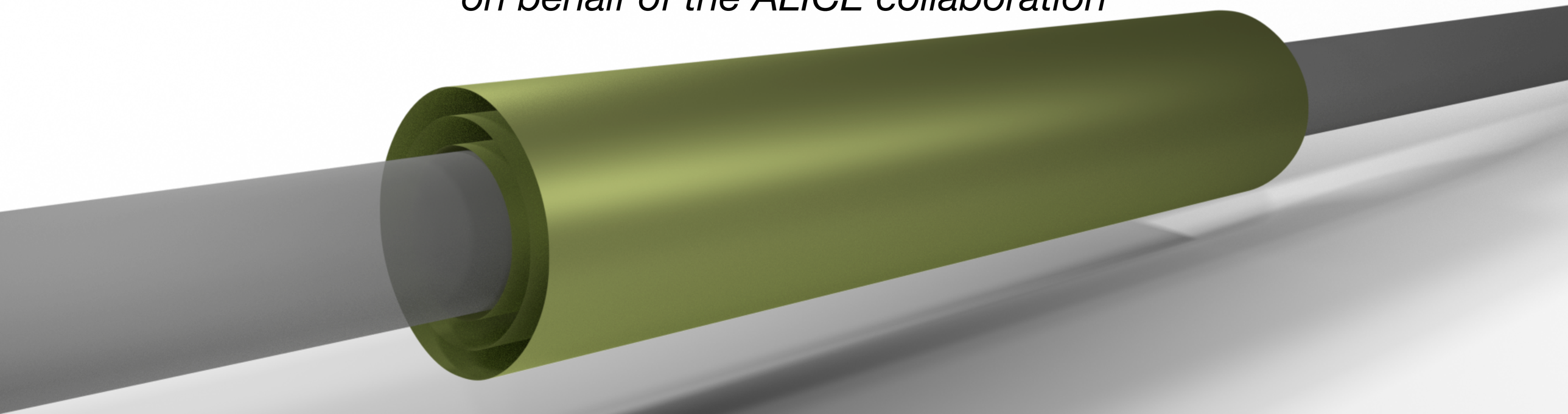
VERTEX 2019

LOPUD ISLAND, CROATIA OCTOBER 13-18, 2019

Upgrade of the ALICE ITS in LS3

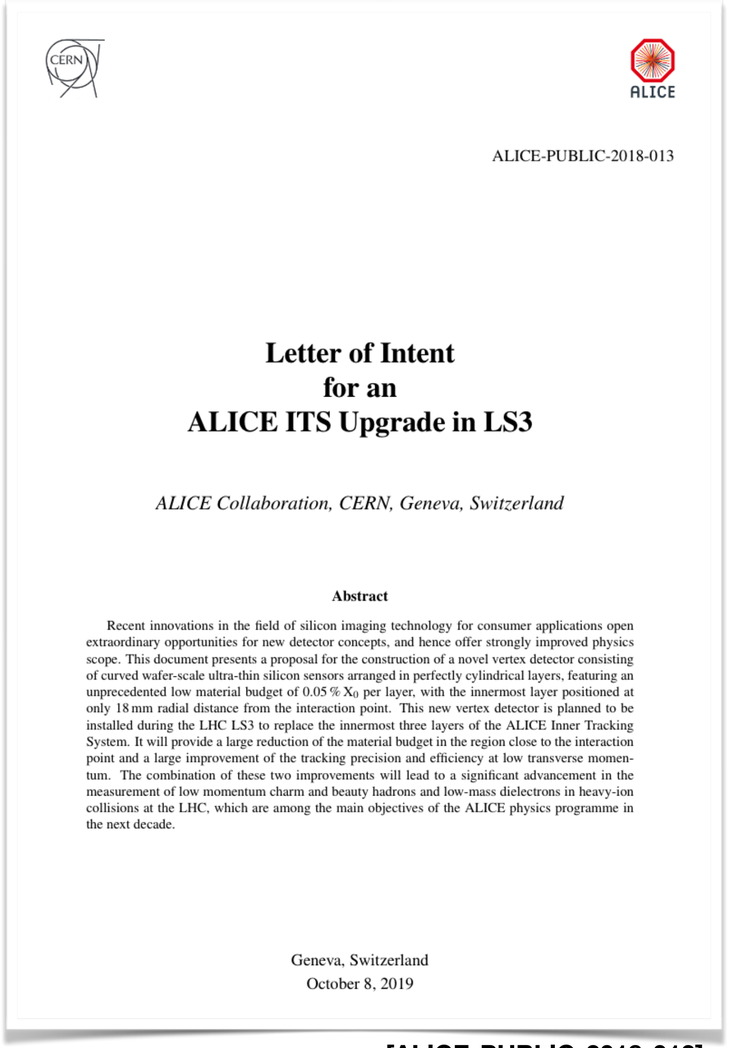
Magnus Mager (CERN)

on behalf of the ALICE collaboration



Contents

- ALICE ITS2 + motivation to go further
- R&D topics:
  - Wafer scale chip (300 mm, 65 nm)
  - Thinning/bending
  - Cooling
- Layout and integration
- Performance projections
  - tracking performance
  - physics projections
- R&D + Construction Timeline



ALICE-PUBLIC-2018-013

Letter of Intent for an ALICE ITS Upgrade in LS3

ALICE Collaboration, CERN, Geneva, Switzerland

Abstract

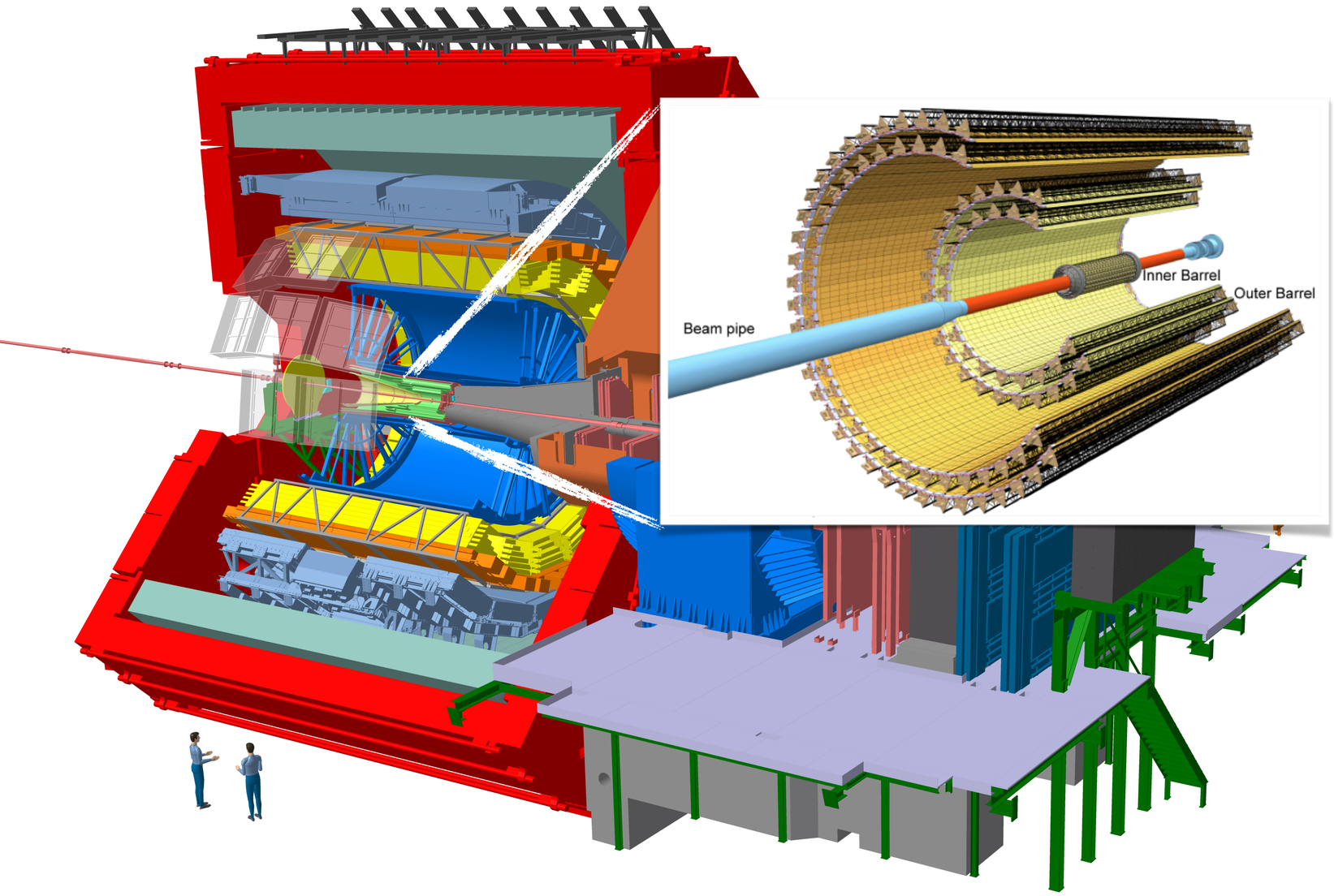
Recent innovations in the field of silicon imaging technology for consumer applications open extraordinary opportunities for new detector concepts, and hence offer strongly improved physics scope. This document presents a proposal for the construction of a novel vertex detector consisting of curved wafer-scale ultra-thin silicon sensors arranged in perfectly cylindrical layers, featuring an unprecedented low material budget of 0.05 % X_0 per layer, with the innermost layer positioned at only 18 mm radial distance from the interaction point. This new vertex detector is planned to be installed during the LHC LS3 to replace the innermost three layers of the ALICE Inner Tracking System. It will provide a large reduction of the material budget in the region close to the interaction point and a large improvement of the tracking precision and efficiency at low transverse momentum. The combination of these two improvements will lead to a significant advancement in the measurement of low momentum charm and beauty hadrons and low-mass dielectrons in heavy-ion collisions at the LHC, which are among the main objectives of the ALICE physics programme in the next decade.

Geneva, Switzerland
October 8, 2019

[ALICE-PUBLIC-2018-013]

- ALICE ITS2 + motivation to go further

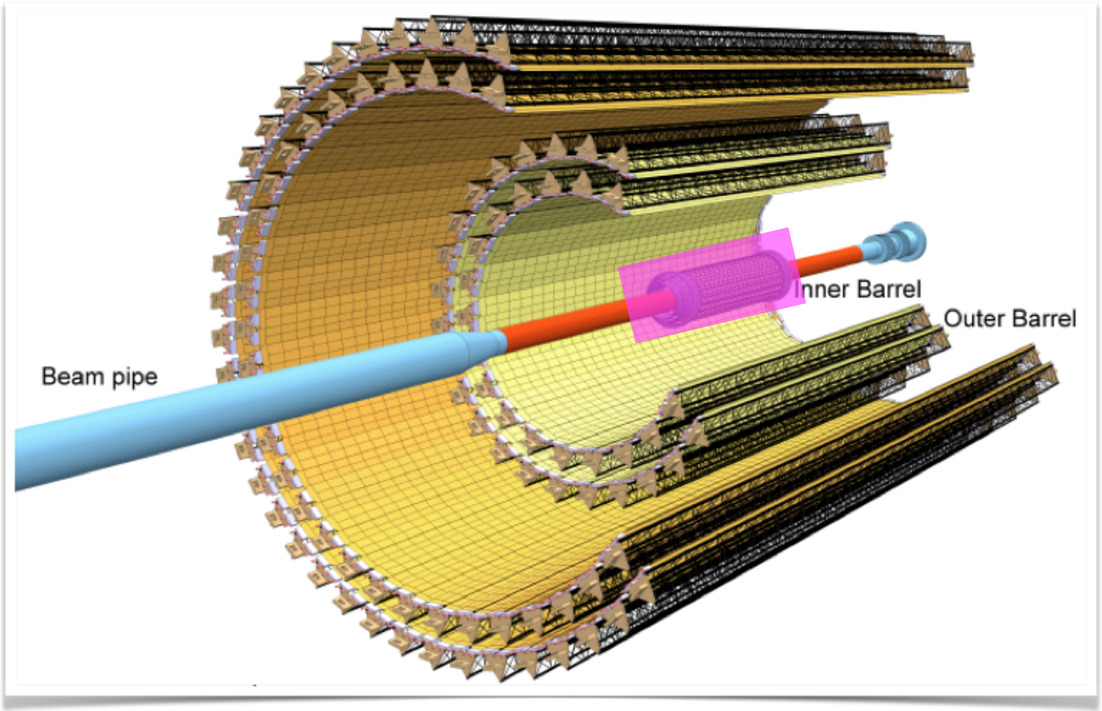
ALICE in Run3 (LS2-LS3)



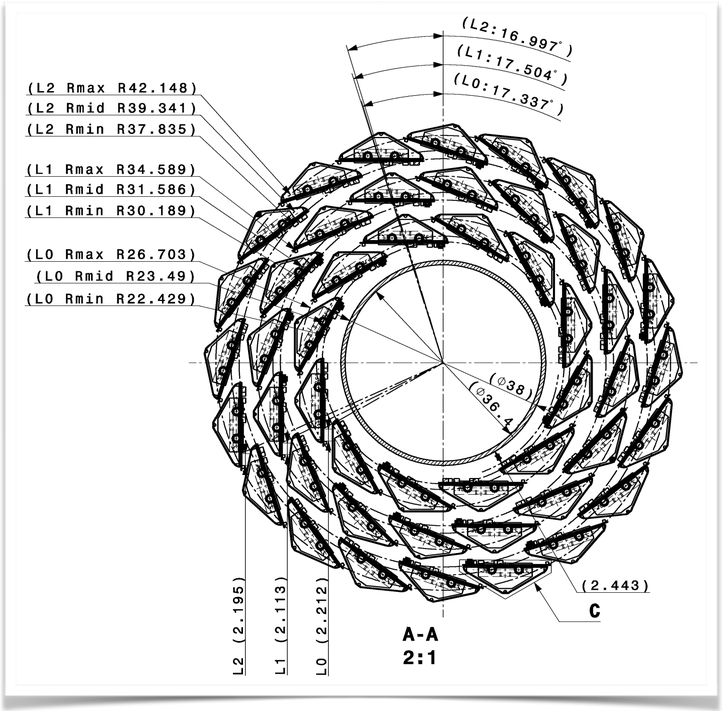
- ALICE had a very successful ITS in Run1+Run2, see:
  - E. Botta: “ALICE ITS: Operational Experience, Performance and Lessons Learned” (Monday)
- ALICE will get a novel MAPS-based ITS2 in LS2 (i.e. right now), see:
  - G. Contin: *“The MAPS-based ITS Upgrade for ALICE”* (Monday)
  - P. Giubilato: *“The ALICE ITS Upgrade Readout and Power System”* (1h ago)
  - V. Raskina: *“Radiation Hardness Studies of ALPIDE, the CMOS sensor for the ALICE ITS Upgrade”* (poster)
  - N. Valle: *“Ageing tests of the Hybrid Modules for the ALICE ITS Upgrade”* (poster)
  - M.D. Buckland: *“Series Production and Test of Hybrid Modules for the ALICE ITS Upgrade”* (poster)
  - T. Lazavera: *“Assembly and Commissioning of the ALICE ITS Upgrade”* (poster)
- ***This* upgrade aims at replacing the inner-most part of ITS2 with an even better detector**

ALICE ITS upgrade (“ITS2”)

ITS2 layout



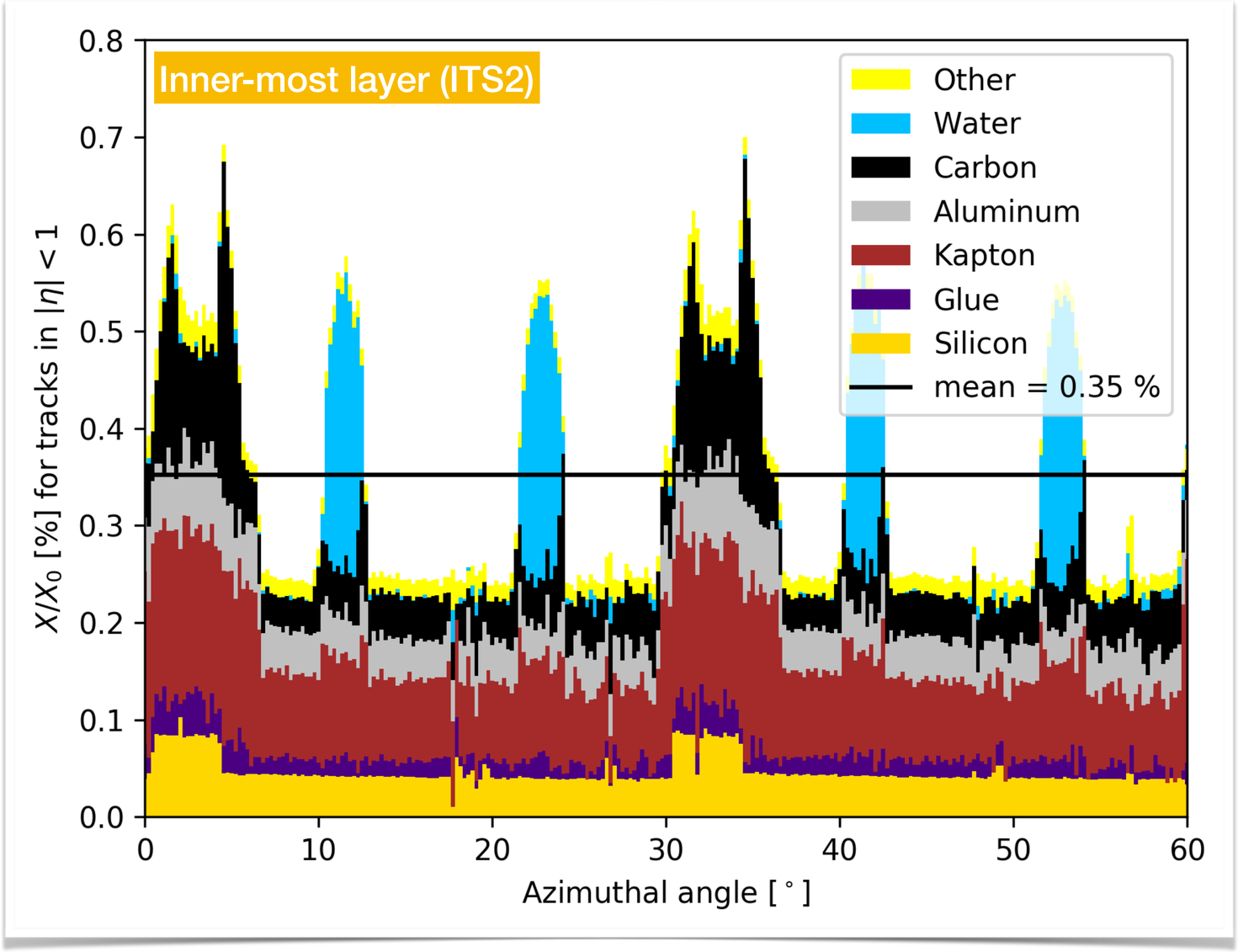
Inner barrel



Layer 2 (20 staves)

- ITS2 will already have unprecedented performance
- Still, further improvements that directly impact the ALICE physics yields are possible
- **Key questions: Can we get closer to the IP? Can we reduce the material?**

Material budget



[ALICE-PUBLIC-2018-013]

- Observations:
  - Si makes only **1/7th** of total material
  - **irregularities** due to support/ cooling

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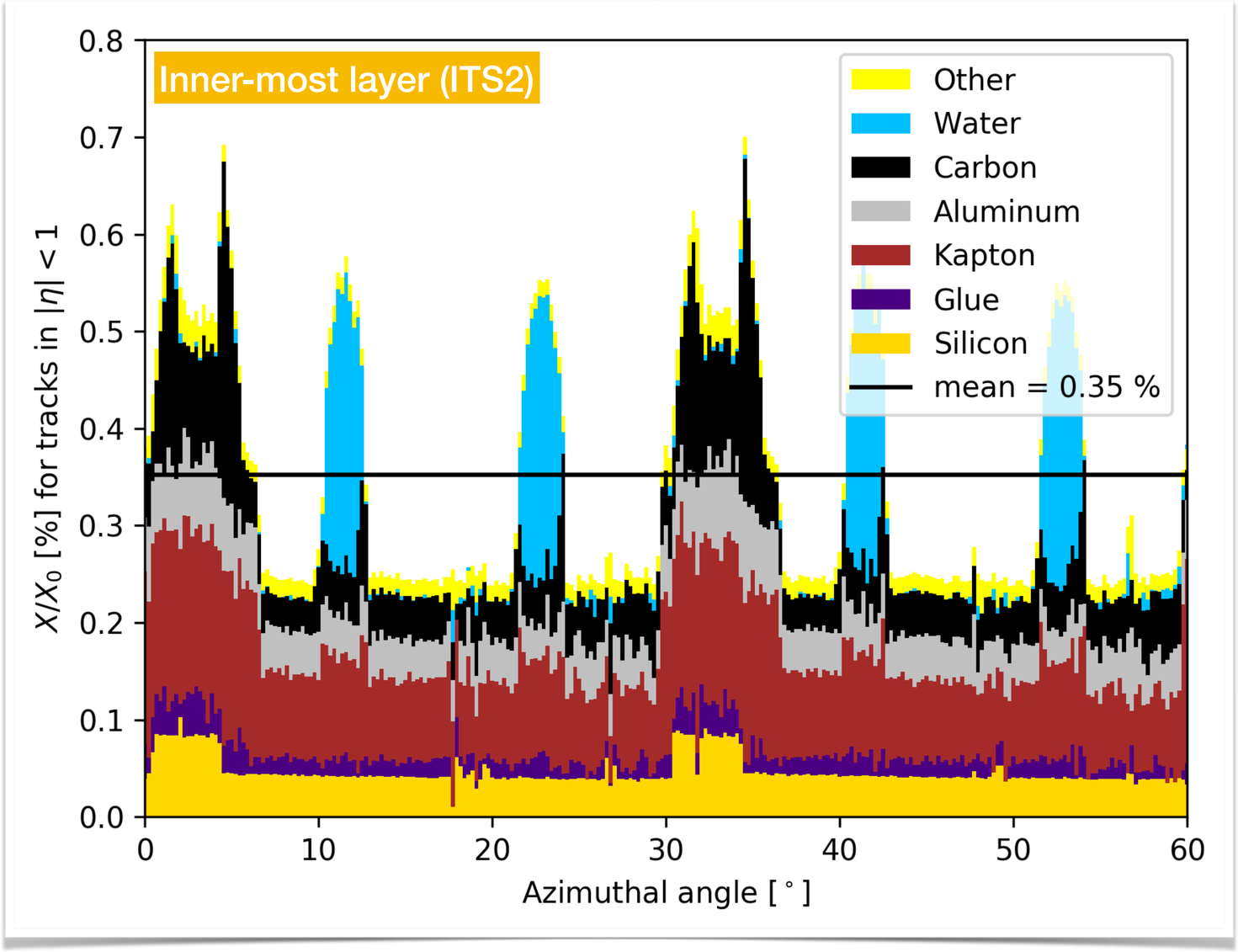

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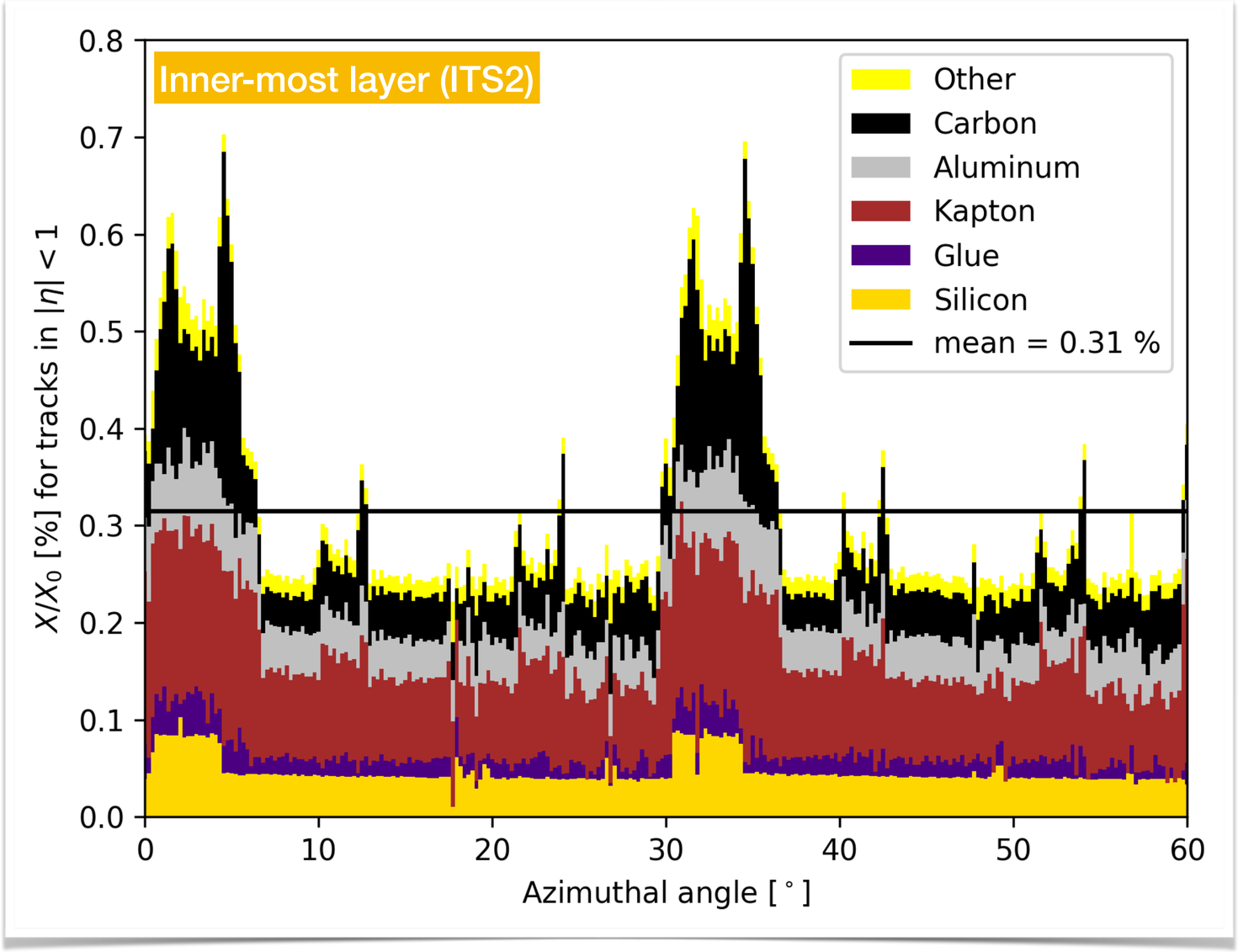

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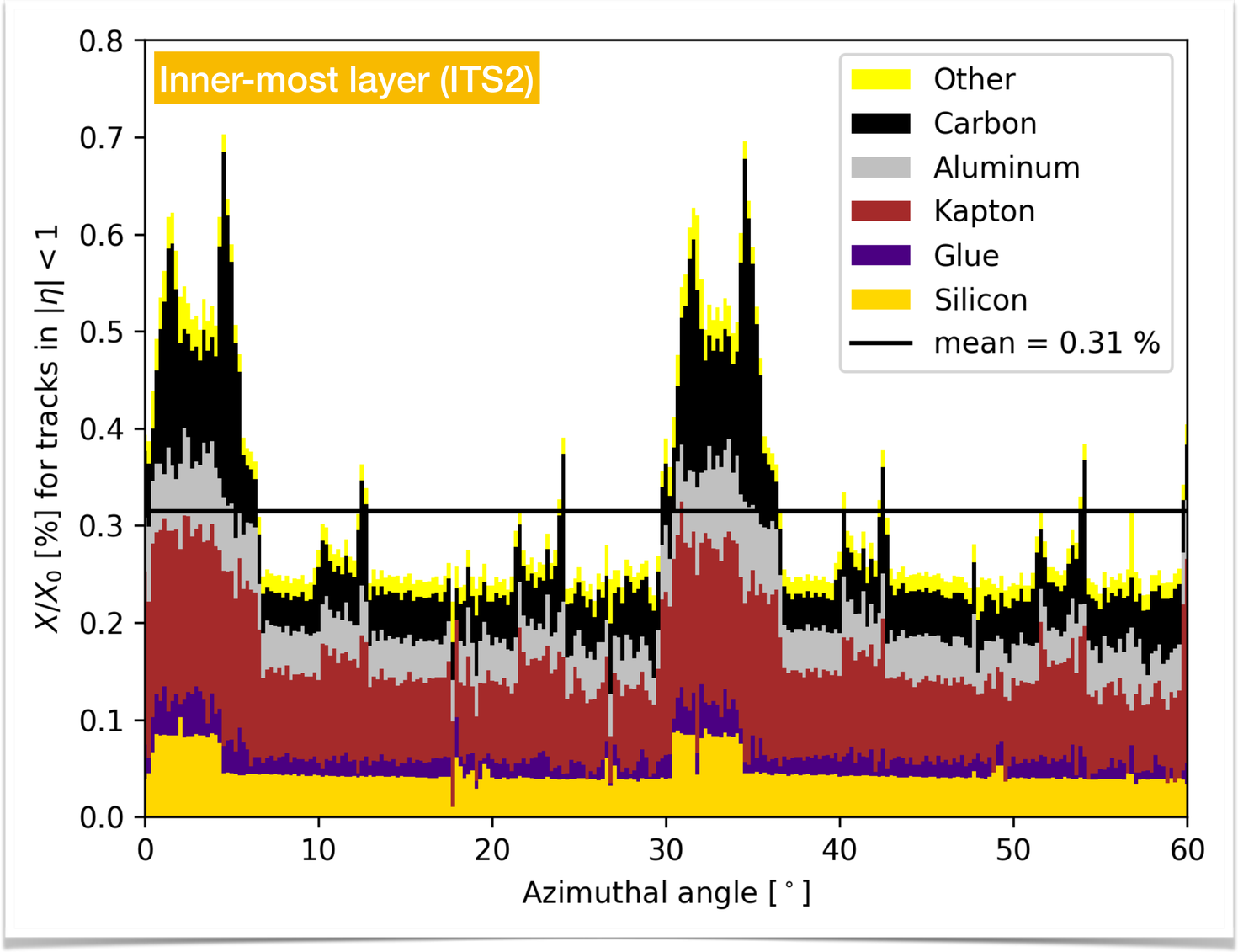

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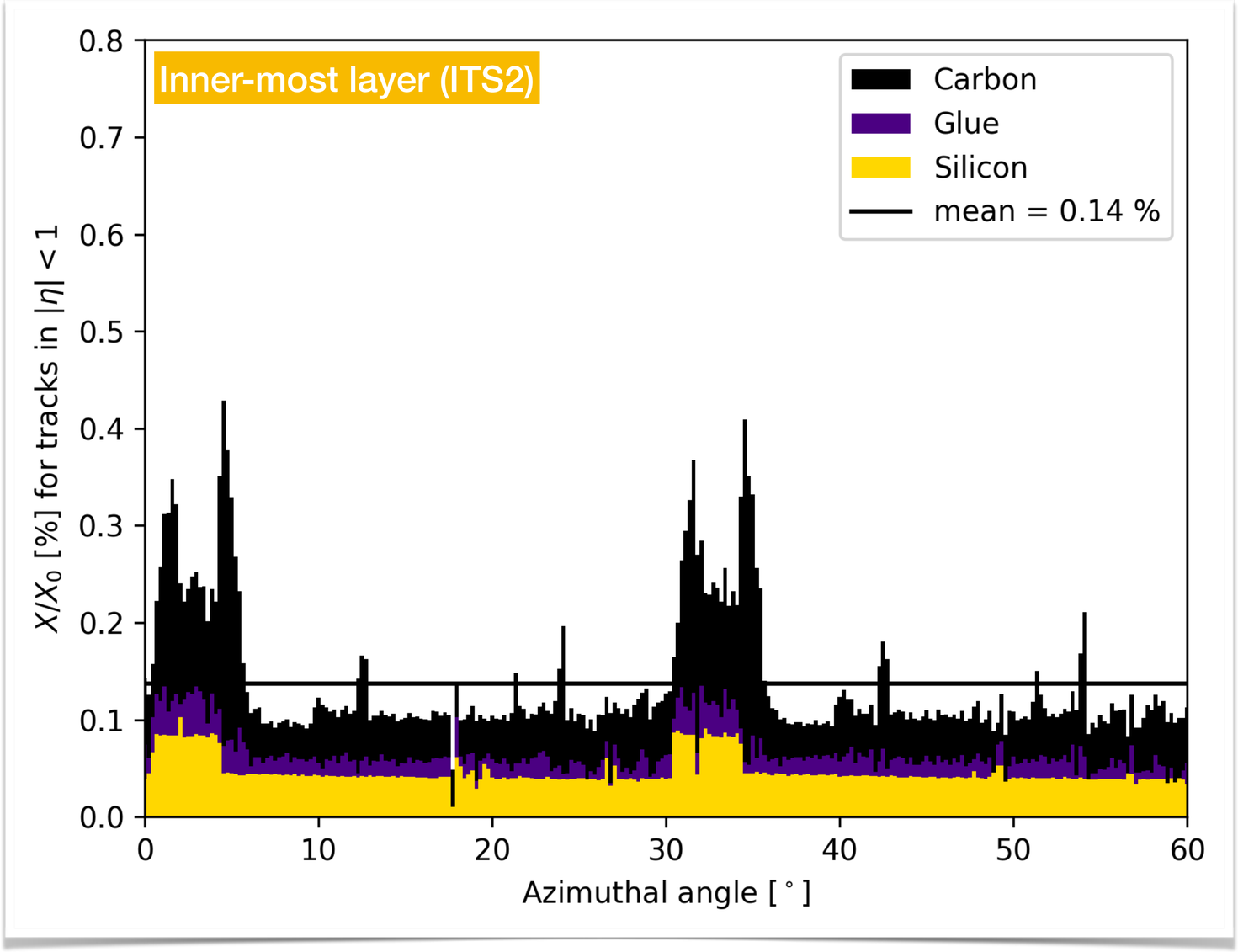

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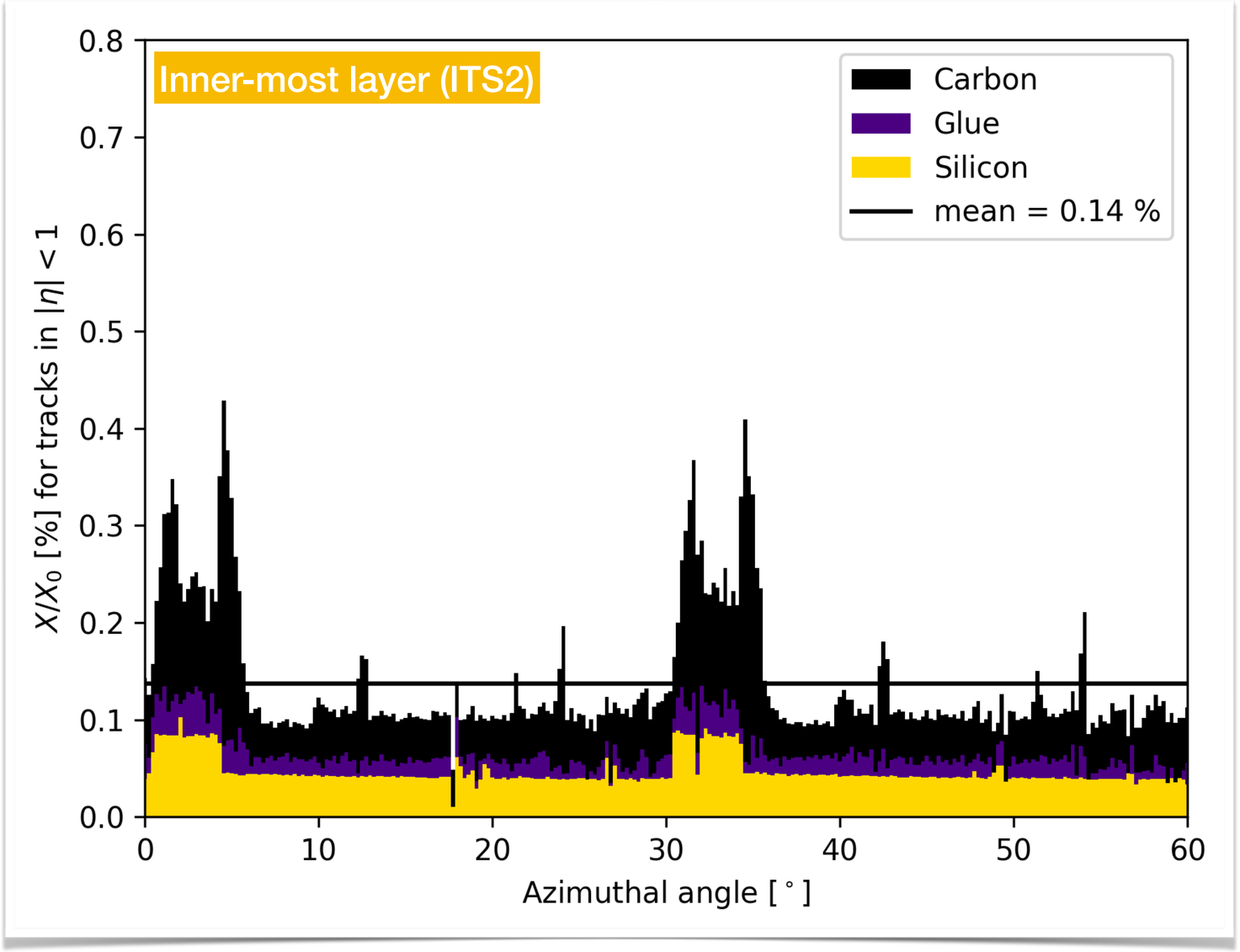

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  - **benefit** from increased stiffness by rolling Si wafers

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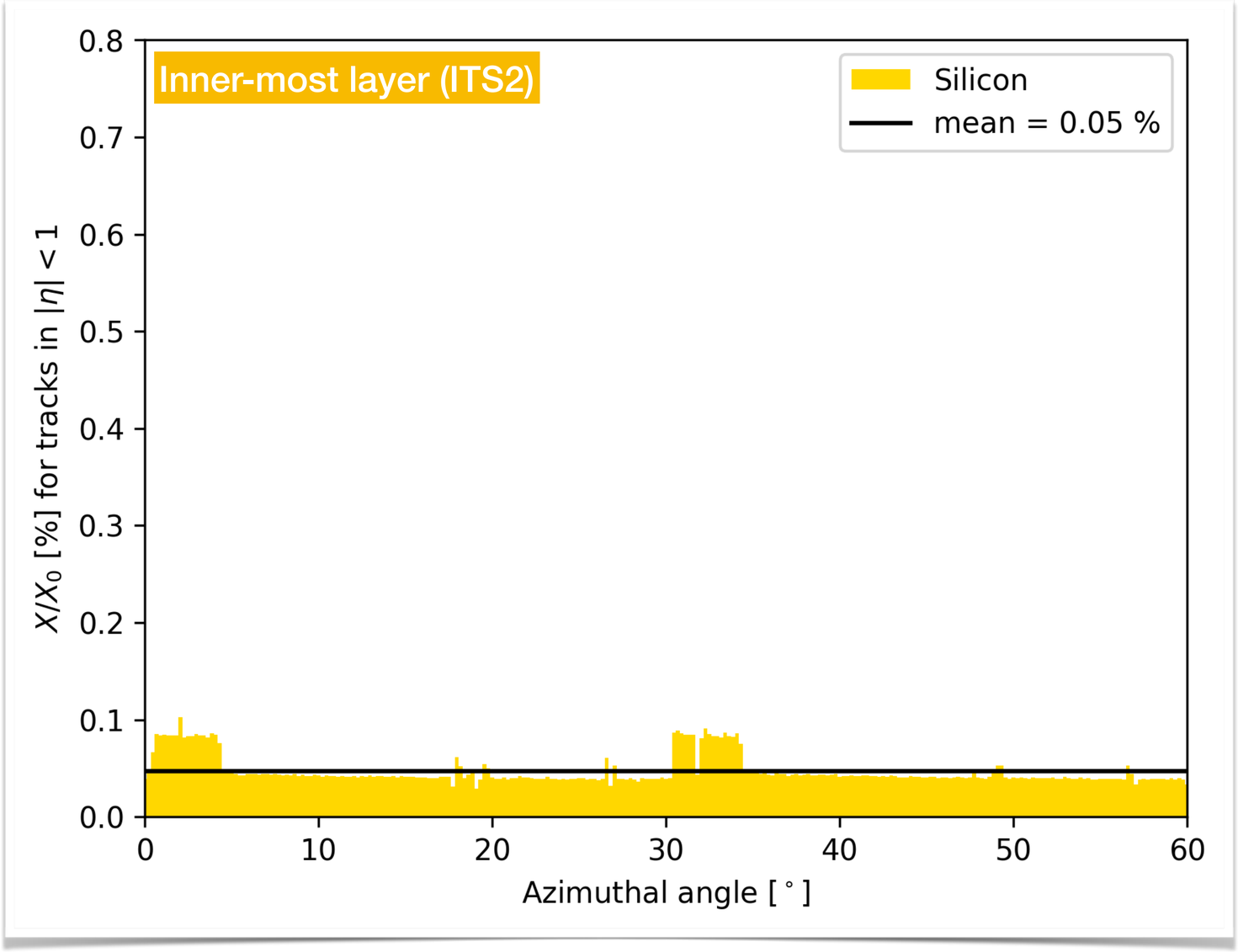

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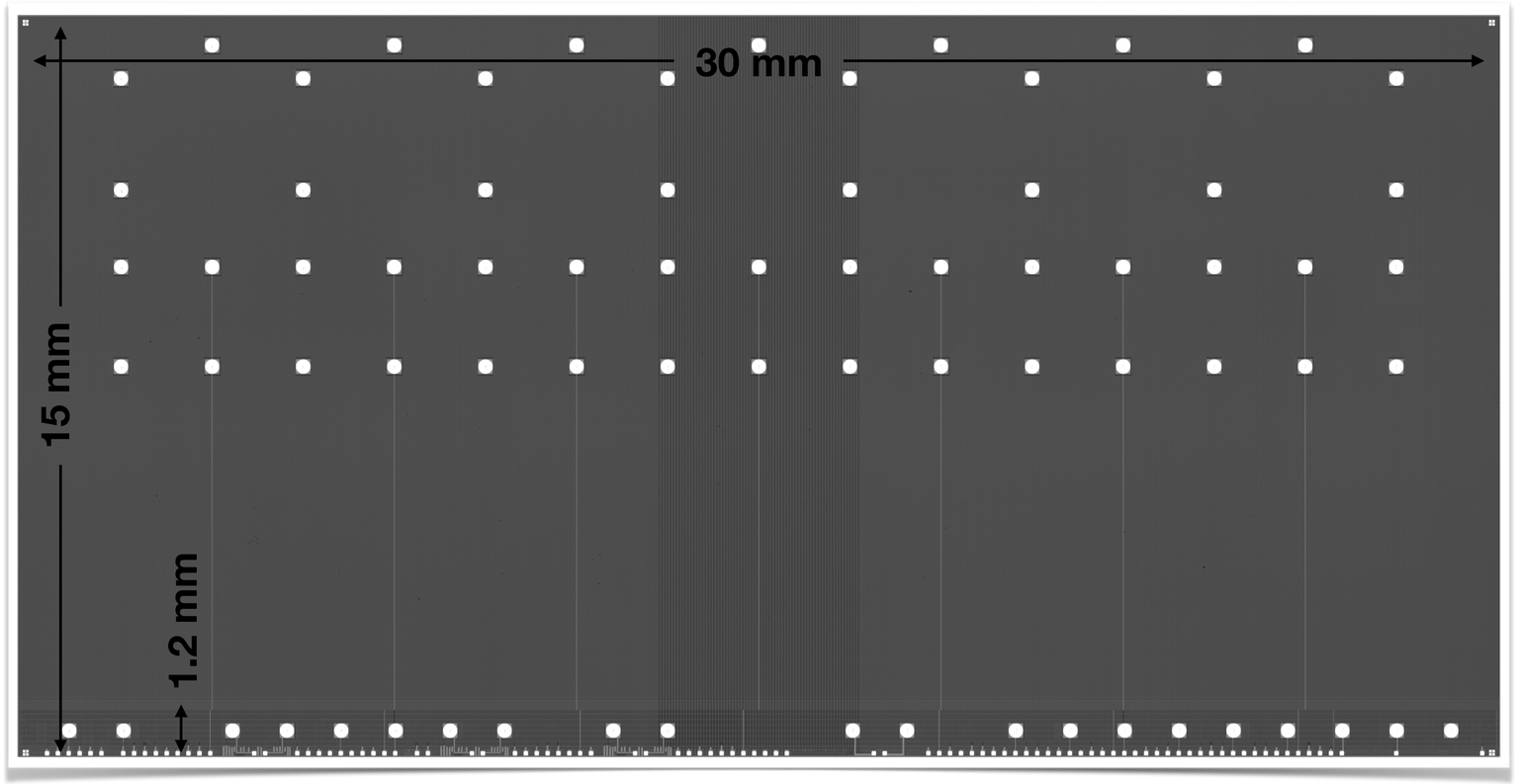
R&D topics

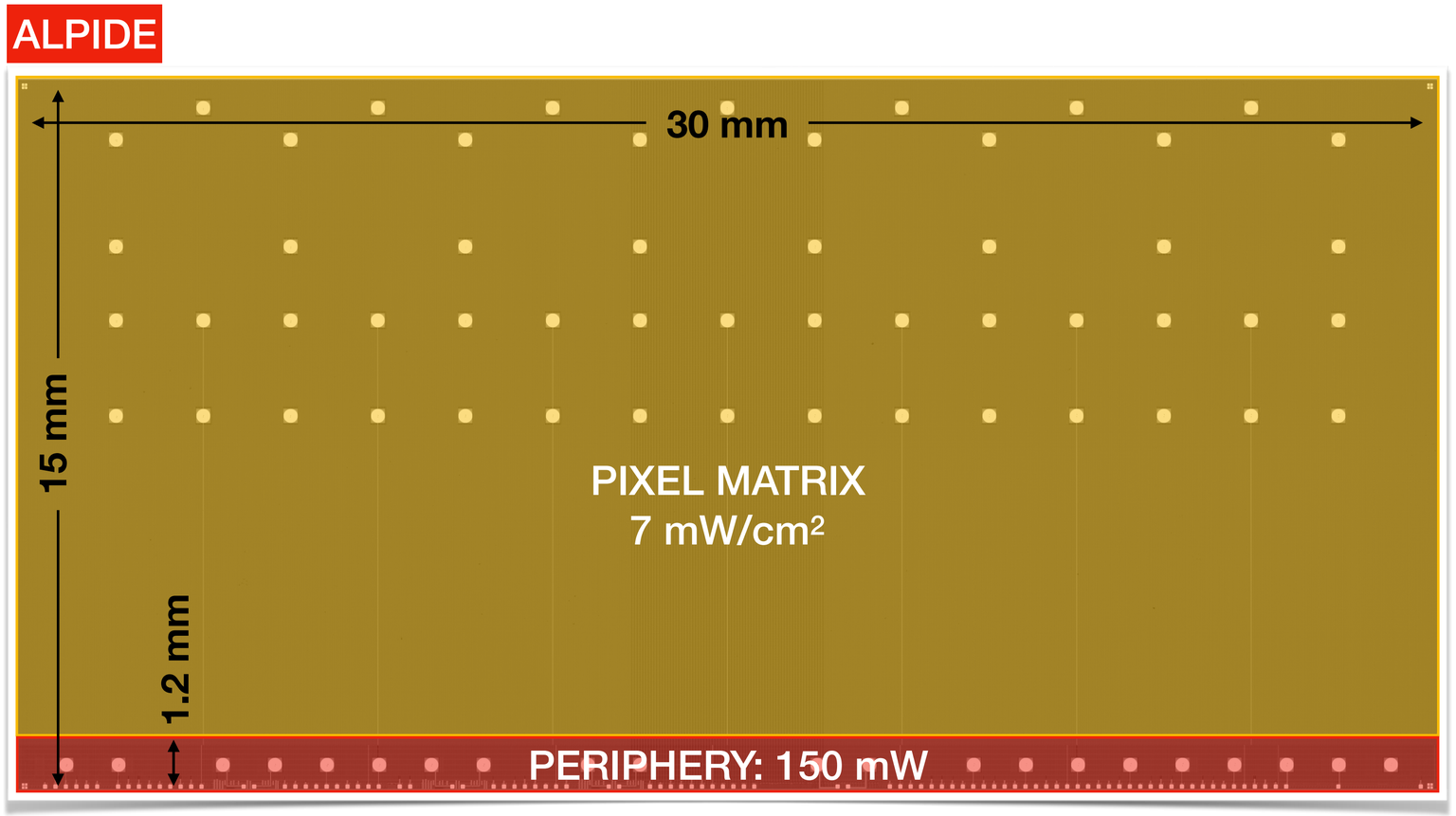
Air cooling

ALPIDE



- air cooling possible from 20 mW/cm² (was indeed studied as option for ITS2)
- ALPIDE is already close: ≈ 40 mW/cm²

Air cooling

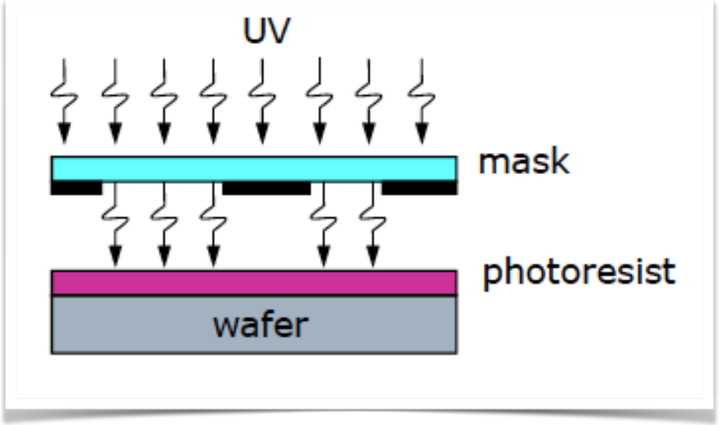


- air cooling possible from 20 mW/cm² (was indeed studied as option for ITS2)
- ALPIDE is already close: ≈ 40 mW/cm²
- Actually, already largely sufficient *if* its periphery can be placed outside the fiducial volume

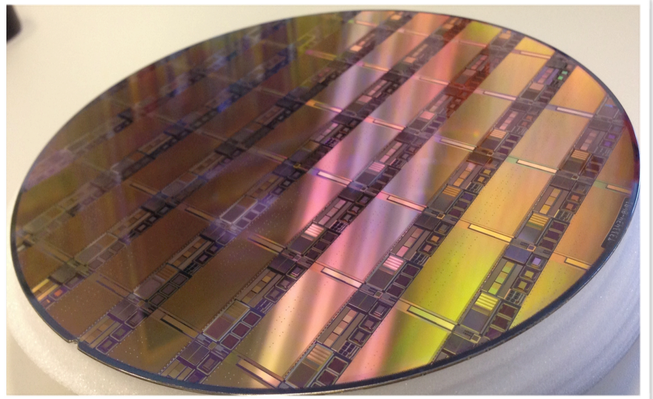
Wafer-scale chip

- Chip size is traditionally limited by CMOS manufacturing (“reticle size”)
  - typical sizes of few cm²
  - modules are tiled by chips connected to a flexible printed circuit board

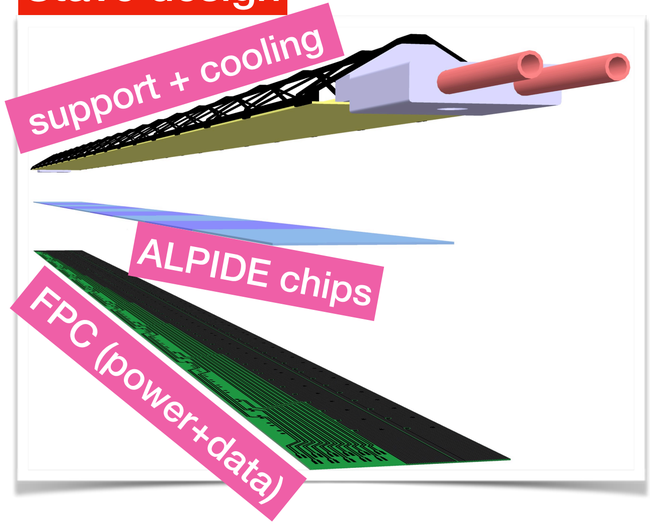
Principle of photolithography



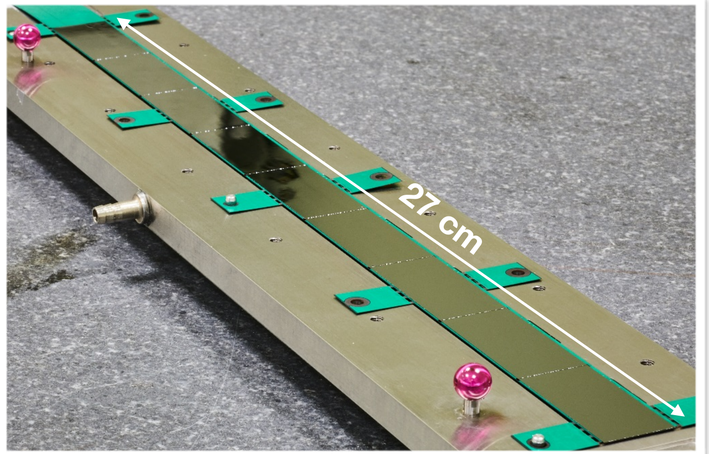
200 mm ALPIDE prototype wafer



Stave design



FPC + chips

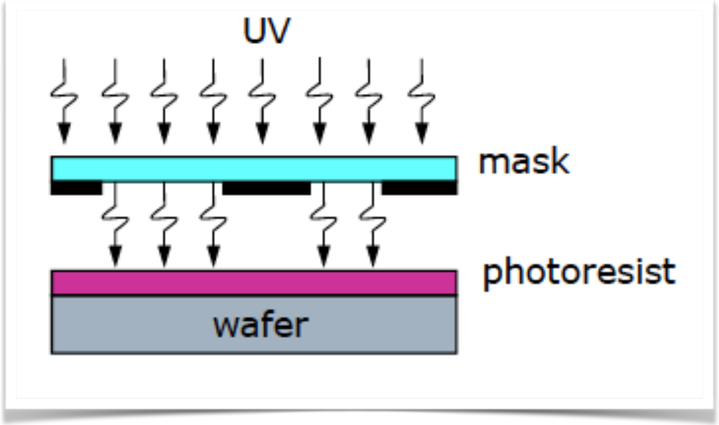


Wafer-scale chip

- Chip size is traditionally limited by CMOS manufacturing (“reticle size”)
  - typical sizes of few cm^2
  - modules are tiled by chips connected to a flexible printed circuit board

- New option: stitching, i.e. aligned exposures of a reticle to produce larger circuits
  - actively used in industry
  - a 300 mm wafer can house a chip to equip a full half-layer
  - *requires dedicated chip design*

Principle of photolithography



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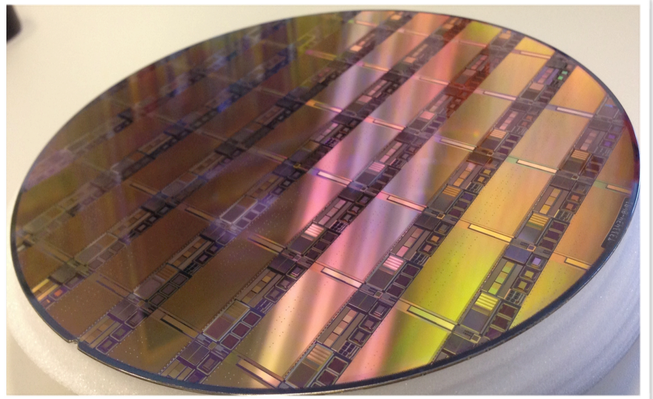
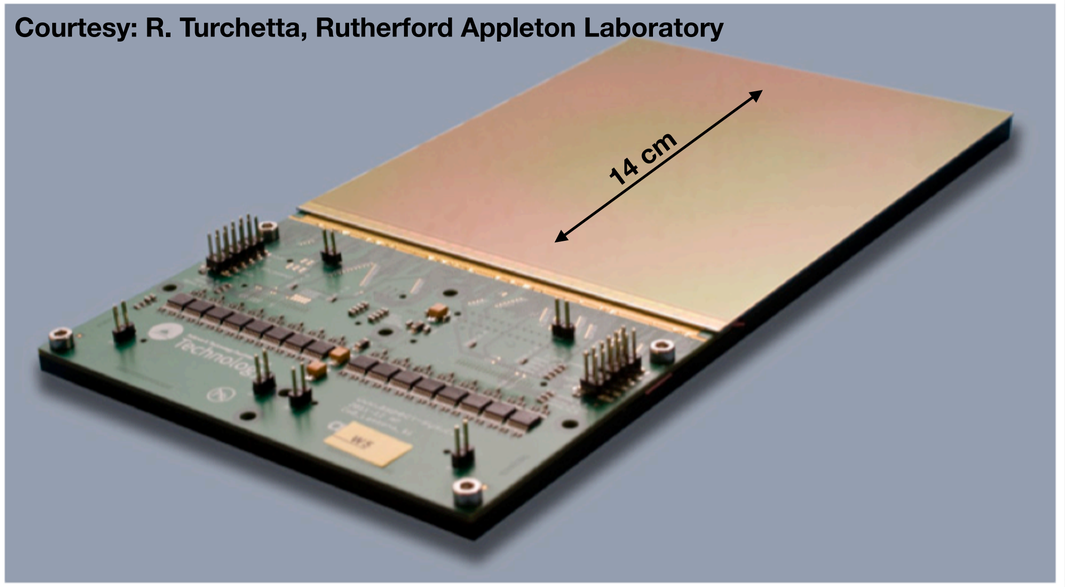
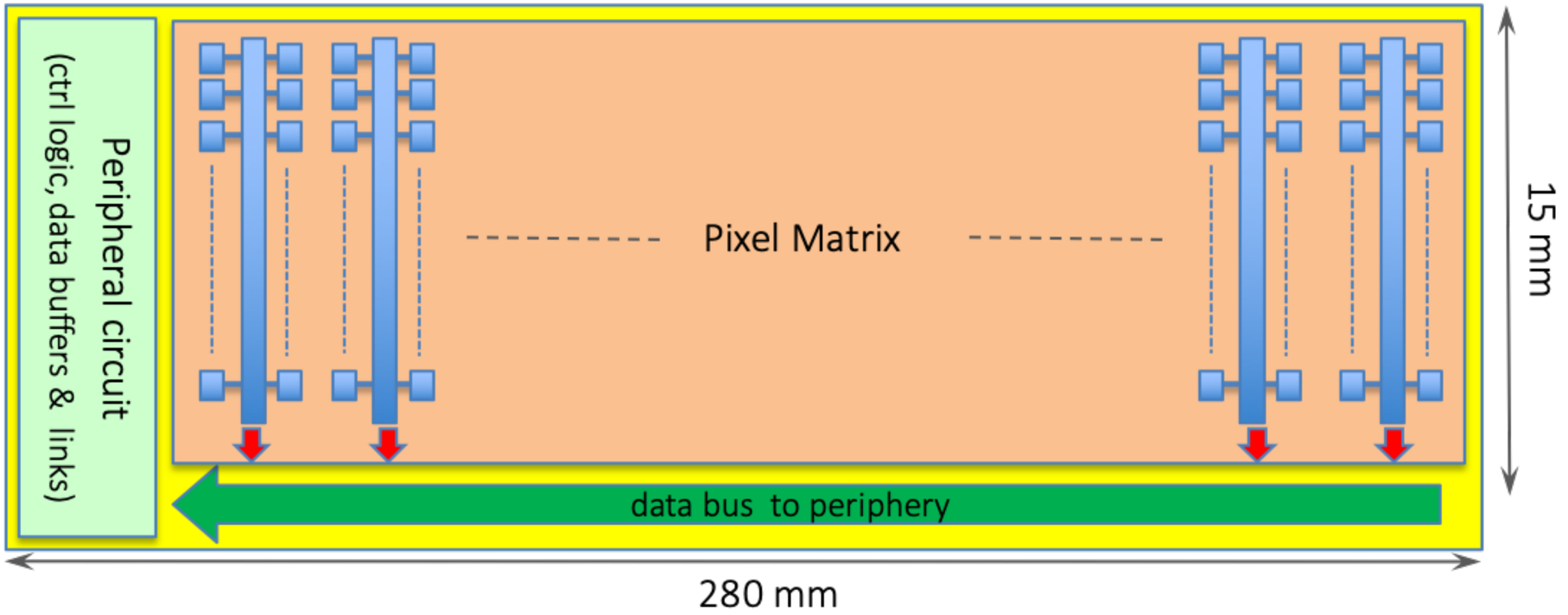


Wafer-scale sensor



Wafer-scale chip (2)

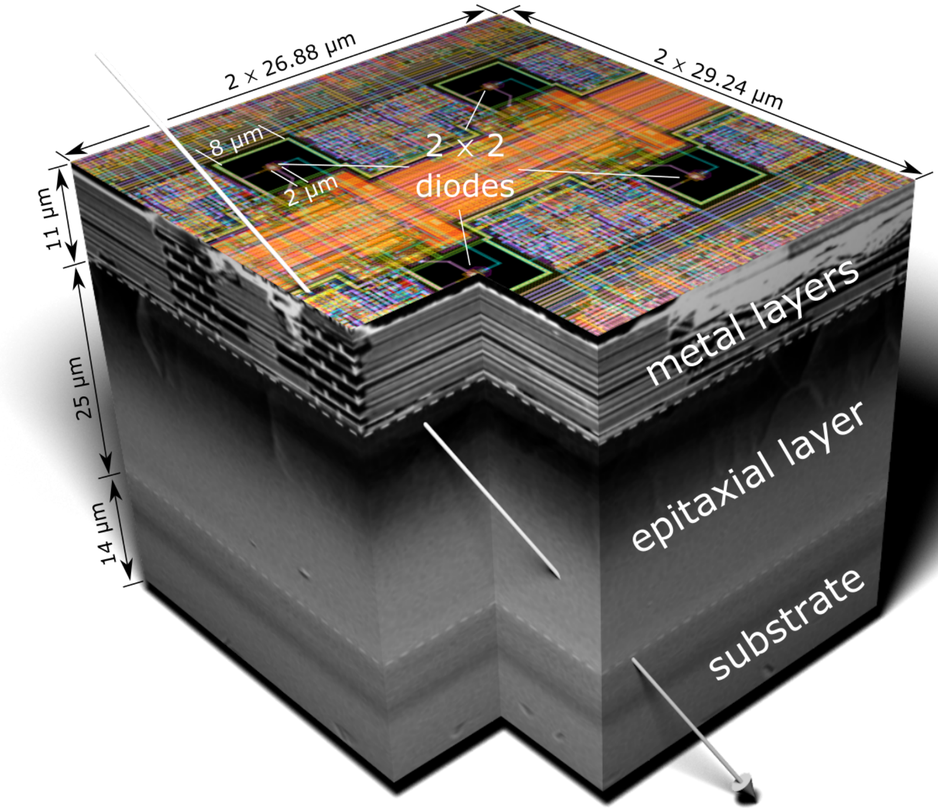
Possible architecture



- Starting from ALPIDE architecture
- Porting to 65 nm technology node
  - smaller pixels
  - larger wafers (300 mm instead of 200 mm)
- Basic building block of 15 mm height
  - to be repeated n times in vertical direction to obtain the sizes needed per layer

Thinning and bending silicon

- CMOS sensors are already very thin
  - ALPIDE is 50 µm thick
  - it uses an epitaxial layer of 25 µm as sensing layer, i.e. 50% of volume is active
  - thinner (18, 20 µm) epitaxial layers were also tried and yield similar performances
- Realistically heights of ≈ 30-40 µm are already possible
  - The 65 nm process has even thinner metal stack
  - smaller pixels would likely allow for even thinner epi-layers
- Below 50 µm, Si wafers become flexible, “paper-like”



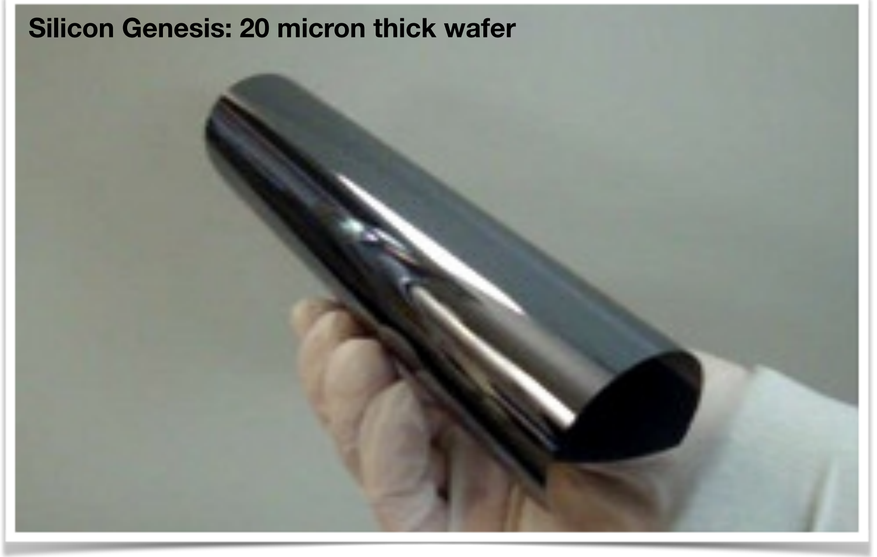
schematic cross-section of ALPIDE

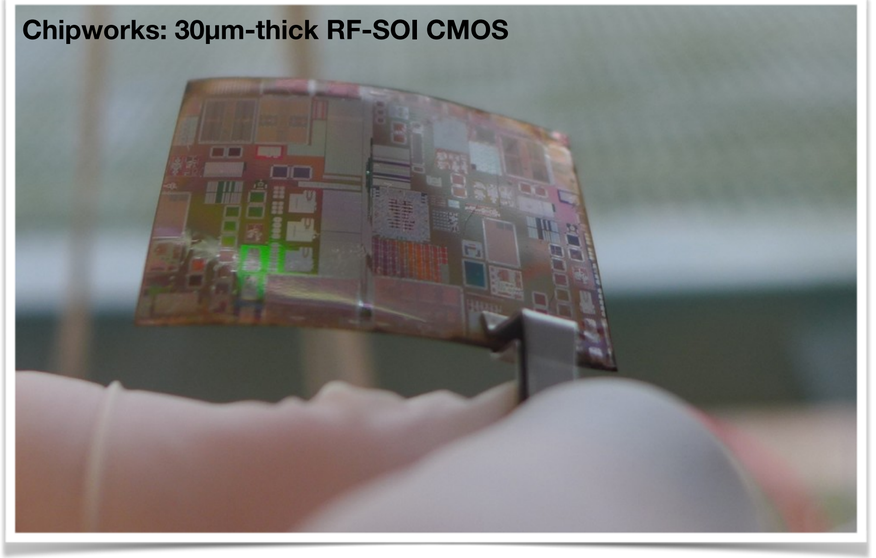
Thinning and bending silicon

- Bending Si wafers and circuits is generally possible and done in industry
- Radii *much* smaller than our needs have been achieved
- Results can depend on circuitry
  - Demonstration with ALPIDE wafers under way
- Interconnection options to be studied

Die type	Front/back side	Ground/polished/plasma	Bumps	Die thickness (µm)	CDS (MPa)	Weibull modulus	MDS (MPa)	r_{min} (mm)
Blank	Front	Ground	No	15–20	1263	7.42	691	2.46
Blank	Back	Ground	No	15–20	575	5.48	221	7.72
IZM28	Front	Ground	Yes	15–20	1032	9.44	636	2.70
IZM28	Back	Ground	Yes	15–20	494	2.04	52	32.7
Blank	Back	Polished	No	25–35	1044	4.17	334	7.72
IZM28	Back	Polished	Yes	25–35	482	2.98	107	24.3
Blank	Back	Plasma	Yes	18–22	2340	12.6	679	2.50
IZM28	Front	Plasma	Yes	18–22	1207	2.64	833	2.05
IZM28	Back	Plasma	Yes	18–22	2139	3.74	362	4.72

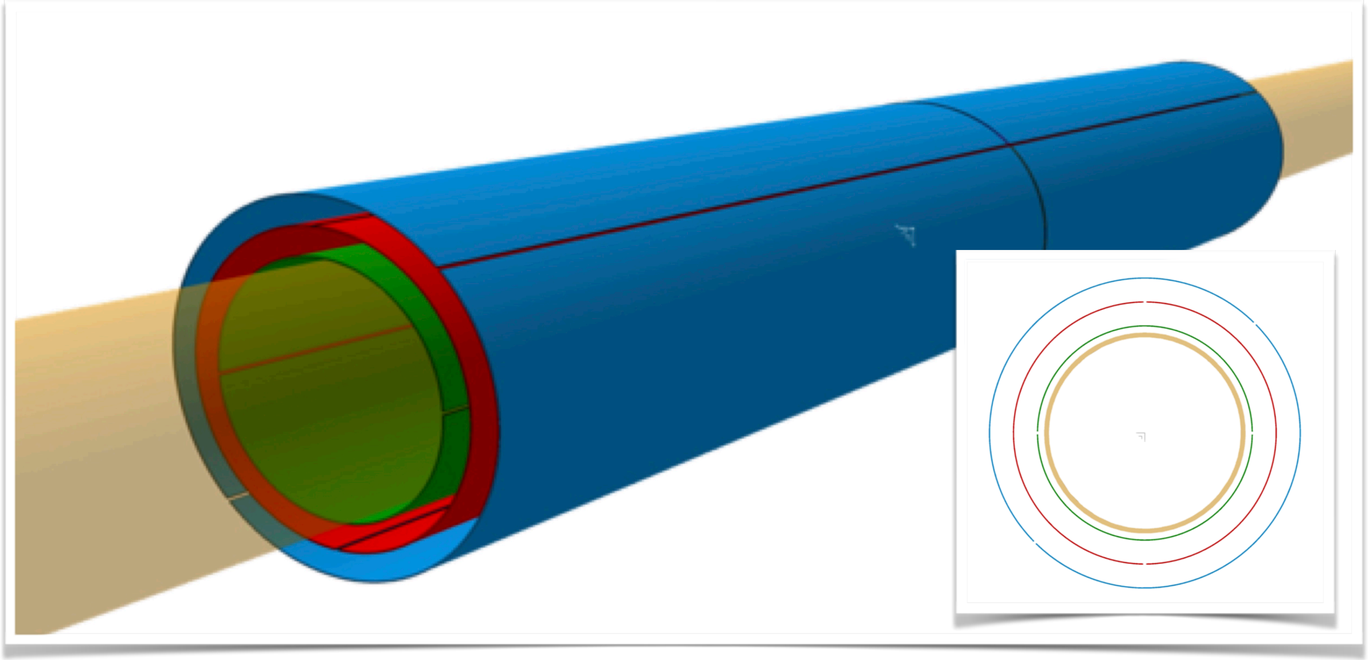
D.A. van den Ende et al., Microelectronics Reliability, vol. 54, pp. 2860-2870, 2014
http://dx.doi.org/10.1016/j.microrel.2014.07.125





- Layout and integration

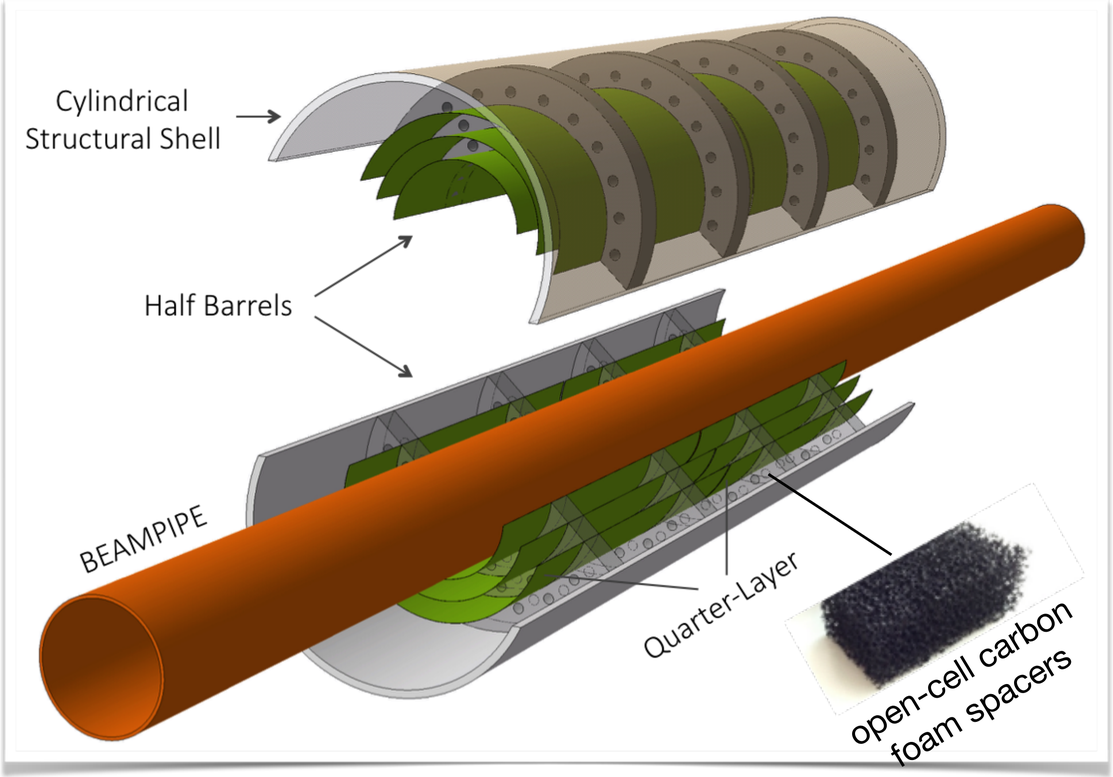
Layout

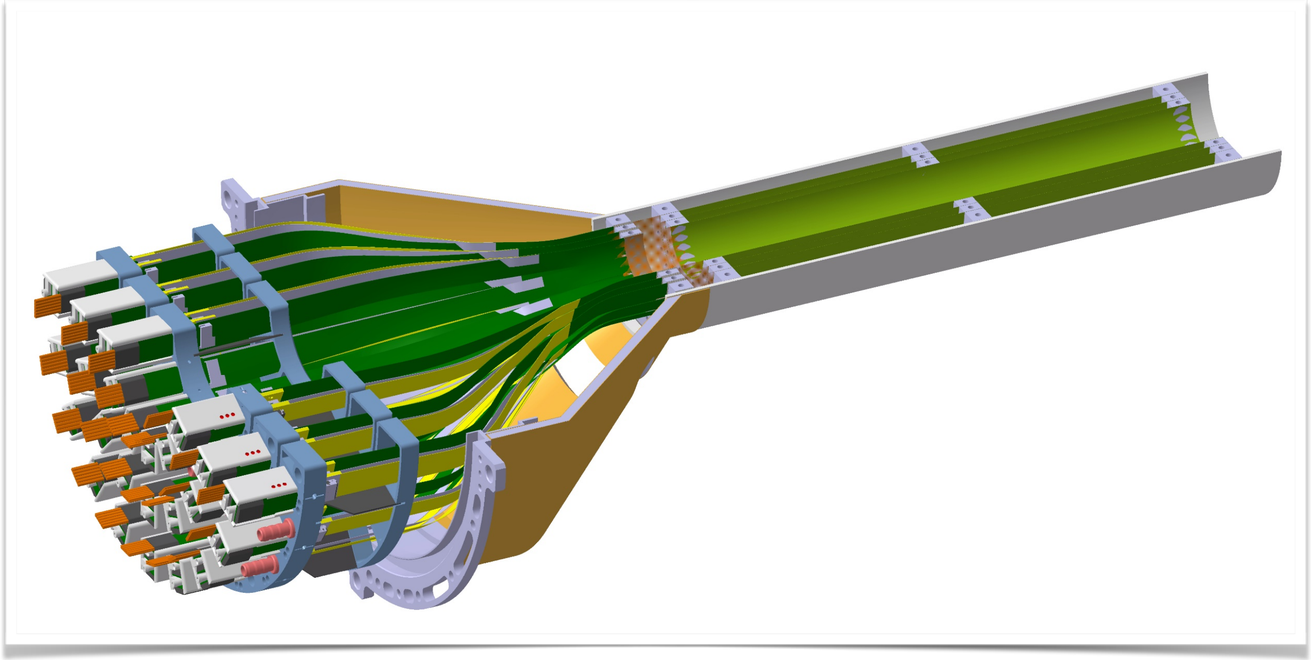


Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm^2)	610	816	1016
Pixel sensor dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		

- New beam pipe:
  - "old" radius/thickness: 18.2/0.8 mm
  - new radius/thickness: 16.0/0.5 mm
- Extremely low material budget:
  - Beam pipe thickness: 500 µm (0.14% X0)
  - Sensor thickness: 20-40 µm (0.02-0.04% X0)
- Material homogeneously distributed:
  - essentially zero systematic error from material distribution

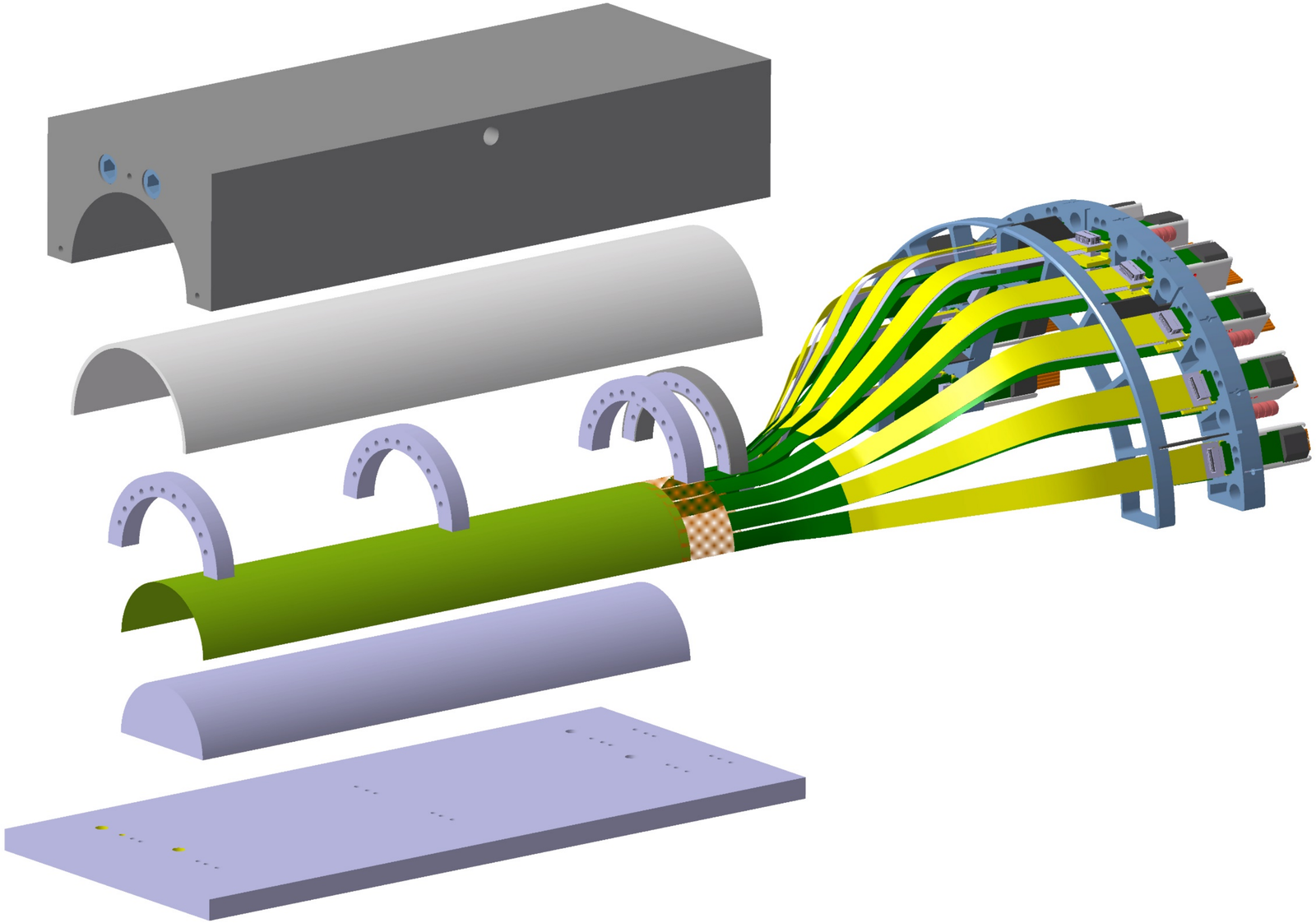
Mechanics





- Possible layout based on air-cooling
- Sensors held in place with low-density carbon foam
- Fixation into the experiment by surrounding support structure, as well as at both ends
- Cooling at the extremities (chip peripheries)

Assembly procedure



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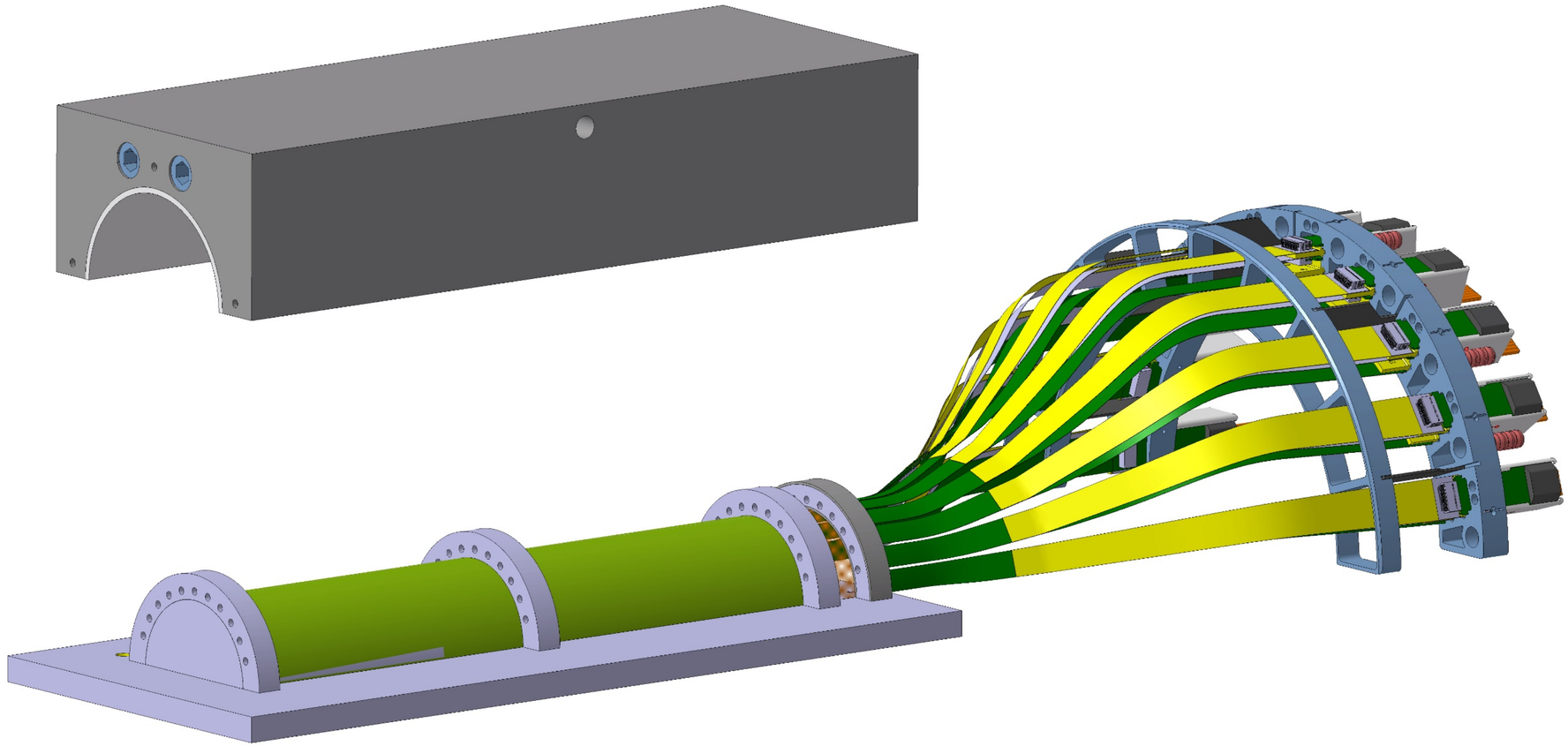

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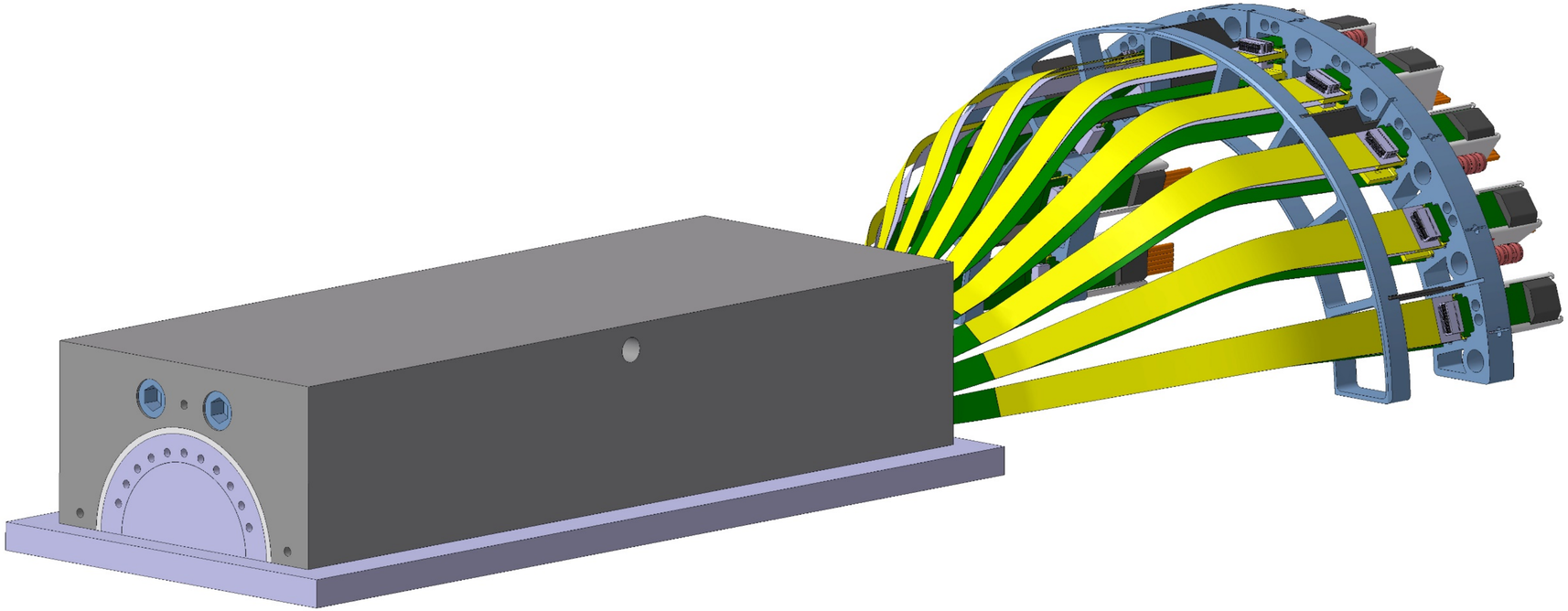

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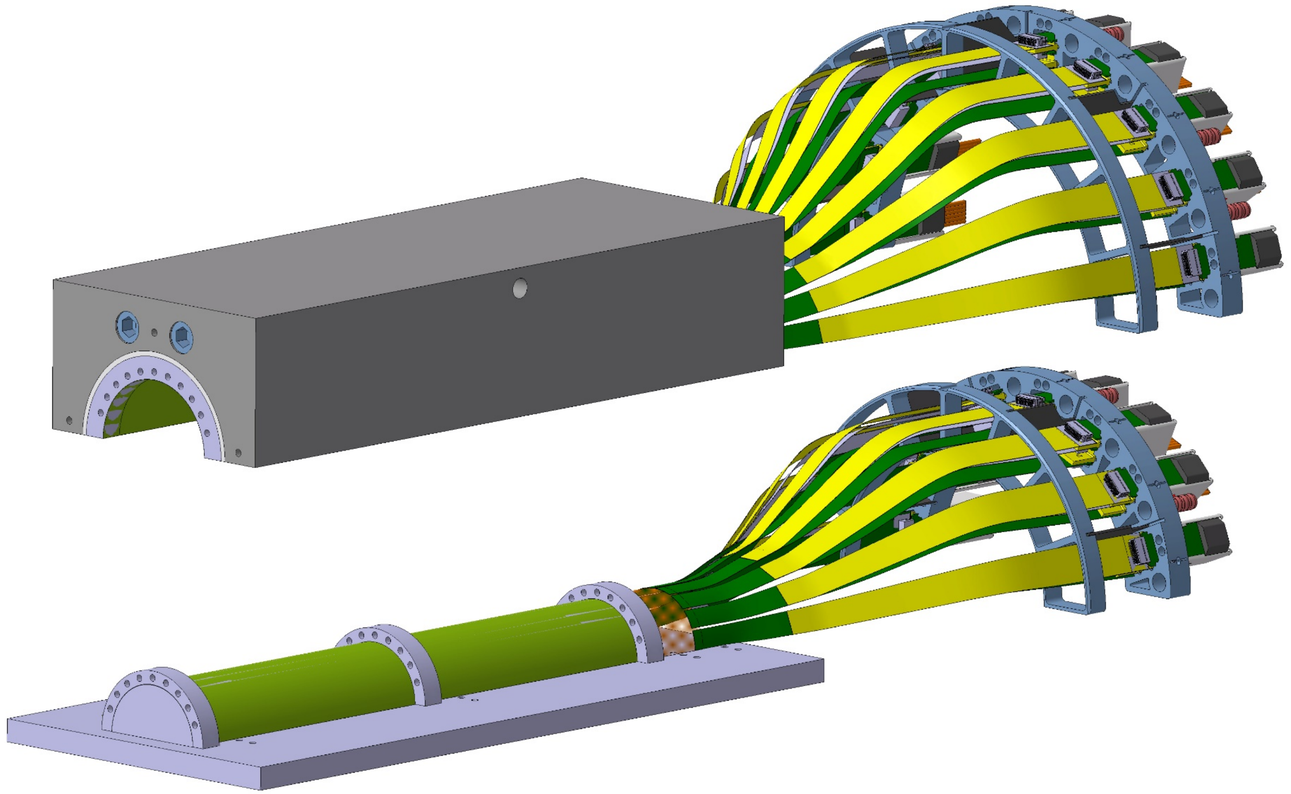

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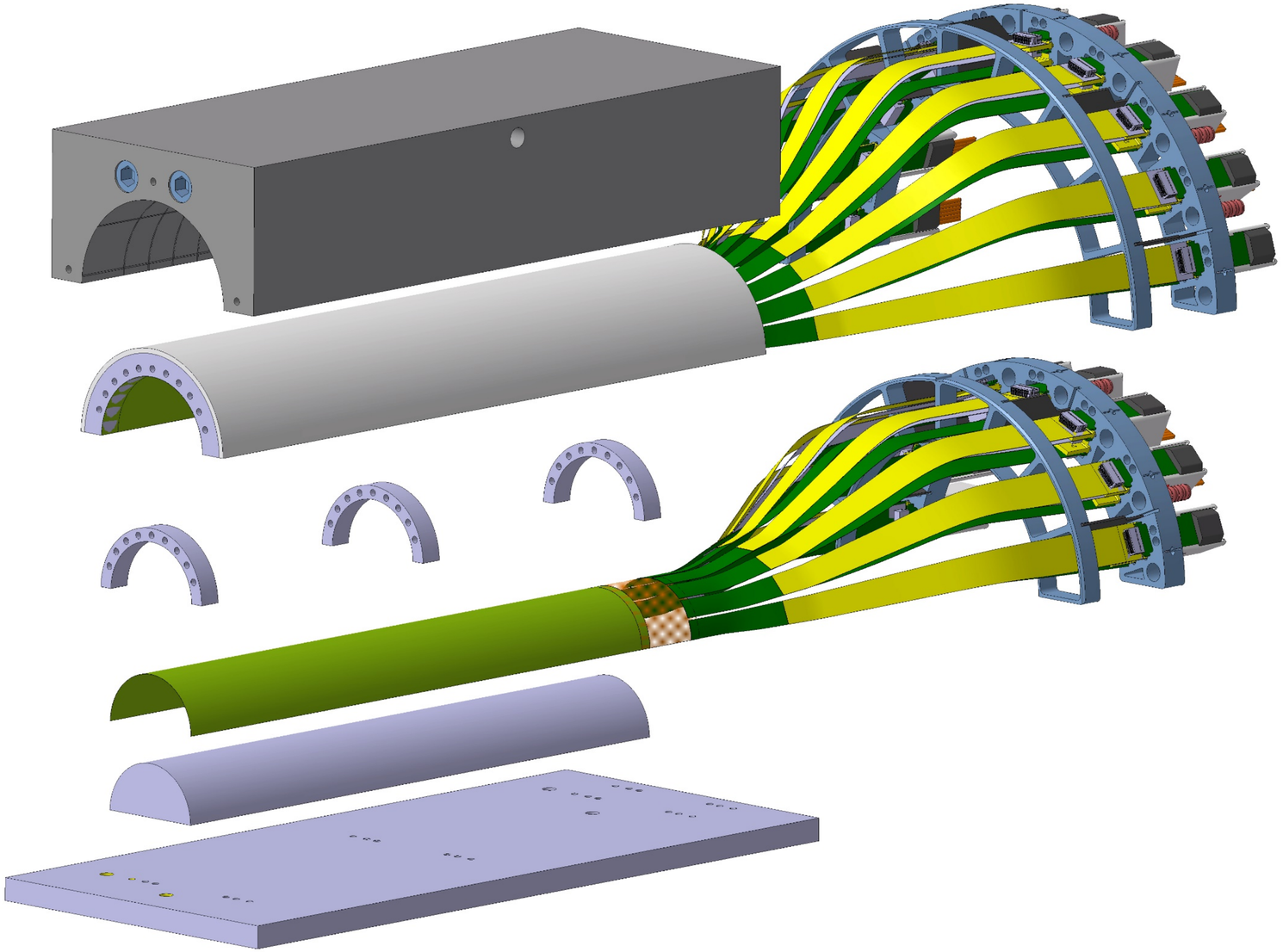

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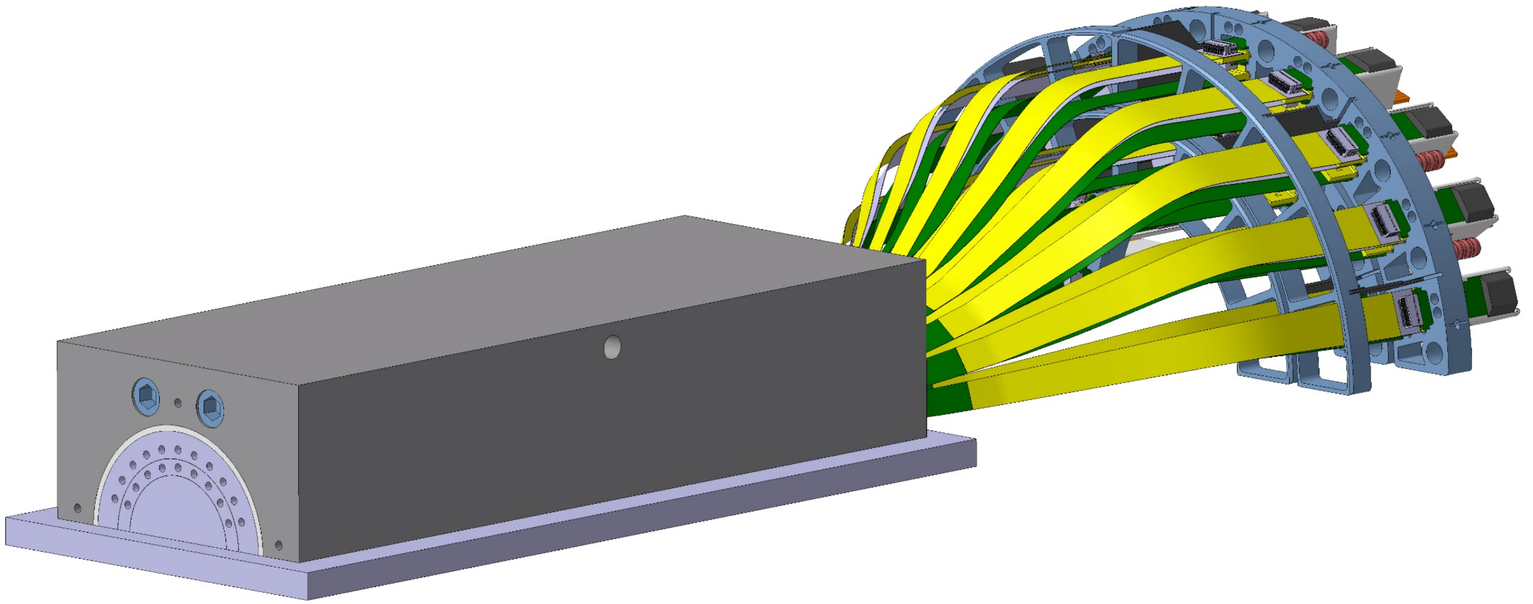

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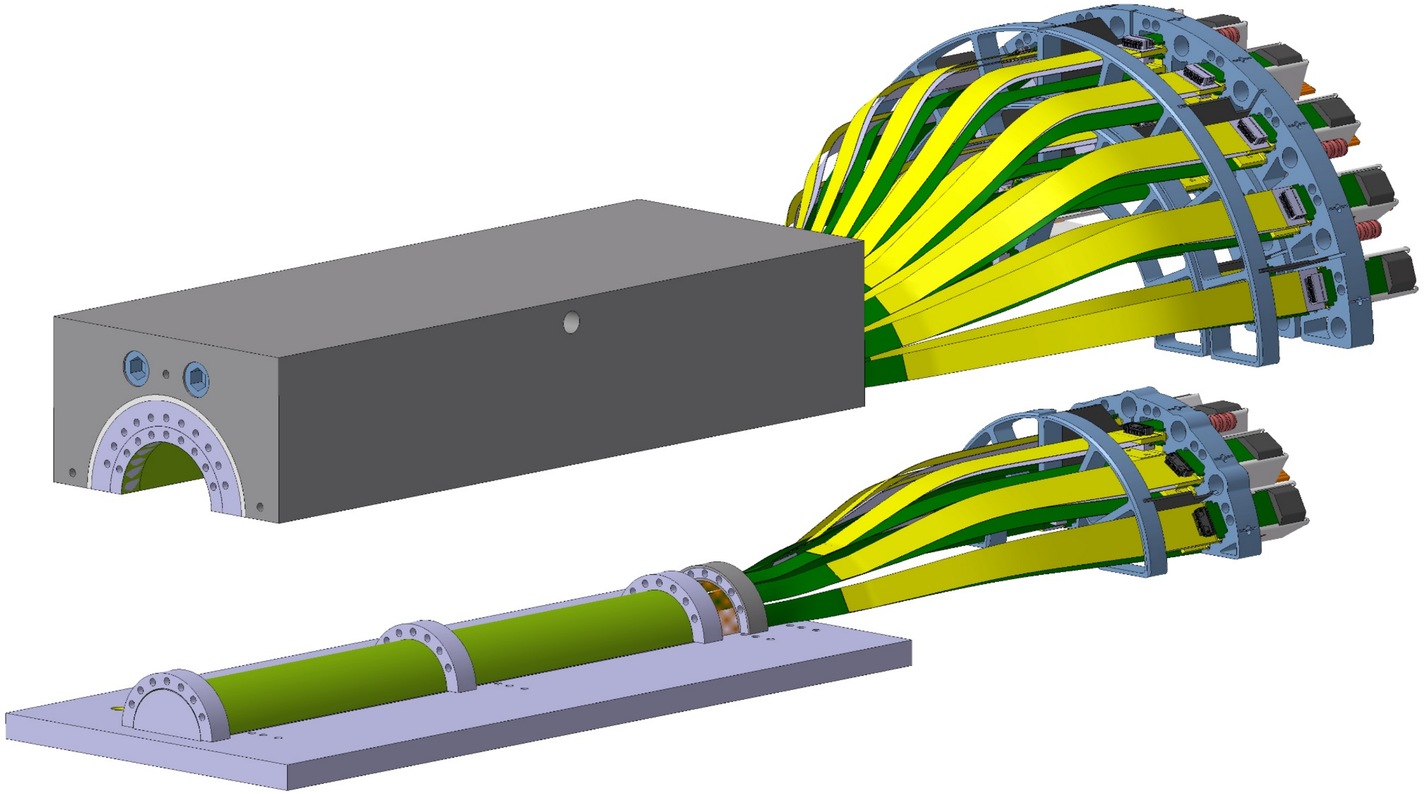

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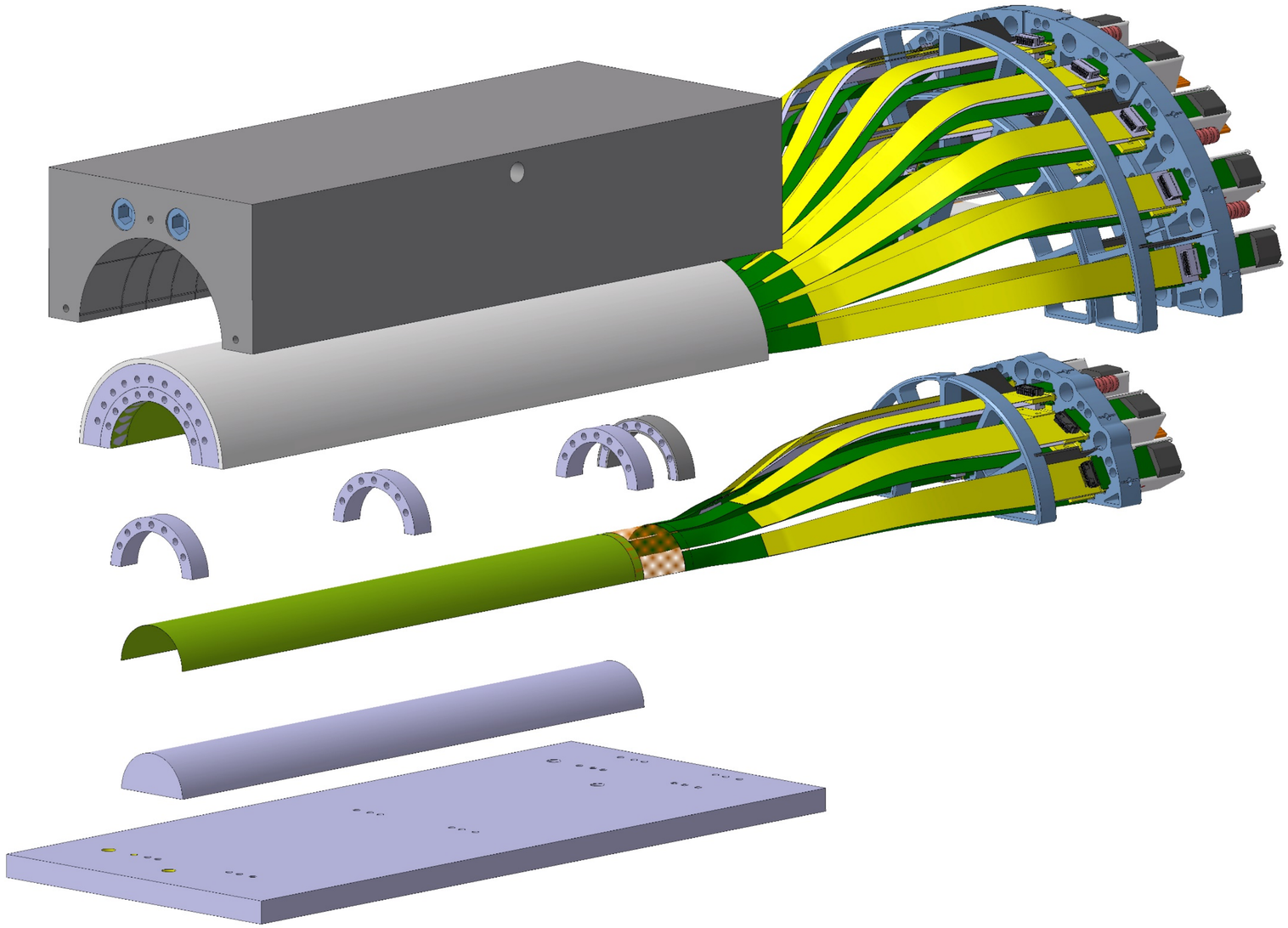
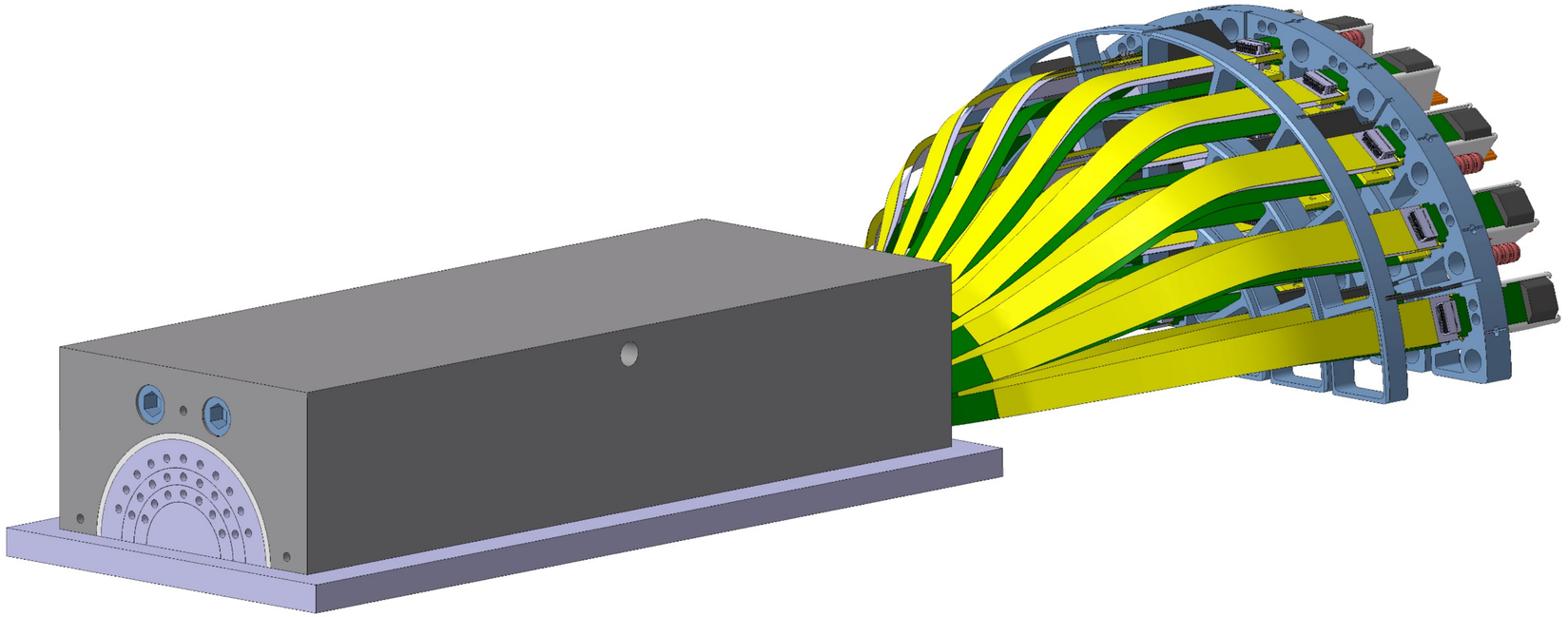
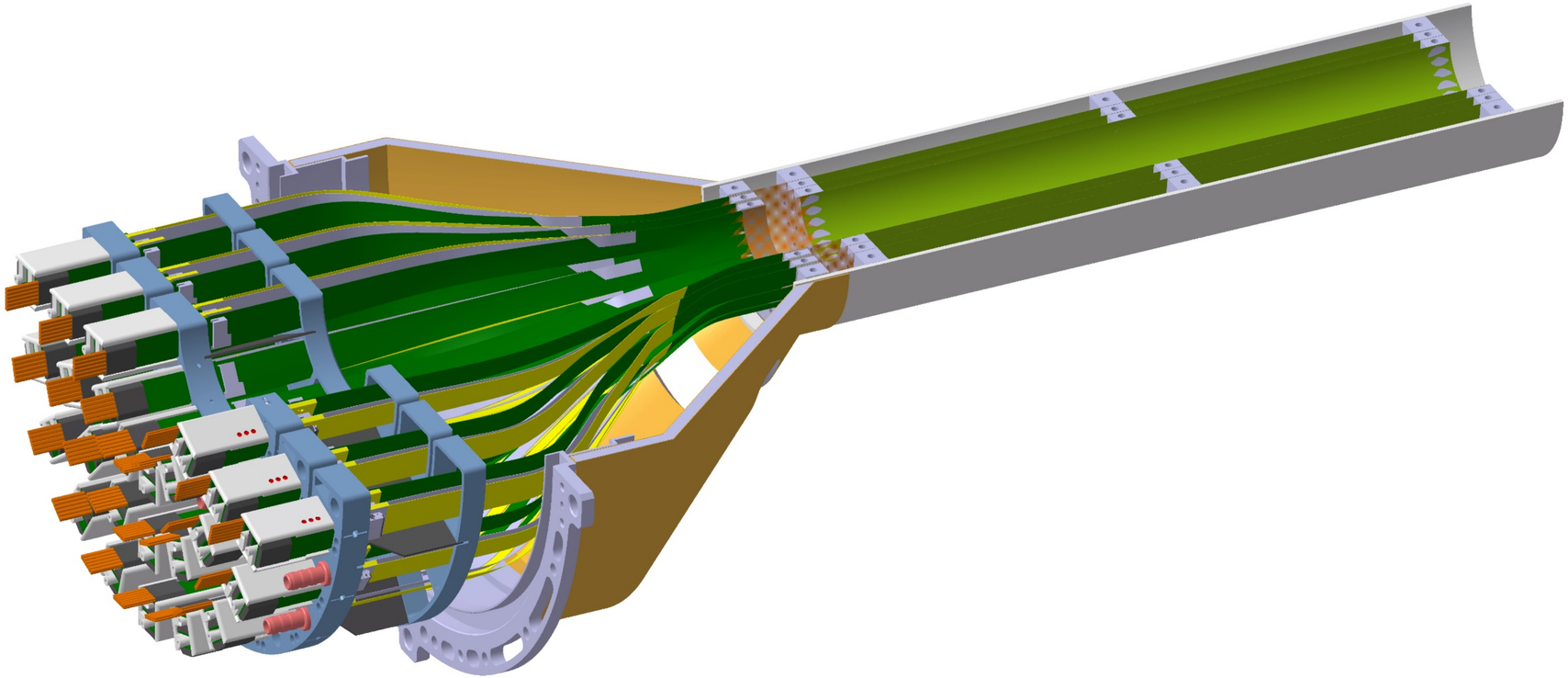


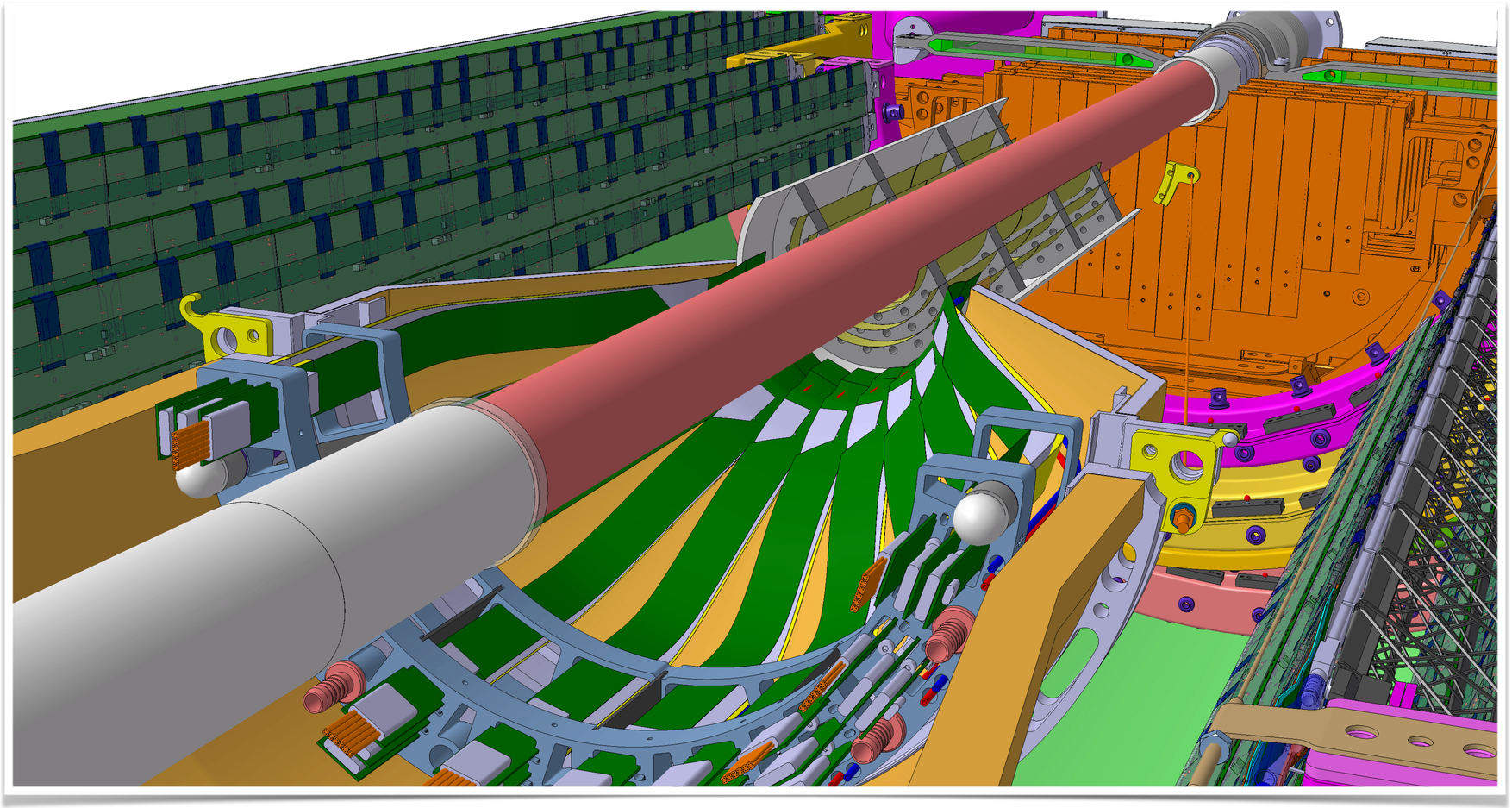
Assembly procedure



Assembly procedure



Integration

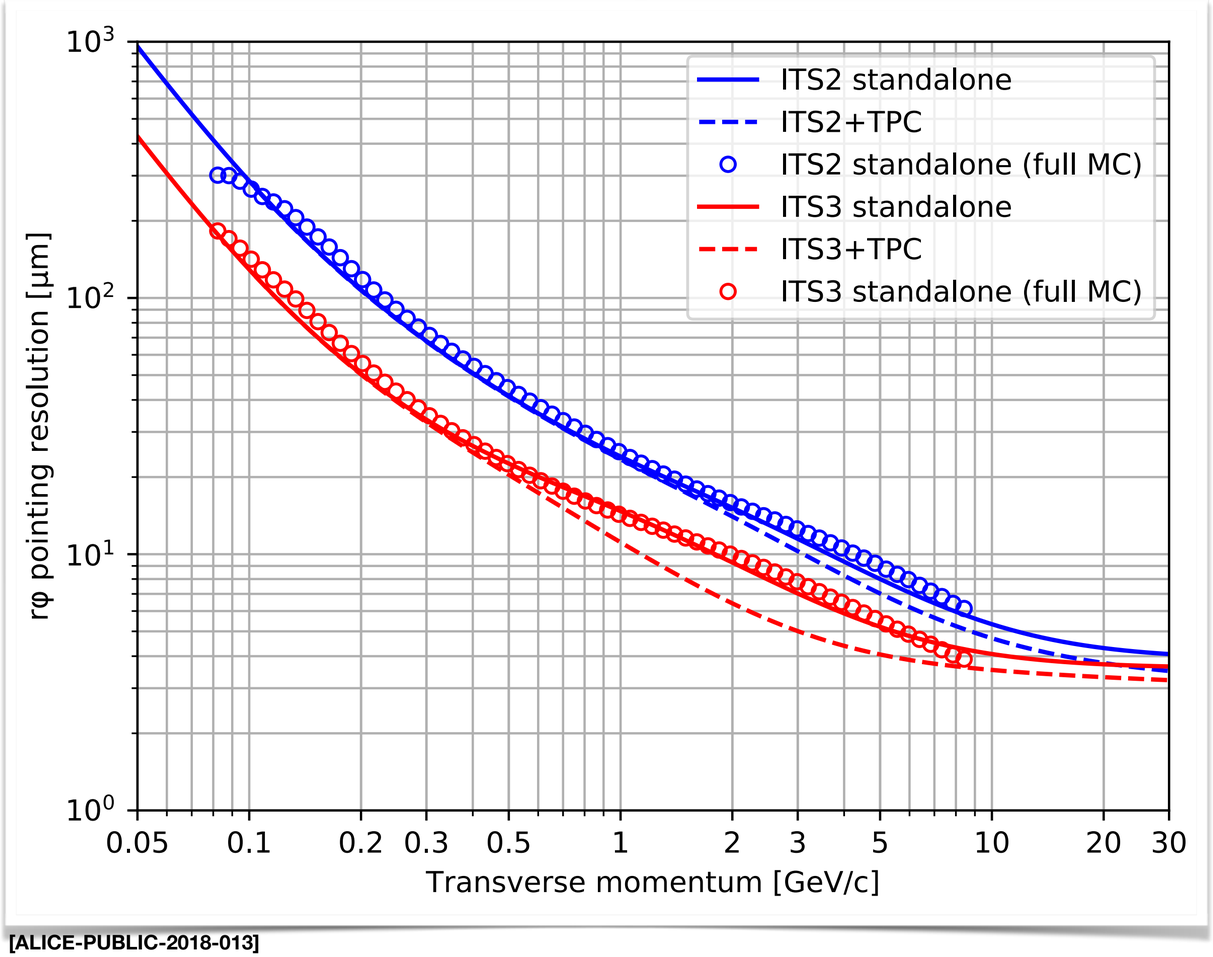


- Simply **replaces** the “old” Inner Barrel, **reuses** services (power, readout, cooling)
- Remaining ITS2 stays in place as is

- Perfomance projections

Performance figures

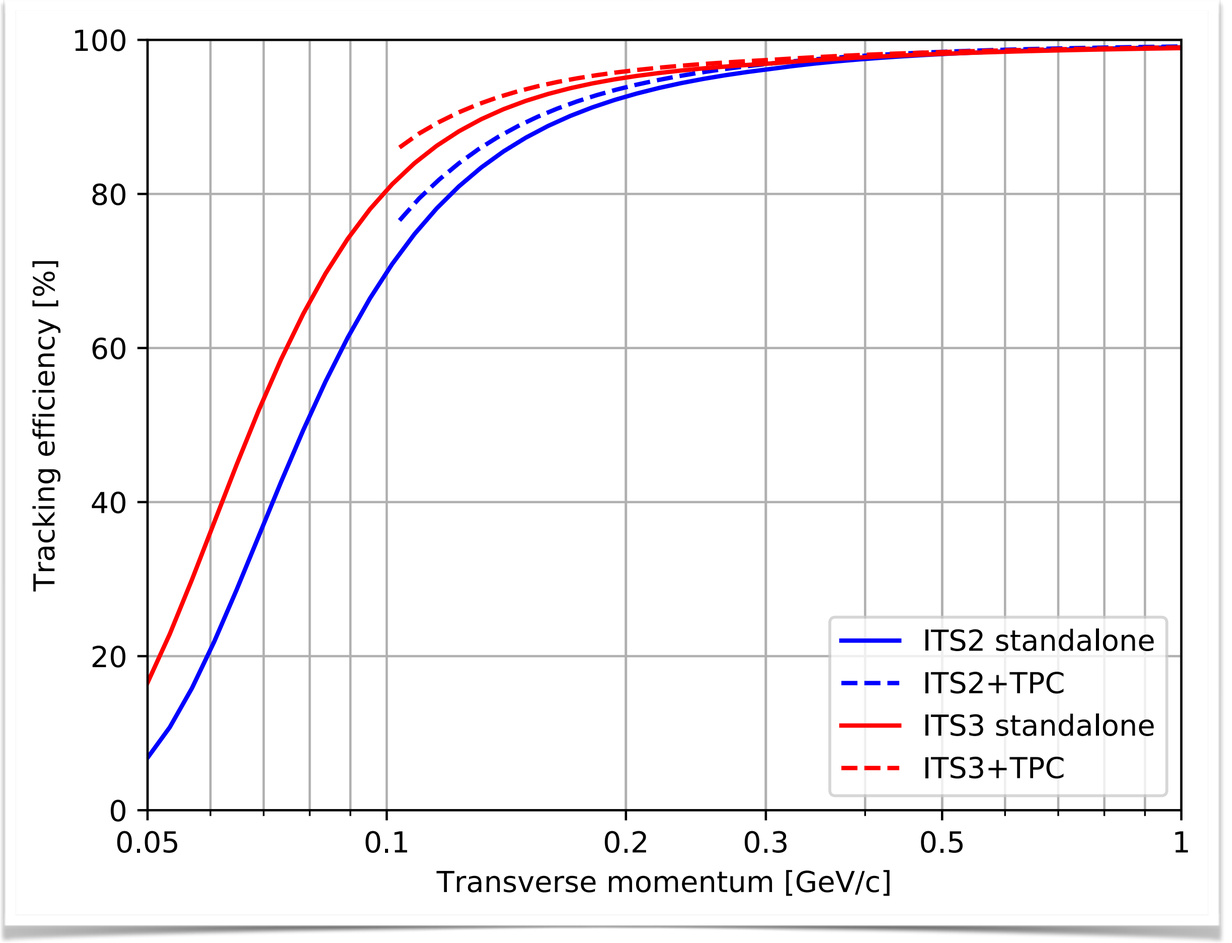
pointing resolution



[ALICE-PUBLIC-2018-013]

improvement of factor 2 over all momenta

tracking efficiency



large improvement for low transverse momenta

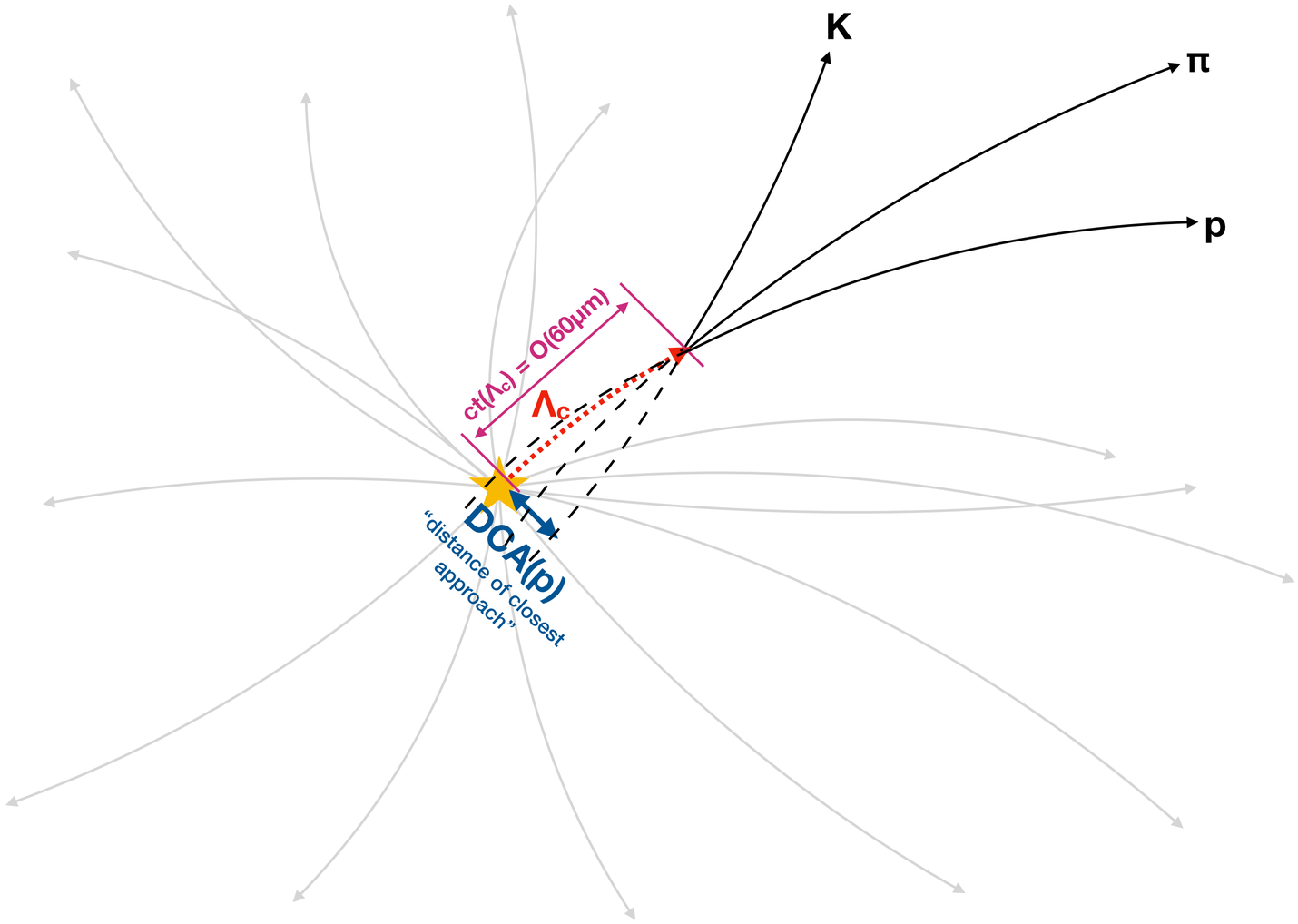
Impact on physics

- **Low-mass di-electrons**
  - Less conversions (x 1/3), one of the main “soft” backgrounds
  - Better low-p_T standalone efficiency to reconstruct and reject conversions
  - Better precision to reject or subtract conversion and charm-decay electrons (displaced)

- **Heavy flavour** in particular those with small $c\tau$ ($\Lambda_c \approx 60$ μm, $D_s \approx 150$ μm)
  - Better precision to separate secondary vertex
  - Increased efficiency also helps in multi-prong decays

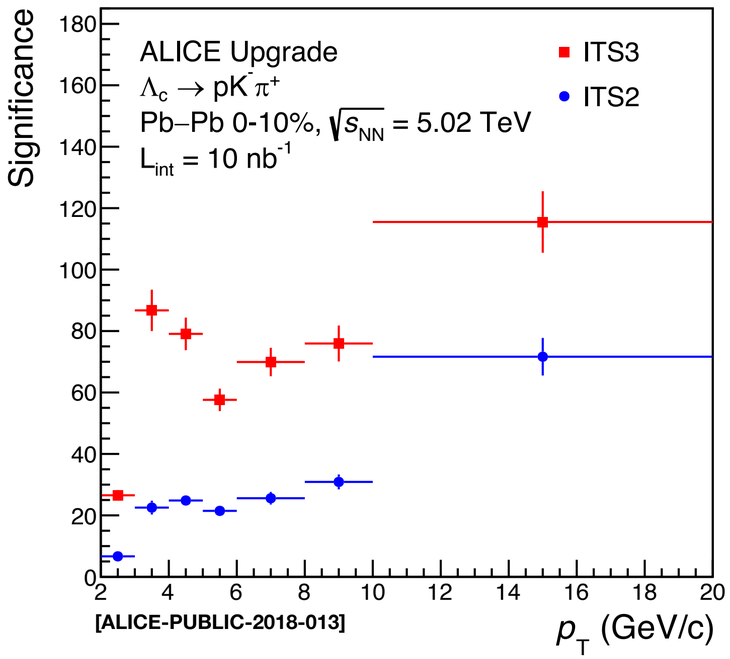
Lambda-c (Λ_c)

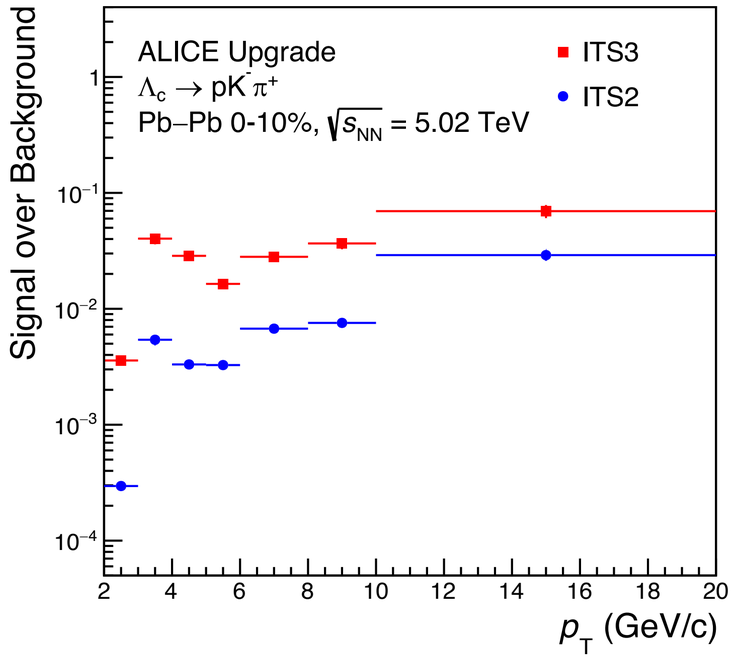
schematic view of a Λ_c decay

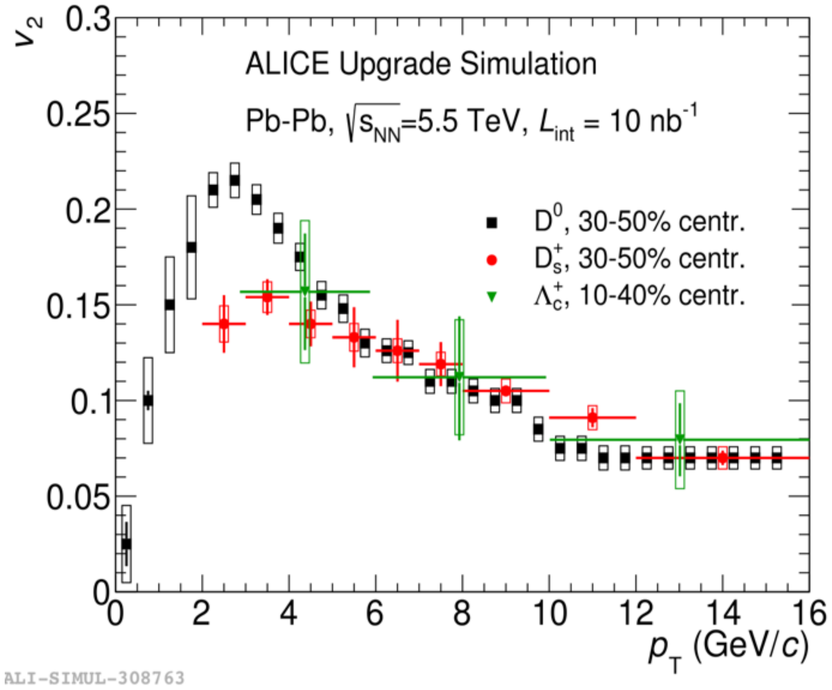


- Analysis difficult due to large combinatorial background:
  - O(10k) charged particles in a central Pb-Pb collision
- Discrimination of background via:
  - Particle identification (relatively low yield of protons and Kaons wrt. pions)
  - **Topology:** cut on DCA of single tracks (before making the combinations) and decay vertex position (needs combinations)

Lambda-c (Λ_c) (2)







- Large improvement of S/B + significance due to better separation power of secondary decay vertex ($\Lambda_c \approx 60$ µm)
- Allows for precision measurements over a wide p_T range

Λ_c yield	S/B	Significance
ITS3 / ITS2	10	4

There is much more

- **Beauty baryon Λ_b**
  - b quark recombination in QGP?
  - $\Lambda_b \rightarrow \Lambda_c\pi$
  - Limited to $p_T > 4$ GeV/c with ITS2
  - Expected improvement from better Λ_c S/B

- **Charm-strange baryons**
  - Interplay of c recombination and s "enhancement" in QGP
  - Ξ_c ($c\tau \approx 80$ μm) → pKπ, Ξp
  - Ω_c ($c\tau \approx 130$ μm) → Ωp

- **Non-prompt D_s and Λ_c**
  - From impact parameter fits of inclusive D_s and Λ_c
  - Give access to B_s and Λ_b
  - Try $B_s \rightarrow D_s\pi$ as well

- **c-deuteron search**
  - Λ_cn bound state
  - Would be the lightest hyper-nucleus with charm
  - Statistical hadronisation model: dN/dy ≈ 104 with L_{int}=10 nb^{-1} Pb-Pb
  - Similar cτ and decays as Λ_c: ≈ 60 μm, → pKπ, → dK^0_S

- **Charm correlations and jets**
  - DD correlations & c-tagged jets sensitive to details of charm energy loss mechanisms (radiative, collisional,…)
  - Expect with improvement with ITS3 (short D0 decay length)

- **… many more under study**

R&D + Construction Timeline

Project milestones

- EoI details milestones for all activities, grouped by:
  - Sensor Chip
  - Thinning and bending
  - Mechanics and cooling
  - Beam pipe
- R&D starts now
- TDR is foreseen for 2022

example: chip design

Milestone	Description	Production[a]	Date
1	**Technology test structures** single pixels, transistors, small memory cell array for studying the radiation hardness of the technology	MPW	Q4 2019
2	**Pixel test vehicle** optimization of pixel and diode geometries	MPW	Q3 2020
3	**Large area prototype** basic blocks: pixel matrix, periphery, output serial links exercising of stitching different parts	ER	Q4 2021
4	**Full-scale prototype** prototype of final chip with all functionality	ER	Q4 2022
5	**Final Chip** possible minor adjustments wrt milestone 4	ER	Q4 2023

[ALICE-PUBLIC-2018-013]

Summary & Outlook

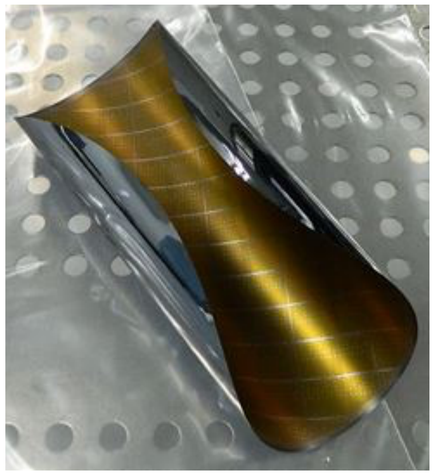
- ALICE is starting the R&D for a **nearly massless, truly cylindrical, Si-only, wafer-scale** Inner Tracking System
- **Unprecedented performance figures**, especially for **low-momentum** particles, will largely increase the ALICE physics yield
- Needed **technology is within reach** but will require an **intense R&D phase**
- At its 139th meeting (Sep 2019), the **LHCC endorsed** the R&D with the goal of presenting the **TDR in 2022**
- **Installation** is foreseen for **LS3**

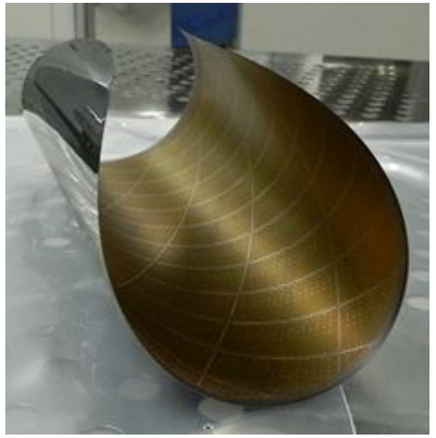
Thank you!

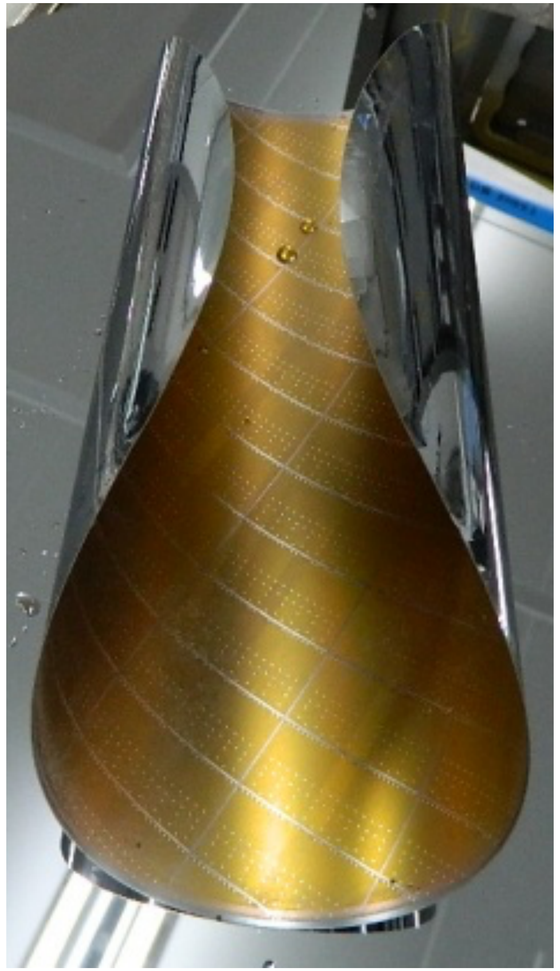
Supplemental material

… it was already done…

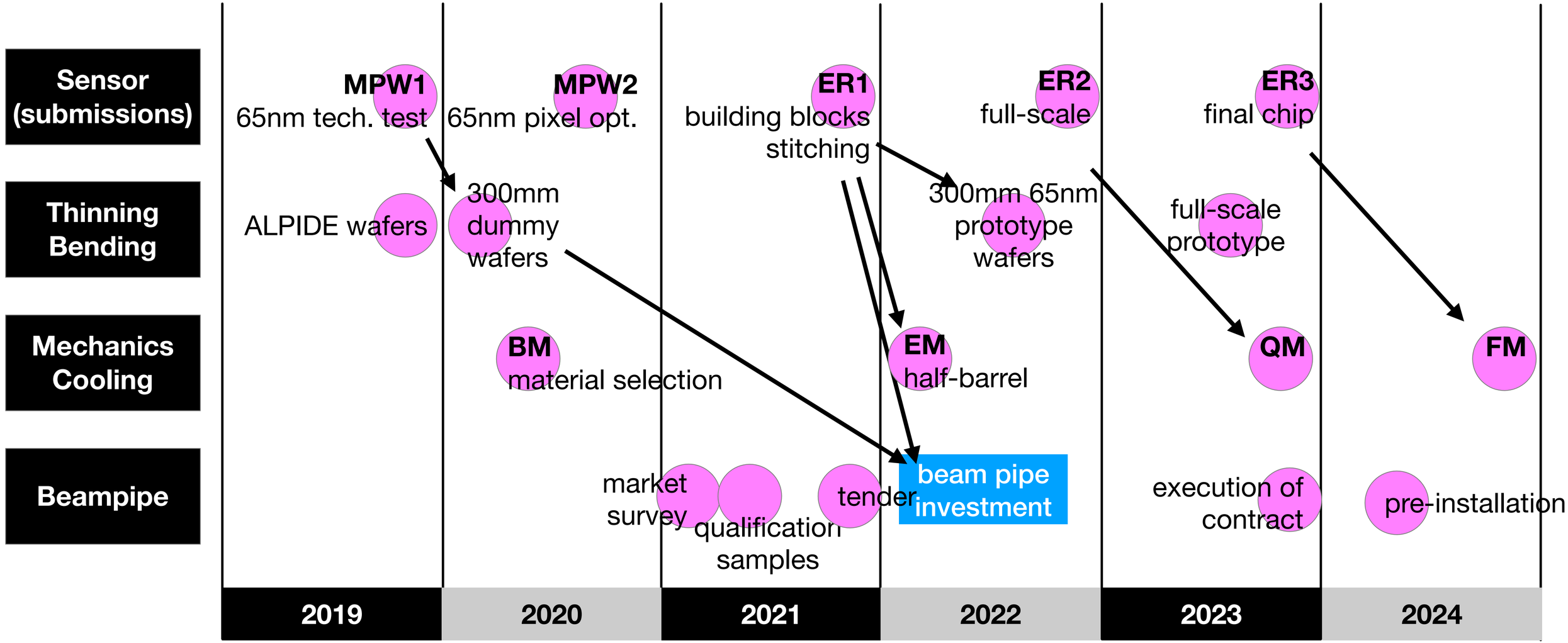
- Indeed “warpage” is omnipresent when working with thin sensors
- We accidentally produced curved ALPIDEs
- On chip and on wafer level







Milestone summary



MPW: multi-project wafer run, **ER:** engineering run, **BM:** breadboard module, **EM:** engineering module, **QM:** qualification module, **FM:** final module

Project milestones

Milestone	Description	Date
1	**Market survey** preparation of beampipe technical specifications definition of technical and commercial criteria for the selection of suppliers preparation of technical specifications for the qualification samples[a] selection of candidate supplier	Q1 2021
2	**Evaluation of candidate suppliers** production of qualification samples (by candidate suppliers) evaluation of qualification samples (by CERN)	Q2 2021
3	**Tender** preparation of technical specification document invitation to tender	Q4 2021
4	**Execution of contract** R&D phase (until Q2 2022) production	Q4 2023
5	**Pre-installation phase (CERN)** Acceptance and post production activities	Q2 2024

Milestone	Description	Date
1	**ALPIDE wafers** based on existing 200 mm ALPIDE wafers characterization of mechanical stability characterization of sensor performance	Q4 2020
2	**300 mm dummy wafers** based on pad wafers (top metal only) characterization of mechanical and thermal properties	Q1 2021
3	**Wafers with large prototypes** using ER with larger arrays (milestone 3 of Tab. 3) characterization of influence of realistic circuitry onto mechanical properties beam tests	Q3 2022
4	**Full-scale prototype** using full-scale prototype (milestone 4 of Tab. 3) validation of mechanical, electrical, and detection properties beam tests	Q3 2023

Milestone	Description	Date
1	**Breadboard Module (BM)** selection of carbon materials based on structural and thermal properties production of samples for material characterization development of FE and CFD models for structural and thermal simulations	Q2 2020
2	**Engineering Module (EM)** production of one half-layer with dummy chips thermal and dynamic stability tests (including wind tunnel) development of half-barrel assembly procedures and jigs production of first half-barrel with dummy chips thermal and dynamic stability tests (including wind tunnel) drawings, FE and CFD analysis reports	Q1 2022
3	**Qualification Module (QM)** production of two half-barrels with prototype chips thermal and dynamic stability tests (including wind tunnel) electrical functional test final assembly and test procedures, technical specifications and drawings	Q4 2023
4	**Final Module (FM)** production of four half-barrels with final chips electrical and mechanical acceptance tests	Q4 2024

Milestone	Description	Production[a]	Date
1	**Technology test structures** single pixels, transistors, small memory cell array for studying the radiation hardness of the technology	MPW	Q4 2019
2	**Pixel test vehicle** optimization of pixel and diode geometries	MPW	Q3 2020
3	**Large area prototype** basic blocks: pixel matrix, periphery, output serial links exercising of stitching different parts	ER	Q4 2021
4	**Full-scale prototype** prototype of final chip with all functionality	ER	Q4 2022
5	**Final Chip** possible minor adjustments wrt milestone 4	ER	Q4 2023

LHCC

CERN/LHCC-2019-010
LHCC-139
September 2019

LARGE HADRON COLLIDER COMMITTEE

Minutes of the one-hundredth-and-thirty-ninth meeting held on

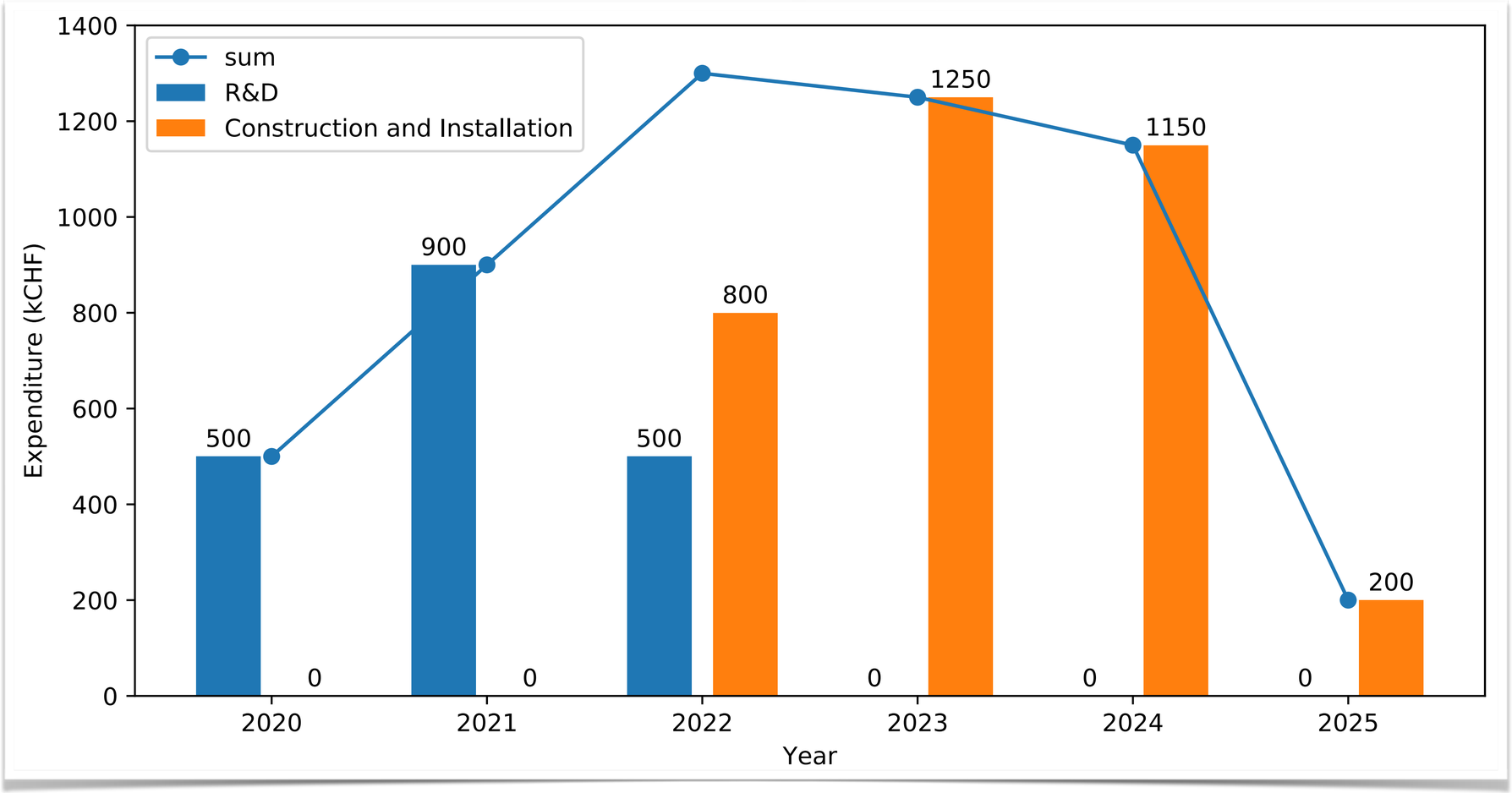
Wednesday and Thursday, 11-12 September 2019

- The **LHCC is impressed** by the new concept for the ITS3 with significantly reduced material budget, recognises the physics case presented in the LoI and in the dedicated ITS3 session and appreciates the on-going simulations on various physics channels to further demonstrate the expected gain from better resolution and efficiency at low transverse momentum. The **LHCC endorses** the plan of ALICE to carry out the necessary R&D studies to demonstrate the technical feasibility of this upgrade project. A TDR to be submitted on a timescale compatible with installation in LS3 will have to include in addition a comprehensive study of its physics gains with respect to the ITS2 detector.

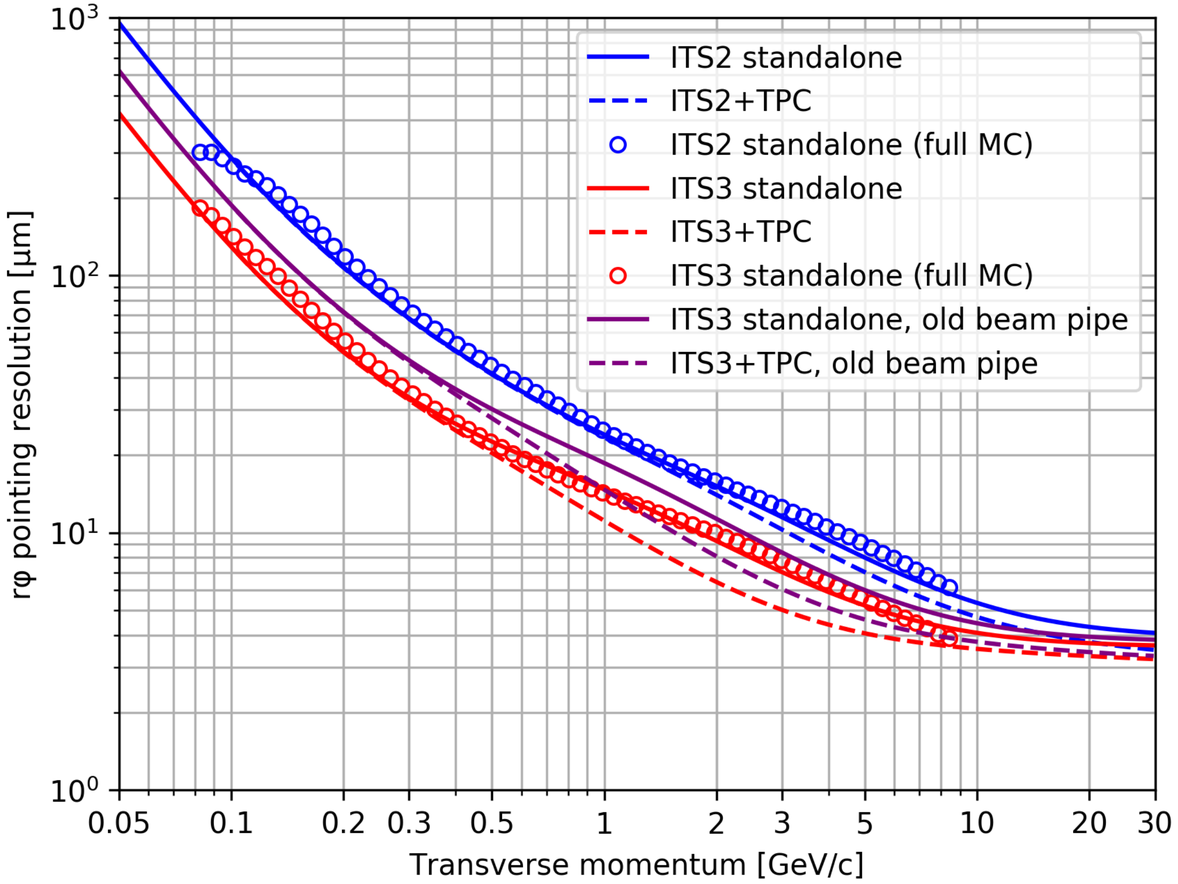
Chip specifications

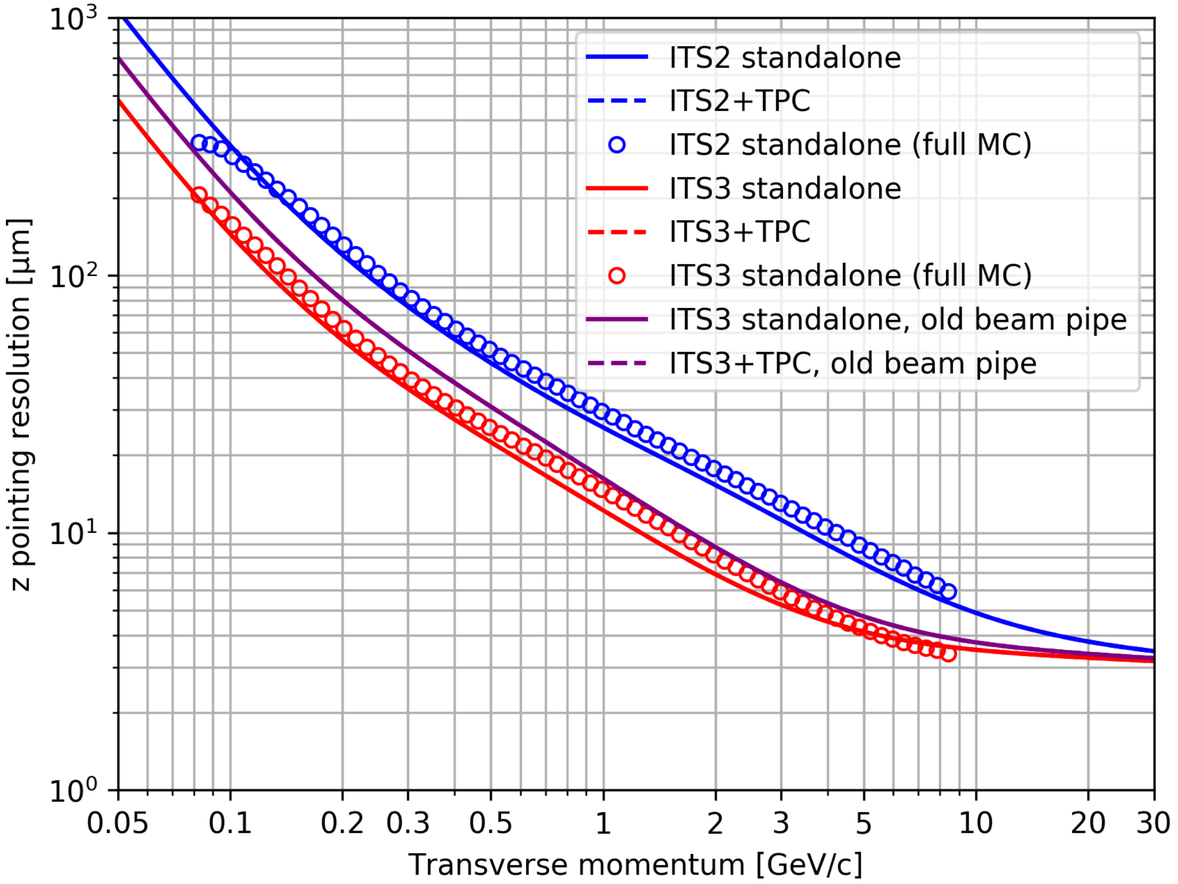
Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 µm	20-40 µm
Pixel size	27 x 29 µm	O(10 x 10 µm)
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 µs	~ 200 ns
Time resolution	~ 1 µs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm^2	100 MHz/cm^2
Max particle readout rate	10 MHz/cm^2	100 MHz/cm^2
Power Consumption	40 mW/cm^2	< 20 mW/cm^2 (pixel matrix)
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10^{-7} event/pixel	< 10^{-7} event/pixel
NIEL radiation tolerance	~3 x 10^{13} 1 MeV n_{eq}/cm^2	10^{14} 1 MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10 MRad

Spending profile

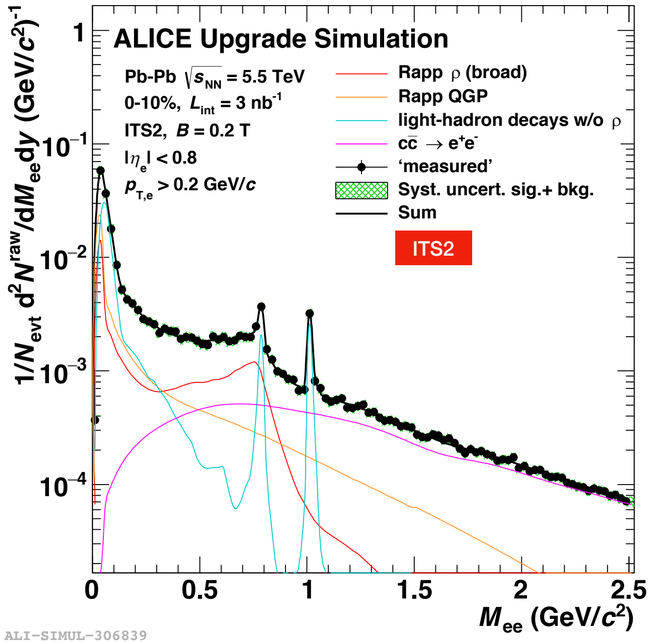


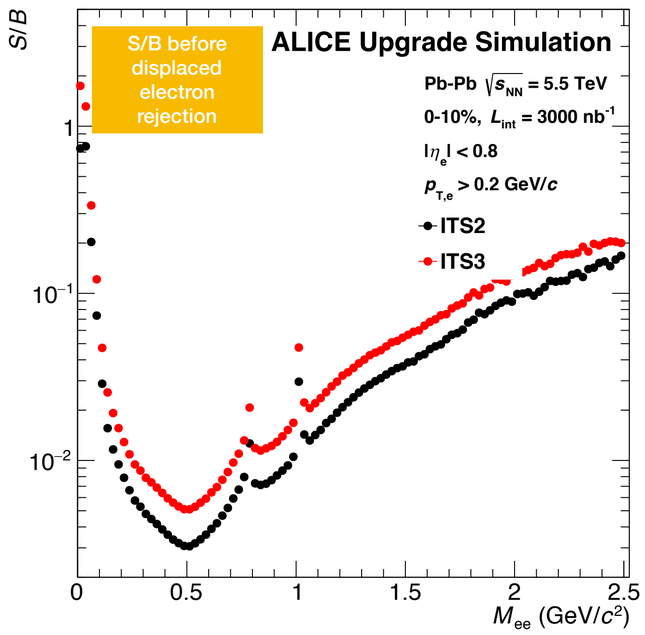
Old beam pipe, new ITS





Low-mass di-leptons



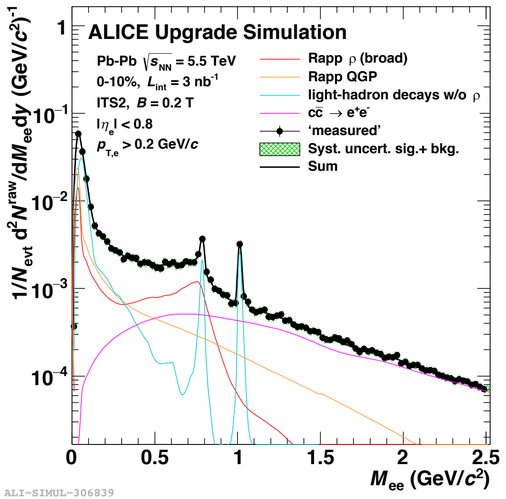


- background: all pairs of particles,
- dominated by conversions, i.e. material
- reduction by 50% due to lower material

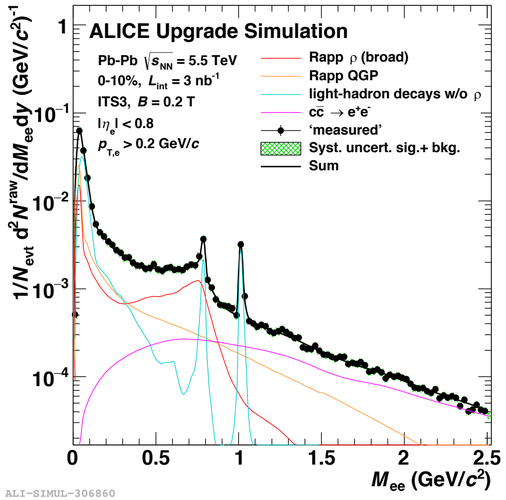
Low-mass di-leptons (2)

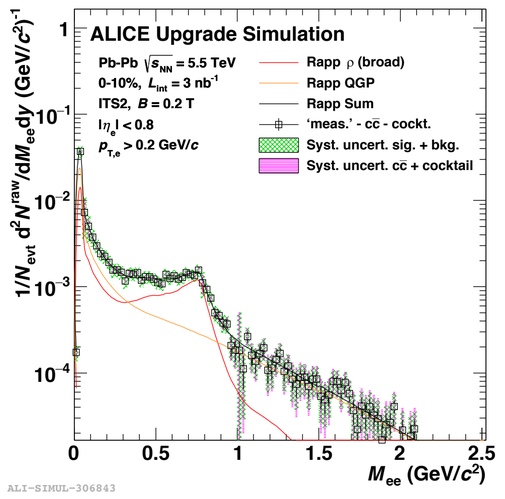
Signals

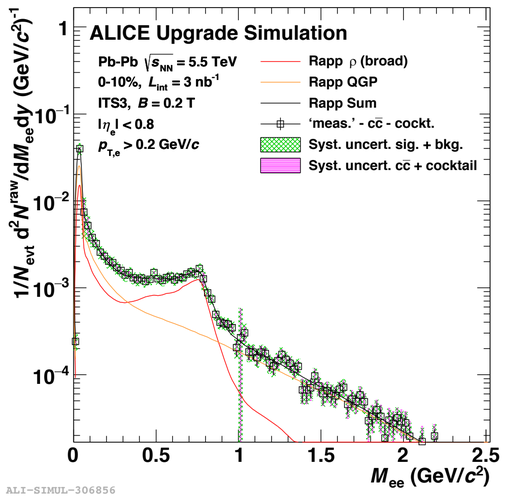
ITS2



ITS3







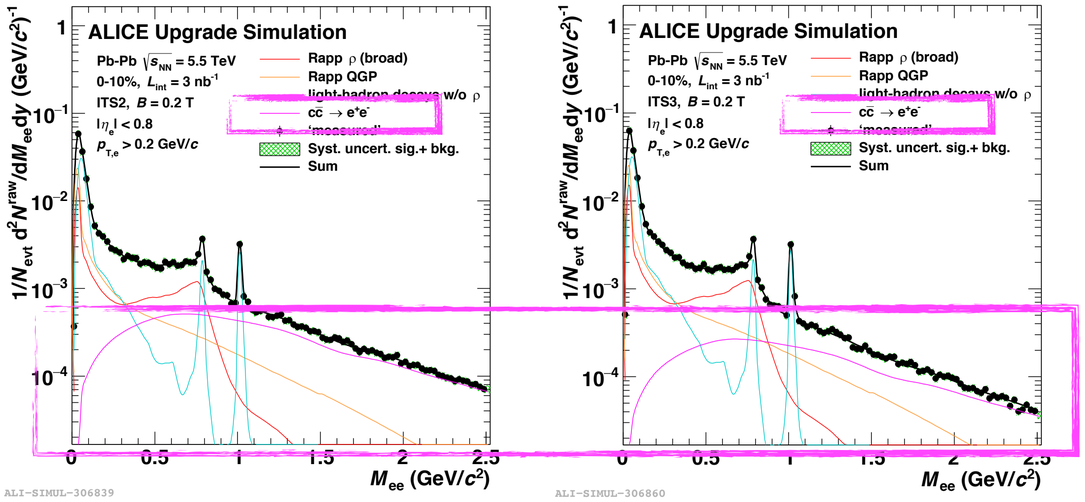
- In addition benefit from better reconstruction of of charm

T(QGP)	stat. err.	sys. err. (bkg)	sys. err. (charm)
ITS3 / ITS2	1/1.3	1/2	1/2

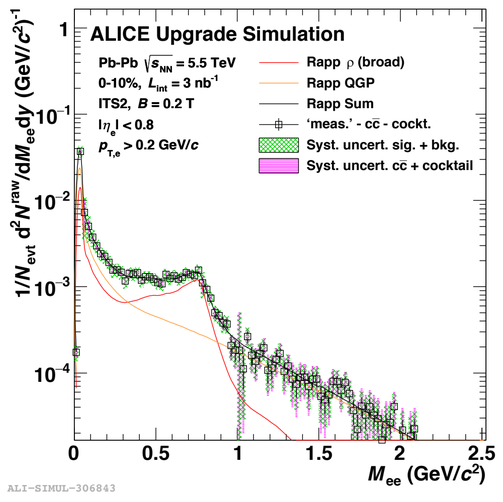
Low-mass di-leptons (2)

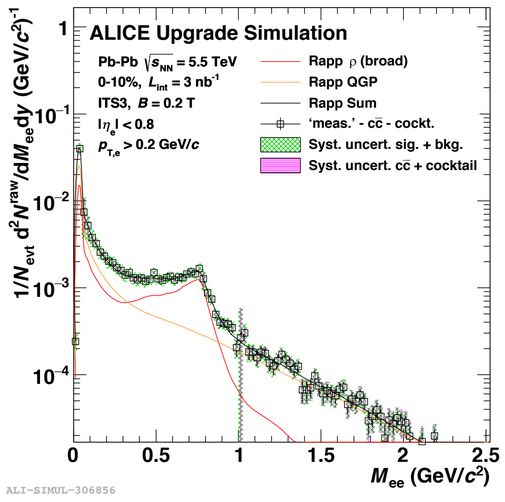
Signals

ITS2



ITS3





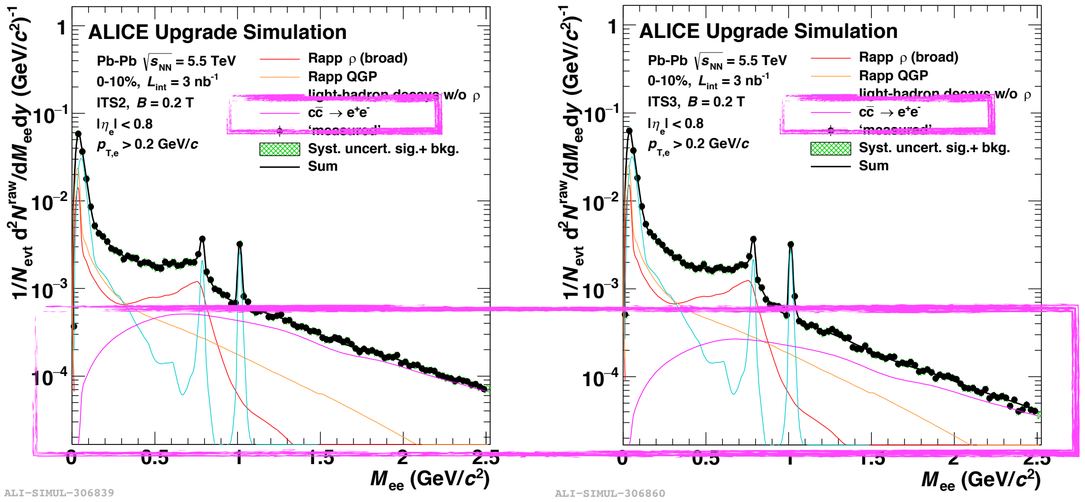
- In addition benefit from better reconstruction of of charm
- (Unidentified) charm background is reduced by 50%

T(QGP)	stat. err.	sys. err. (bkg)	sys. err. (charm)
ITS3 / ITS2	1/1.3	1/2	1/2

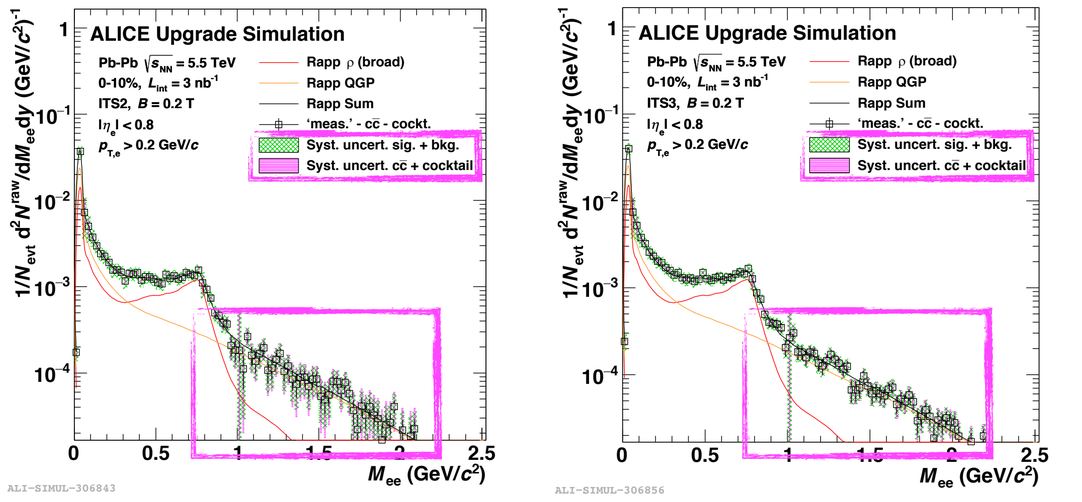
Low-mass di-leptons (2)

Signals

ITS2



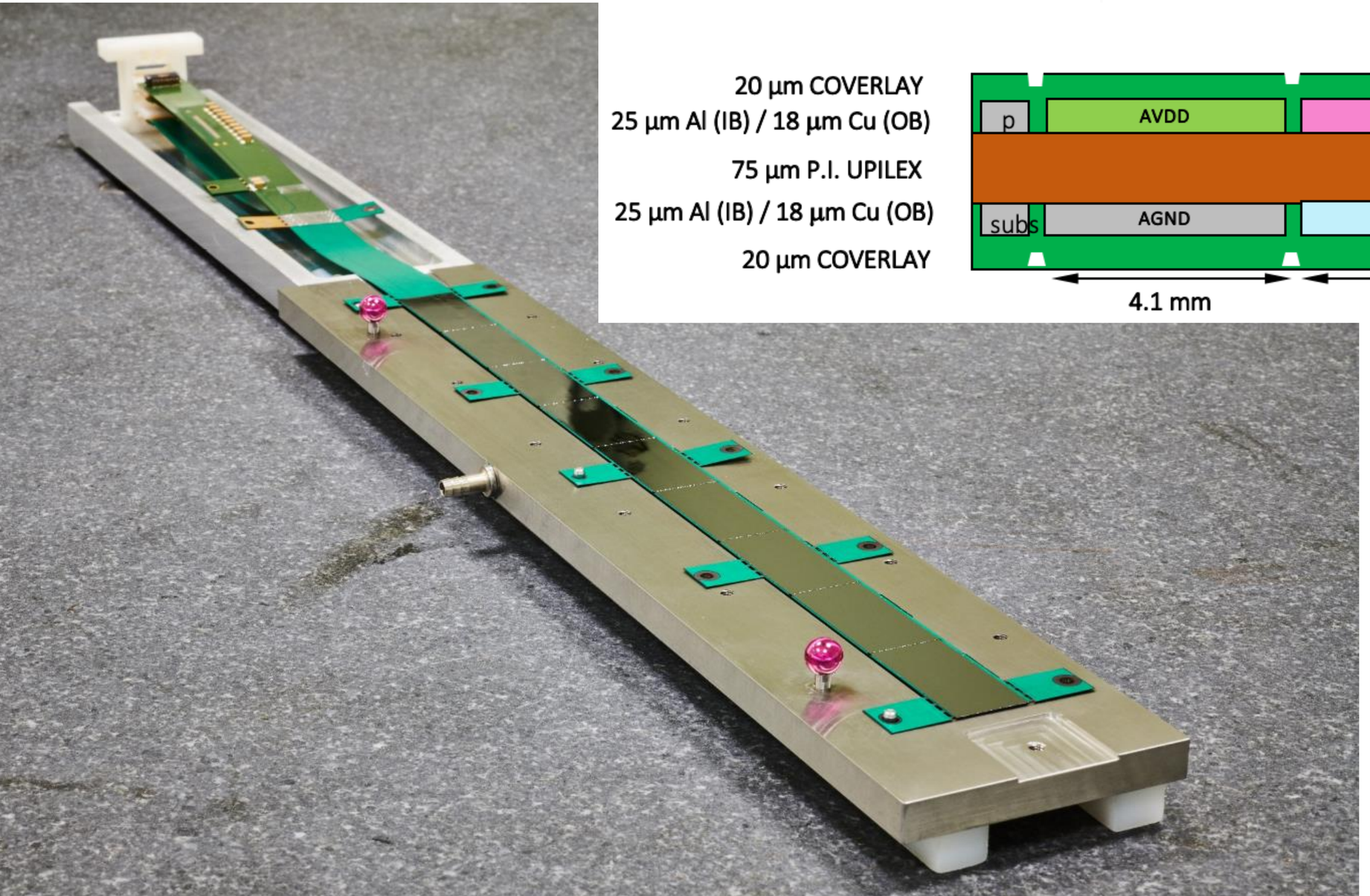
ITS3



- In addition benefit from better reconstruction of of charm
- (Unidentified) charm background is reduced by 50%
- Temperature fit:
  - $\mathrm{d}N_{ee}/\mathrm{d}M_{ee} \propto M_{ee}^{3/2} \exp(-M_{ee}/T_{fit})$
  - Systematic uncertainties of temperature fit reduced significantly

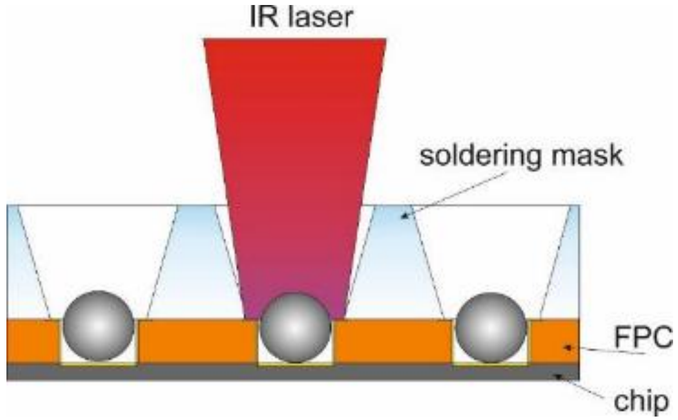
T(QGP)	stat. err.	sys. err. (bkg)	sys. err. (charm)
ITS3 / ITS2	1/1.3	1/2	1/2

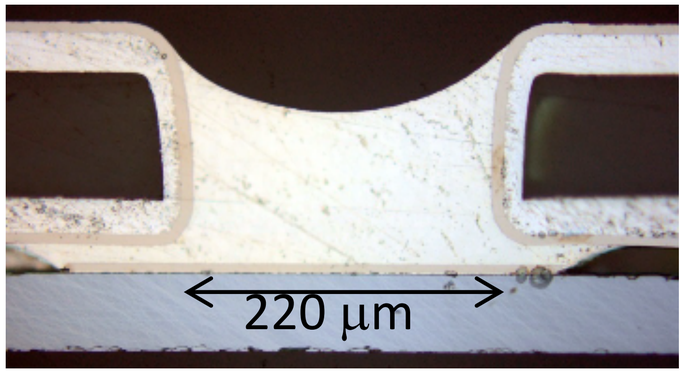
Hybrid Integrated Circuit



Interconnection technology

Selective laser soldering





Wire bodning