

Monolithic fully depleted CMOS sensors for frontier vertex and silicon detectors

VERTEX 2019

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Istituto Nazionale di Fisica Nucleare

Manuel Da Rocha Rolo

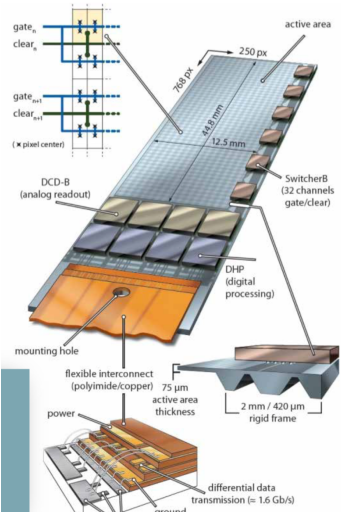
Outline

- Trends on Monolithic Active Pixel Sensors for HEP
- Boundary conditions on the use of DMAPS for future Leptonic Colliders
- ARCADIA: design and characterisation program for CMOS DMAPS

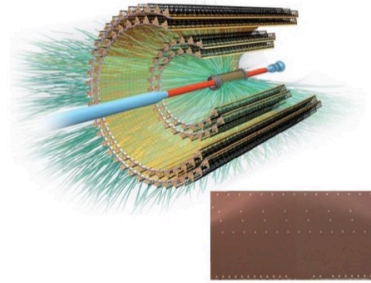
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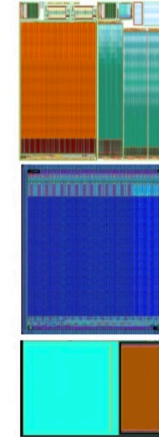
MAPS: The Evolution of the Species



ULTIMATE in STAR
IPHC Strasbourg
First HEP MAPS system

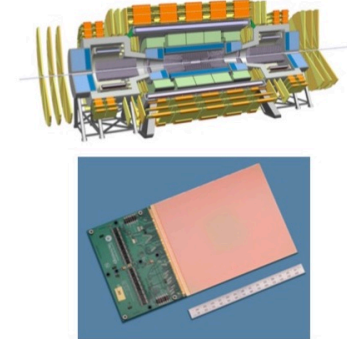


ALPIDE in ALICE
First MAPS with sparse readout similar to hybrid sensors
Chip-to-chip communication for data aggregation



ATLAS CMOS
Depleted radiation hard MAPS with:
Sparse readout
Chip-to-chip communication
Serial power

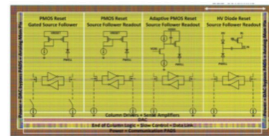
W. Snoeys, TWEPP2018



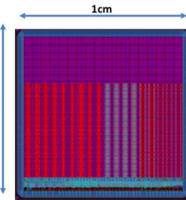
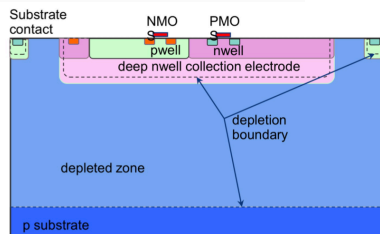
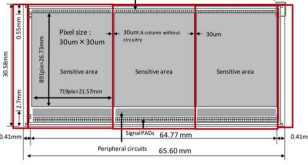
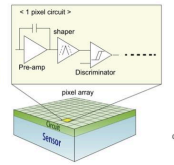
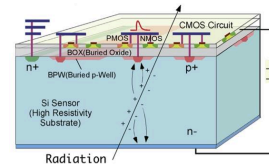
FCC, CLIC, ...
Large stitched fast radiation hard MAPS with:
Sparse readout
Chip-to-chip communication
Serial power



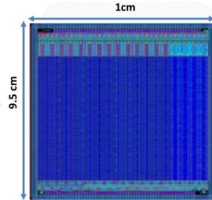
MALTA: 20 x 20 mm



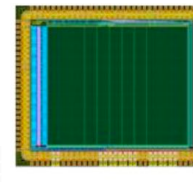
TJ-Monopix: 20 x 10 mm



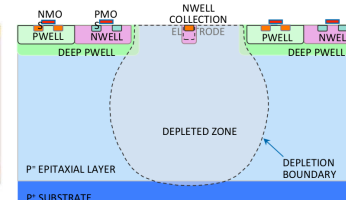
LF-CPIX (Demonstrator)



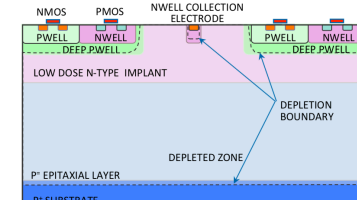
LF-Monopix (monolithic FE-14)



JadePix2 (IHEP)
3 × 3.3 mm²

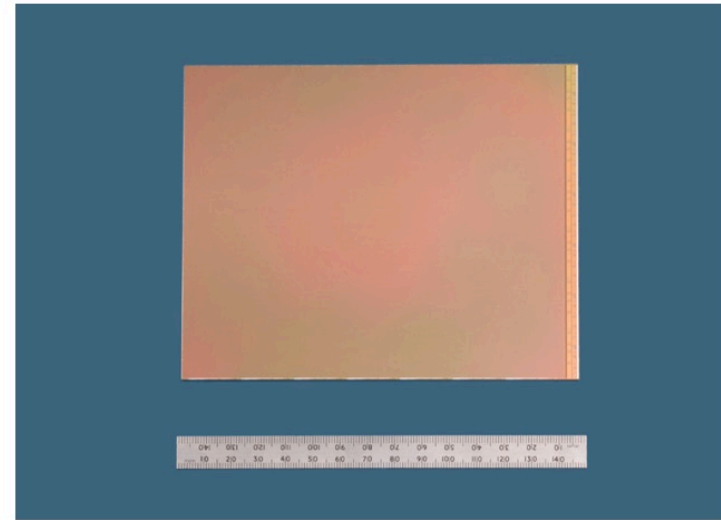
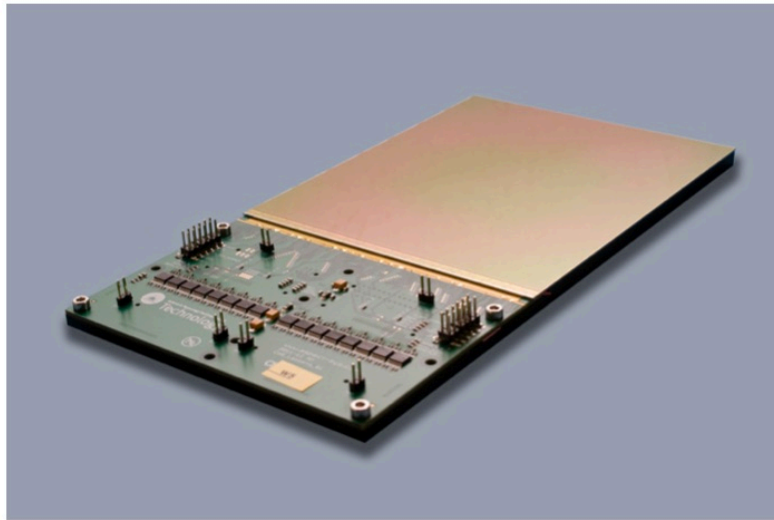


Standard: no full depletion



Modified: full depletion, better radiation tolerance

Trending up: Bigger, Stitched Silicon



- * Example of a wafer-scale imaging sensor chip for X-Ray applications developed at RAL (UK)
- * 139.2 mm x 120 mm CIS, abutment 2x2 allows for a **278.4 mm x 240 mm** active area!
- * Towerjazz 180nm on 200 mm (8") wafers, 1 sensor per wafer

- ▶ Paves the way for *all-silicon CMOS active interposers*
 - ✓ substrate handles signal, power and data interconnects
- ▶ particularly interesting assuming 12" wafers

Trending up: Thinner Silicon

Technology:

- Course + fine grinding
- Critical: thinning damage, impact on devices

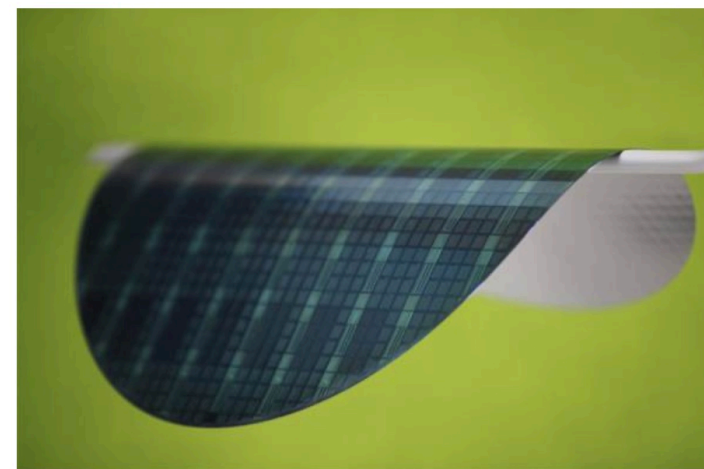
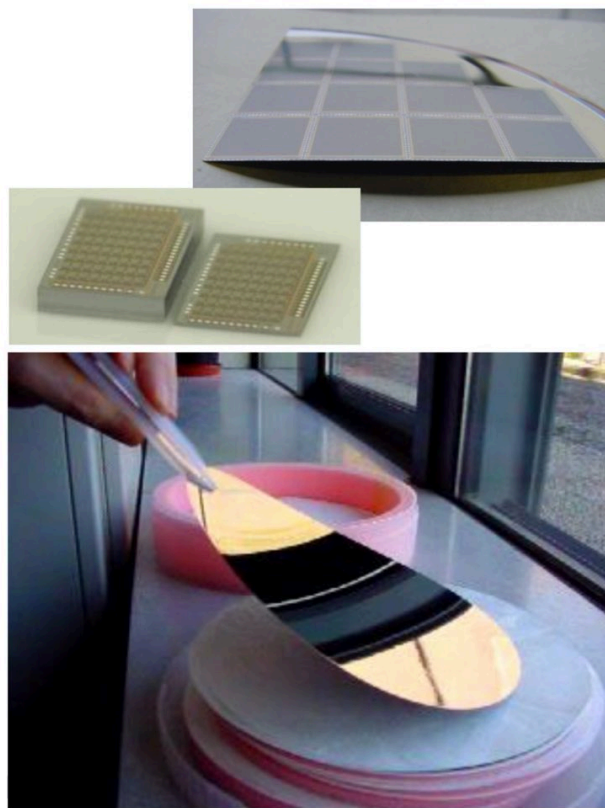
Wafer handling:

- Very thin wafers (< 100 μm): use of carrier wafers and temporary wafer (de-)bonding technology

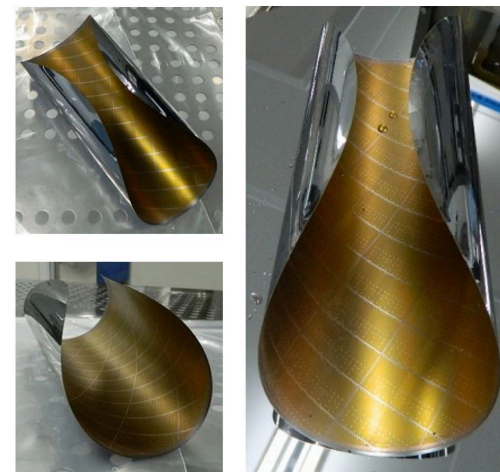
IMEC results:

- Thinning down to 15 μm
- Total thickness variation $\sim 2 \mu\text{m}$ on 200 mm wafer

P. De Moor (IMEC)



50 μm thin 300 mm Silicon Interposer Wafer with Cu-RDL metallisation. Source: Fraunhofer IZM



Magnus Mager,
this morning at VERTEX2019

* **Wafer-scale ultra-thin (< 20 μm) stitched MAPS could bend into a cylindrical mechanically stable self-supporting shape:**

purely Si based collider detector for tracking and PID with a VERTEX with an unprecedented low material budget of < 0.05 % X_0 per layer

Depleted MAPS for Future Detectors

	RHIC STAR	LHC - ALICE ITS	CLIC	HL-LHC Outer Pixel	HL-LHC Inner Pixel	FCC pp
NIEL [n_{eq}/cm^2]	10^{12}	10^{13}	$<10^{12}$	10^{15}	10^{16}	$10^{15}-10^{17}$
TID	0.2Mrad	<3 Mrad	<1 Mrad	80 Mrad	2x500Mrad	>1 Grad
Hit rate [MHz/cm ²]	0.4	10	<0.3	100-200	2000	200-20000

- Hit rate and radiation hardness for Frontier Detectors could **require improvements of ~2 orders of magnitude** in respect to the state-of-the-art technology

- * Charge collection by drift: faster signals, better radiation hardness
- * New architectures for higher event rate capability
- * Advanced integration and interconnect technology for large sensor area and lightweight modules

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- ***Boundary conditions on the use of DMAPS for future Leptonic Colliders***
- ARCADIA: design and characterisation program for CMOS DMAPS

Setting the stage... for leptonic colliders



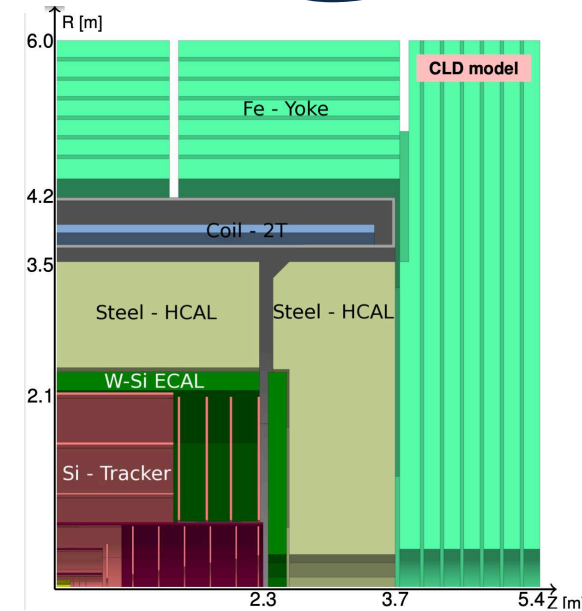
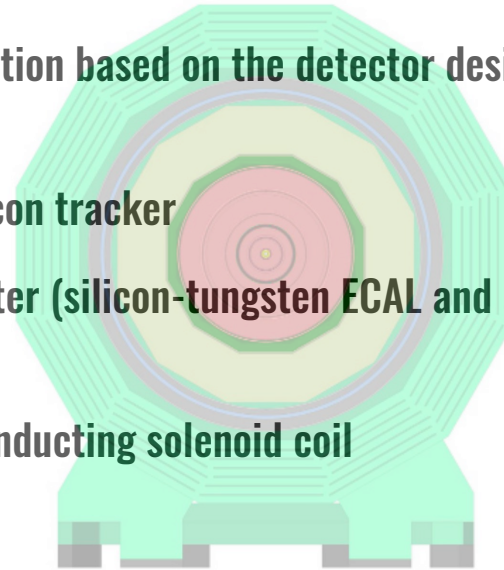
The exploitation of the physics reach at the next generation **electron-positron colliders** requires outstanding flavour tagging performance with a precise determination of the track parameters of charged particles very close to the IP → reconstruction of the displaced decay vertices of short-lived particles.

Impact on the vertex detector characteristics:

- * state-of-the-art **granularity** for resolutions at the few micron level shall be guaranteed while preserving a high event rate capability;
- * **minimum multiple scattering** at the innermost radius calls for a material budget at the level of 0.15% X0 per layer;
- * “compact” detectors requires **advanced integration and packaging technologies**, innovative **cooling** and **assembly** solutions.

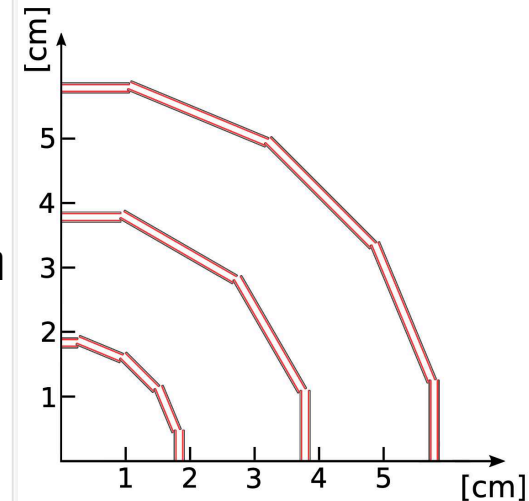
CLD - a detector concept for FCC-ee

- * “CLIC-Like Detector”: consolidated option based on the detector design developed for CLIC
- * silicon pixel vertex detector and a silicon tracker
- * 3D-imaging high-granularity calorimeter (silicon-tungsten ECAL and a scintillator-steel HCAL)
- * surrounded by a conventional superconducting solenoid coil



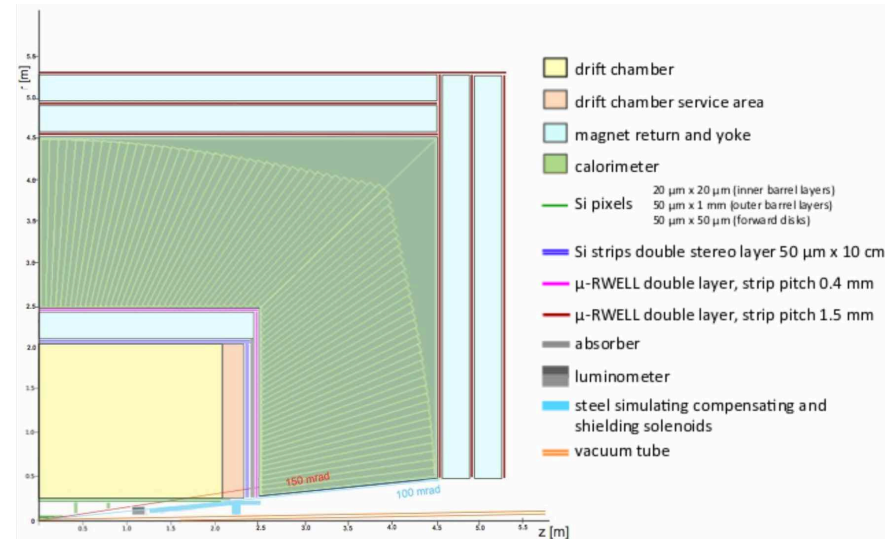
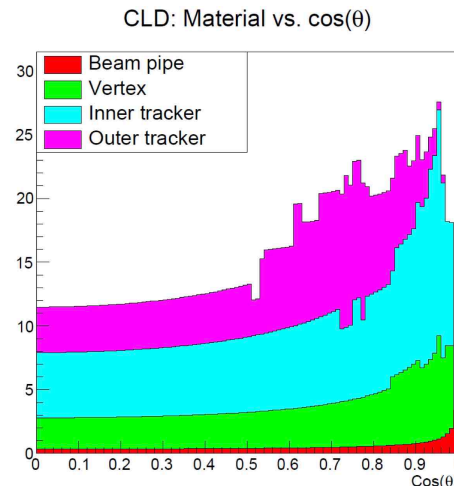
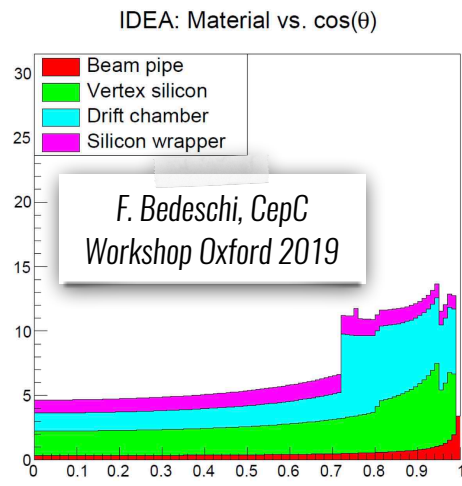
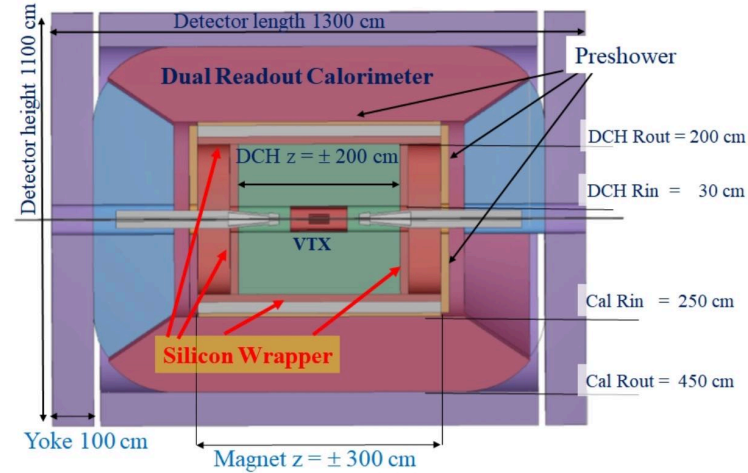
Vertex Detector

- 3 double layers (barrel), 3 double disks (forward)
- double layer includes 2 sensitive layers on a common cooled support
- each layer is 0.63% X_0 (barrel), 0.70% X_0 (forward)
- $25 \times 25 \mu\text{m}^2$ pixels, s. p. resolution 3 μm using pulse height information
- assuming ALICE ITS MAPS for VXD, material budget per double layer in the CLD vertex detector is 0.6% X_0
- The low occupancies allow for rather modest readout times

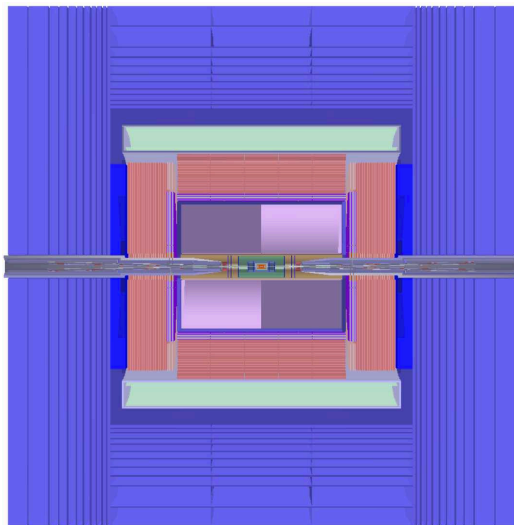


IDEA Detector - proposal for FCC-ee

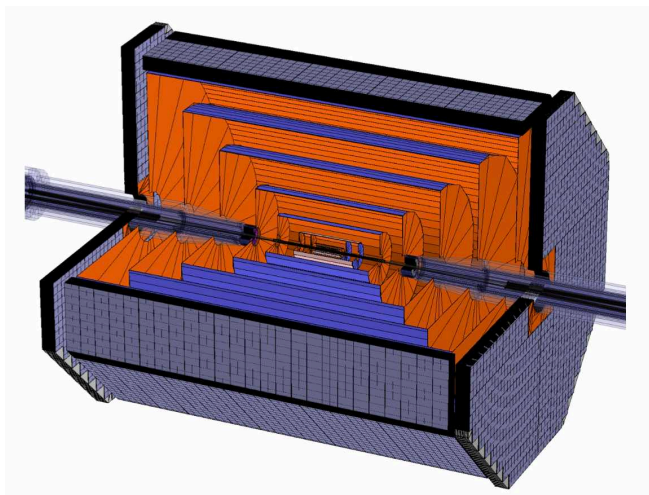
- * an “Innovative Detector for Electron-Positron Accelerators”, inspired on R&D “4th detector concept” for ILC (DREAM/RD52)
- * bolder, possibly more cost-effective, design
- * MAPS-based silicon pixel vertex detector and silicon tracker
- * ultra-light drift chamber wrapped by silicon microstrip layer
- * dual-readout calorimeter and thin, low-mass superconducting solenoid coil



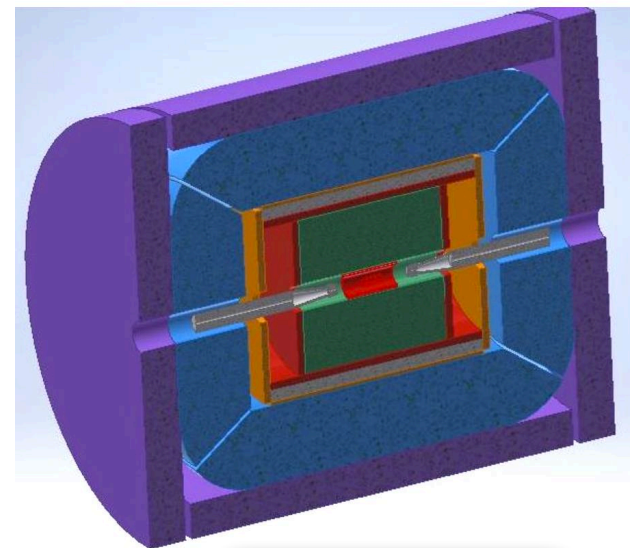
CEPC Detector Concepts



**Baseline Detector
ILD-like**



**Full Silicon
Tracker**



**IDEA
Concept**

* CEPC plans for 2 interaction points; final two detectors likely to be a mix of different options

**None of the existing CMOS sensors can fully satisfy the requirement of the high-rate CEPC
Vertex Detector (operating at the Z pole)**

*João Guimarães da Costa
CEPC Workshop Oxford, 2019*

Requirements for the CEPC Vertex (CDR)



*intrinsic single-point resolution of the vertex detector in the absence of multiple scattering (depends on the **geometry and number of layers**)*

*effects of Coulomb multiple scattering, depends on the **material budget** of the beam pipe and inner-most detector*

$$\sigma_{r\phi} = a \oplus \frac{b}{p(\text{ GeV}) \sin^{3/2} \theta}$$

impact parameter resolution \rightarrow $\sigma_{r\phi}$

a \oplus $\frac{b}{p(\text{ GeV}) \sin^{3/2} \theta}$

track momentum p polar track angle θ

Accelerator	a [μm]	b [$\mu\text{m} \cdot \text{GeV}/c$]
LEP	25	70
SLC	8	33
LHC	12	70
RHIC-II	13	19
ILC	<5	<10
CEPC	5	10

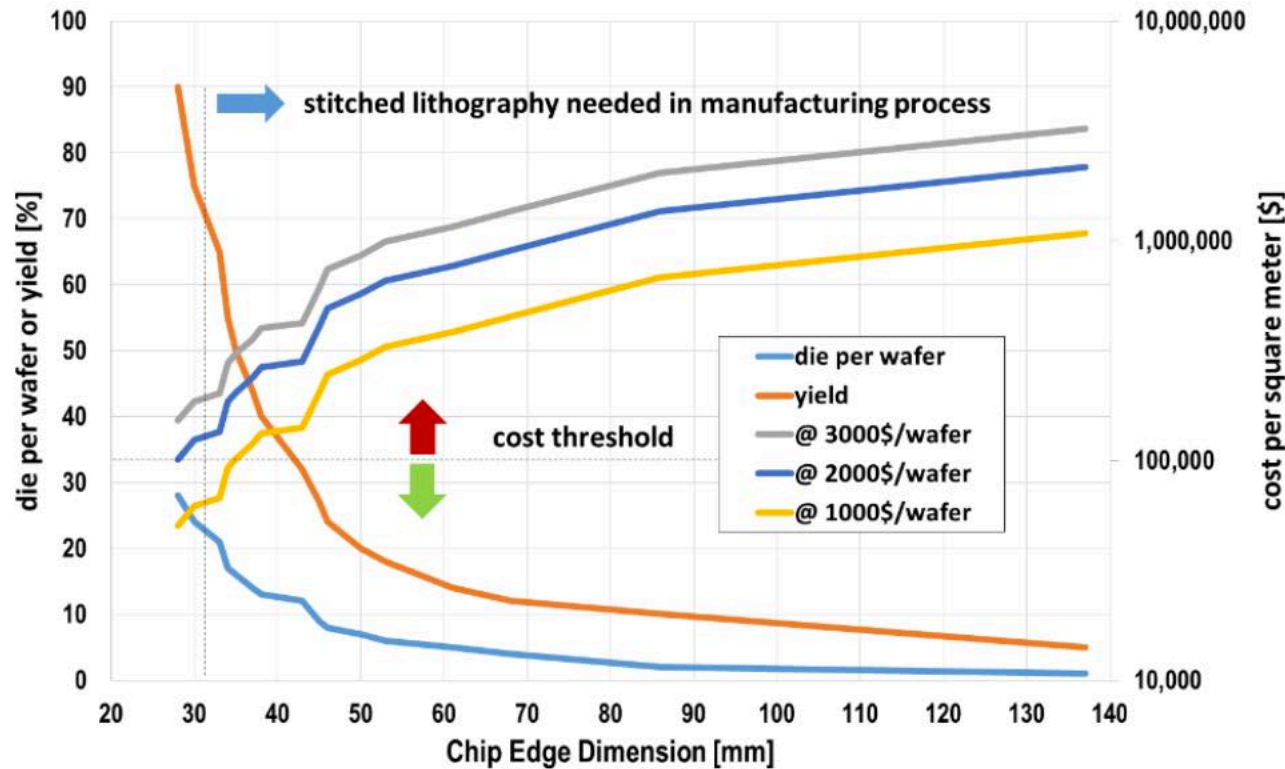
* 3 concentric cylinders of double-layer pixelated vertex detector with:

- * Single-point resolution of the first layer better than $3 \mu\text{m}$;
- * Material budget below $0.15\% X_0$ per layer;
- * Innermost tracker radius of 16 mm (material budget of $0.15\% X_0$ for the beam pipe);
- * Detector occupancy below 1%

Boundary Conditions for a CMOS APS VTX

- * excellent impact parameter resolution $O(3-5 \mu\text{m}) \rightarrow$ pixel pitch below $25 \mu\text{m}$
- * very low material budget $O(0.15\% X_0 \text{ per layer}) \rightarrow$ thin sensors, low power
 - ▶ *CepC has a bunch spacing of $0.68 \mu\text{s}$ for the Higgs factory operation, 25 ns for the Z factory operation \rightarrow no power pulsing possible (“a la ILC”)*
 - ▶ *the power consumption of the sensors and readout electronics should be kept below 20 mW/cm^2 , if the detector is to be air cooled (otherwise use silicon micro-channels)*
- * lightweight but robust support structure and related mechanics
 - ▶ *low material budget detector modules need to integrate mechanical support, power and signal connections, and have sufficient stiffness to avoid vibration.*
- * low to moderate requirements for radiation tolerance
- * moderate rate capability

Cost of a CMOS MAPS-based Silicon Tracker



Stefan Lauxtermann
(Sensor Creations)
PIXEL2018

Cost of \$100,000/m² tracking area is achievable with the following assumptions

- **> 75% Yield**
- **No stitching**
- **Wafer cost <\$2,000 (only achievable using high volume CMOS manufacturing)**

Boundary Conditions for a CMOS APS STK

- * the requirements for the **single point resolution** are a function of the **position of the tracker components**, but necessarily more relaxed than for a vertex detector;
 - ▶ *pitch below 50 μm*
 - ▶ *silicon thickness below 200 μm , needs to minimise multiple scattering*
- * considering material budget and power density, silicon strips are the natural candidate, but... a **fully-pixelated CMOS silicon tracker would allow** for:
 - ▶ better single point resolution
 - ▶ potentially **lower material budget** (CMOS wafer thinning down to 50 μm is relatively standard), **lower cost** and **high throughput** from a production of the APS silicon in a standard CMOS foundry
- * **Practical implementation:**
 - ▶ *CMOS passive strip sensors (volume, low-cost)*
 - ▶ *larger, or longer, APS pixels with ADC, zero suppression, time stamp, or*
 - ▶ *binary readout with DSP and clustering on-chip (periphery)*

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- ***ARCADIA: design and characterisation program for CMOS DMAPS***

Towards a CMOS sensor design and fabrication platform allowing for:

- * **Active sensor thickness in the range 50 μm to 500 μm or more;**
- * **Operation in full depletion with fast charge collection only by drift;**
- * **Small charge collecting electrode for optimal signal-to-noise ratio;**
- * **Scalable readout architecture with ultra-low power capability (0(10 mW/cm²));**
- * **Compatibility with standard CMOS fabrication processes: concept study with small-scale test structure (SEED), technology demonstration with large area sensors (ARCADIA)**
- * **Use of a deep sub-micron 110nm CMOS node for higher gate density**

ARCADIA (INFN CSNV Call Project)

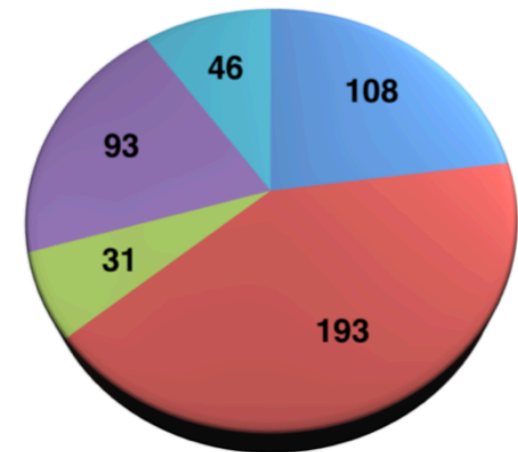
Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays



INFN - Bologna, Milano, Padova, Perugia, Pavia, TIFPA, Torino

A. Gabrielli, D. Falchieri, G. D'Amen, F. Alfonsi, N. Giangiacomi, A. Cervelli, A. Andreazza, M. Caccia, R. Santoro, A. De Angelis, P. Giubilato, S. Mattiazzo, J. Wyss, A. Candelori, R. Rando, D. Bastieri, G. Ambrosi, P. Placidi, D. Passeri, T. Croci, L. Servoli, A. Scorzoni, G. Traversi, L. Ratti, M. Pezzoli, C. Vacchi, L. Gaioni, L. Pancheri, G.-F. Dalla Betta, A. Ficorella, M. Zarghami, M. Favaro, R. Iuppa, S. B. Ricciarini, P. Zuccon, F. Nozzoli, B. Di Ruzza, E. Ricci, M. Da Rocha Rolo, R. Giampaolo, A. Rivetti, S. Beolè, R. Wheadon, F. Tosello, N. Demaria, A. Di Salvo, G. Dellacasa, J. Olave, M. Mandurrino, A. Paternò, S. Garbolino

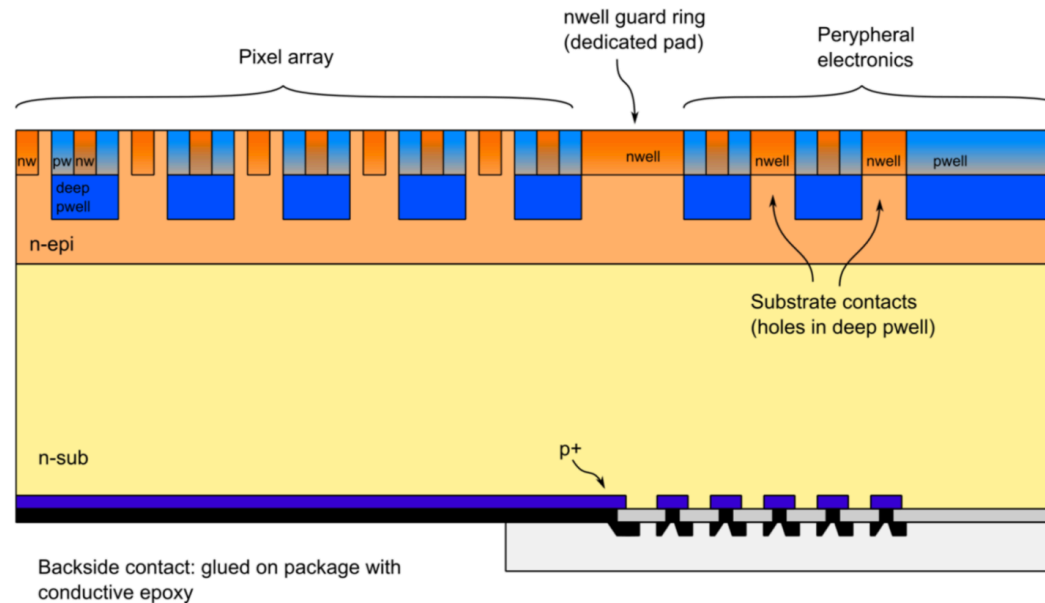
Person/month assignment per Work-Package



* 3-year 1M€ R&D project 2019-2021

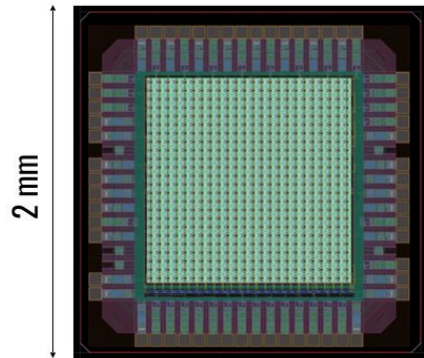
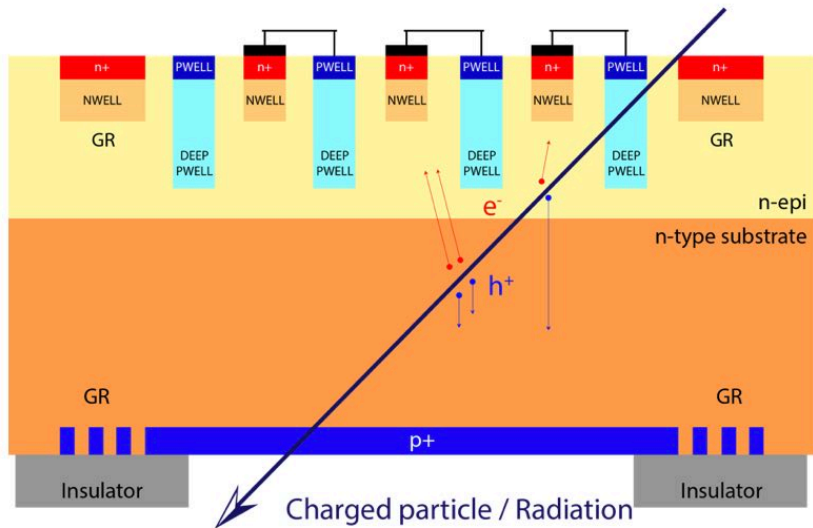
* Sensor&CMOS design, DAQ, System characterisation (medical, future colliders, space)

ARCADIA - Proposed Sensor

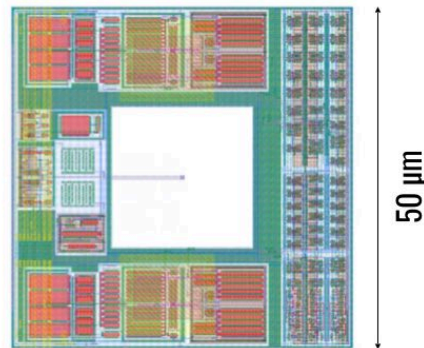


- * Technology: 110 nm CMOS CIS technology (quad-well, both PMOS and NMOS), high-resistivity bulk
- * SEED : Sensor with Embedded Electronics Development (INFN CSNV Project)
- * Backside: diode surrounded by a guard-ring
- * Custom patterned backside, process developed in collaboration with LFoundry
- * Pixel size 25 μm x 25 μm : process, back-side pattern and geometry validated in silicon (both MATISSE and pseudo-matrices, electrical, laser, radioactive source and microbeam)

Small-scale demo: MATISSE



MATISSE



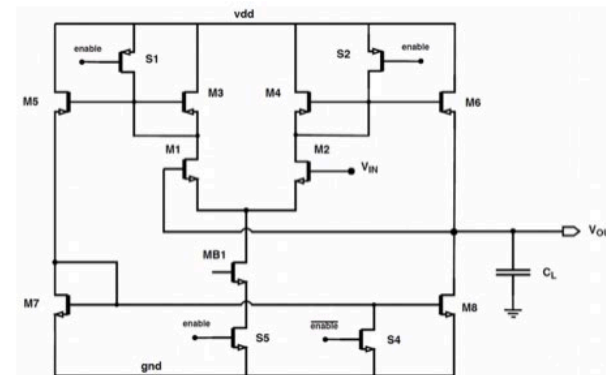
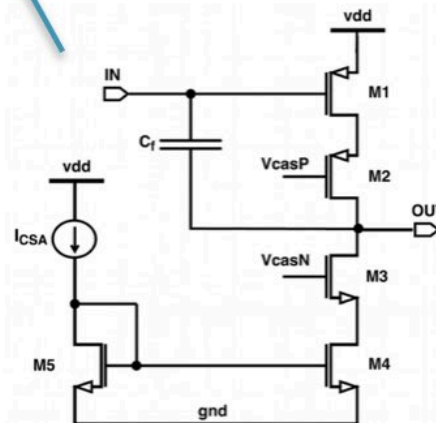
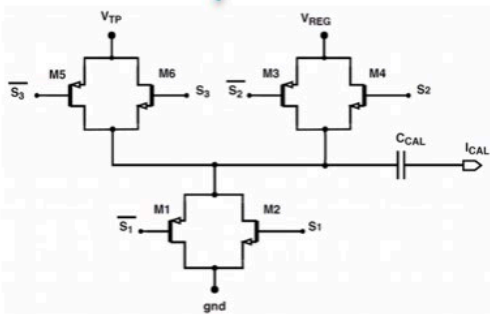
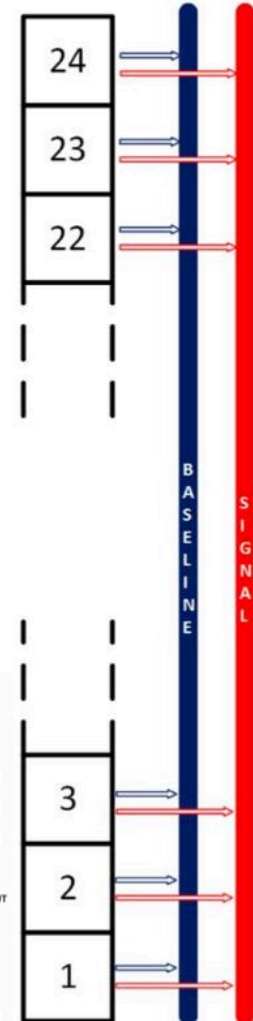
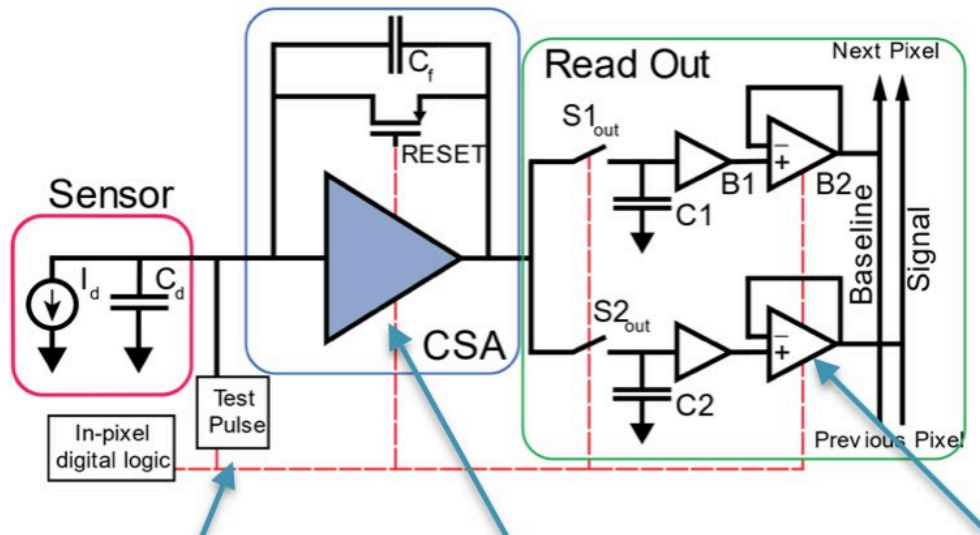
Pixel CAD Layout

PIXEL ELECTRONICS		
	DESIGN SPECS	RESULTS
Technology	CMOS 110 nm	
Voltage Supply	1.2 V	
Measurements	Hit Position	Energy Loss
Number of Channels	24 × 24	
Input Dynamic Range	Up to 24 ke ⁻	
Sensor Capacitance	~20 fF	
Analog Gain	131 mV/fC	116 mV/fC
CSA Input Common Mode Voltage	> 600 mV	
Local Memories	2 (~70 fF each)	
Noise	< 100 e ⁻	~40 e ⁻
Shutter Type	Snapshot	
Readout Type	Correlated Double Sampling	Double Sampling
Readout Speed	Up to 5 MHz	
Other Features	Internat test pulse	Mask Mode
	Baseline Regulation	

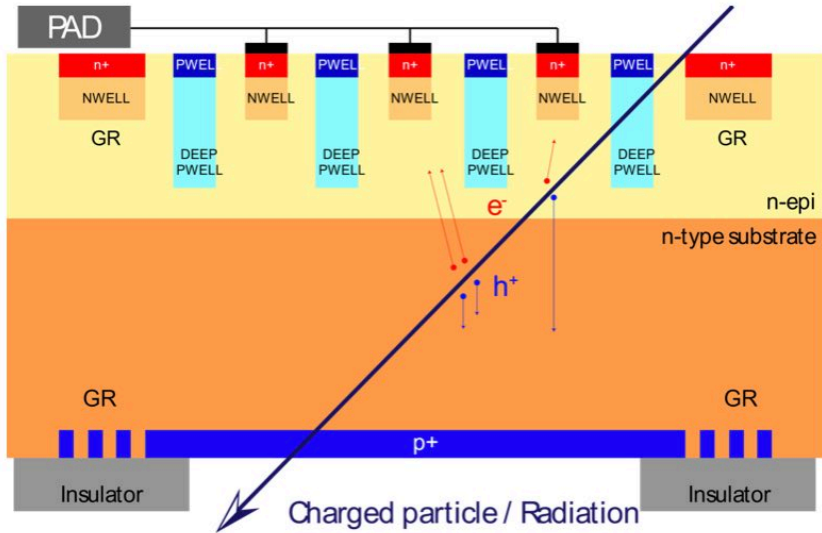
Small-scale demo: MATISSE

Charge Sensitive Amplifier
With a RESET transistor

Correlated Double Sampling

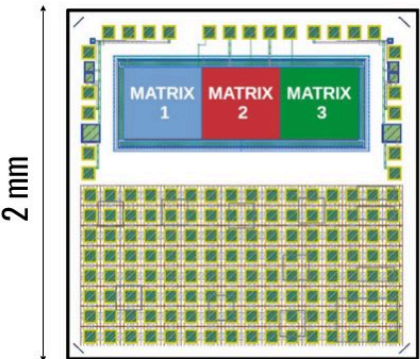


Small-scale demo: pseudo-matrices

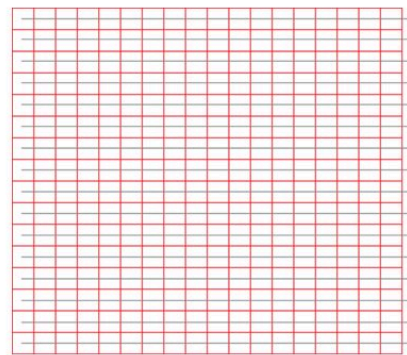


- ❑ Sensor **thicknesses**: 100 μm , 300 μm , 400 μm
- ❑ Three matrices with different **pixel sizes**: 10 μm (40 x 45), 25 μm (16 x 18) and 50 μm (8 x 9)
- ❑ Front-side **deep-pwell**, would host the CMOS electronics (no electronics on PMs)

- ❑ All the collector nodes of a matrix are **shorted** and connected to a PAD
- ❑ Each pixel is shorted using **Al metal lines** of increasing width per PM: 6, 8 and 15 μm



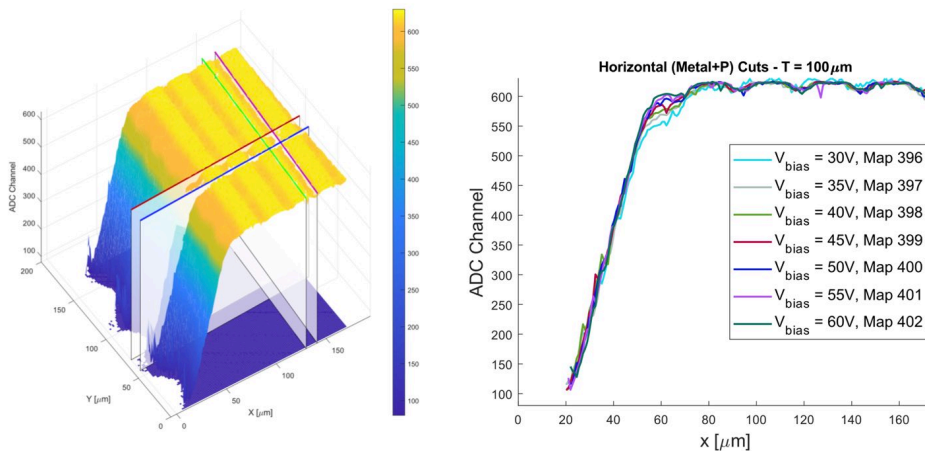
Pseudo-matrix Layout



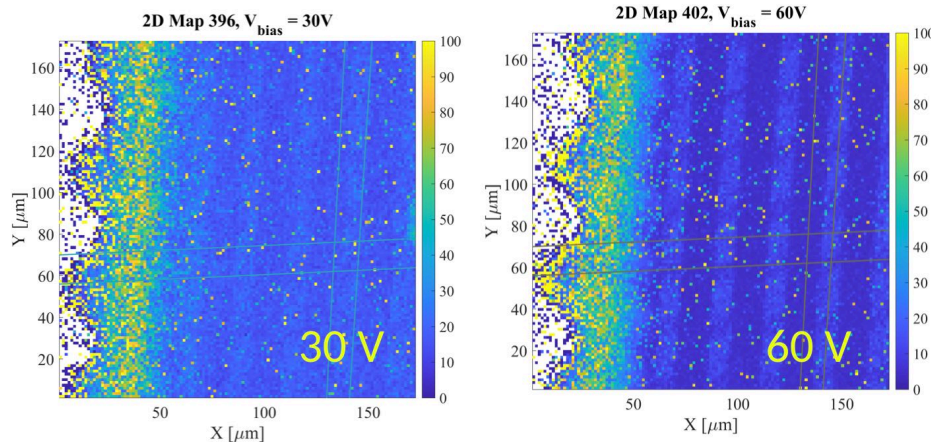
Pixel Scheme

Results in a nutshell: pseudo-matrices

Cuts along the **Metal + P** and **Metal + N** lines on the energy map with varying bias voltages show **uniform CCE** above FD with **~1.7 % loss over metals** (100 μm thick)



Standard deviation maps show the expected higher electronic noise when the sensor is not depleted (below 30 V), due to the higher top capacitance.

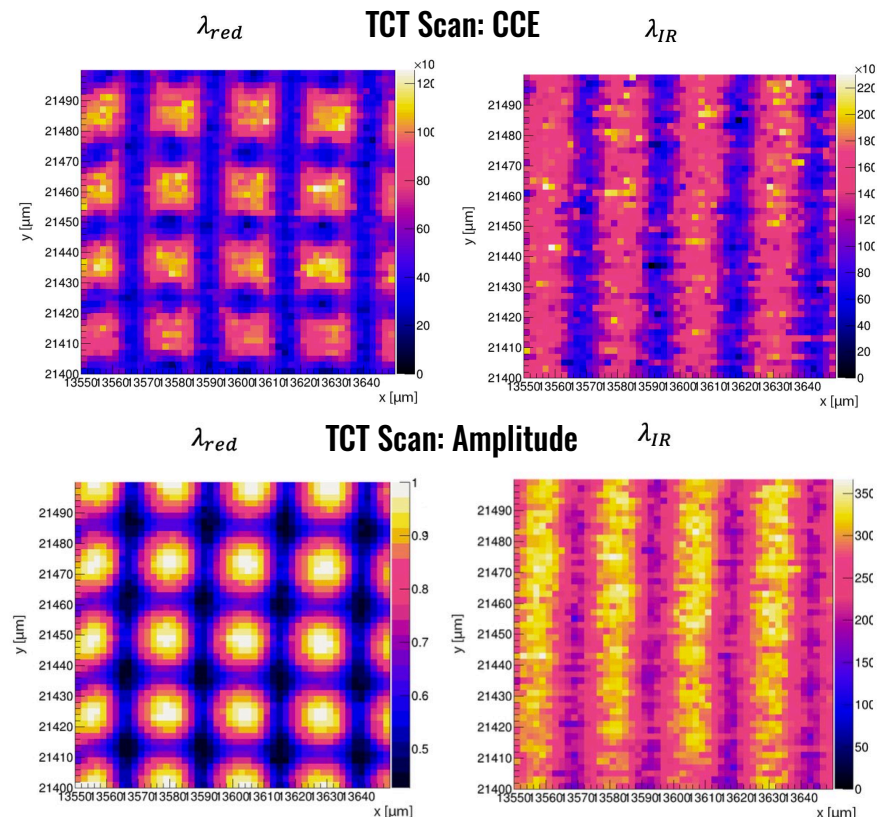


(**RUĐER BOŠKOVIĆ INSTITUTE**)* Zagreb, Croatia

- 600 keV to 2 MeV Tandetron
- TANDEM 1-6 MeV proton source
- LASER TCT laboratory

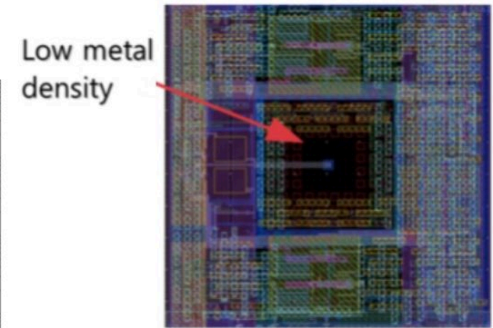
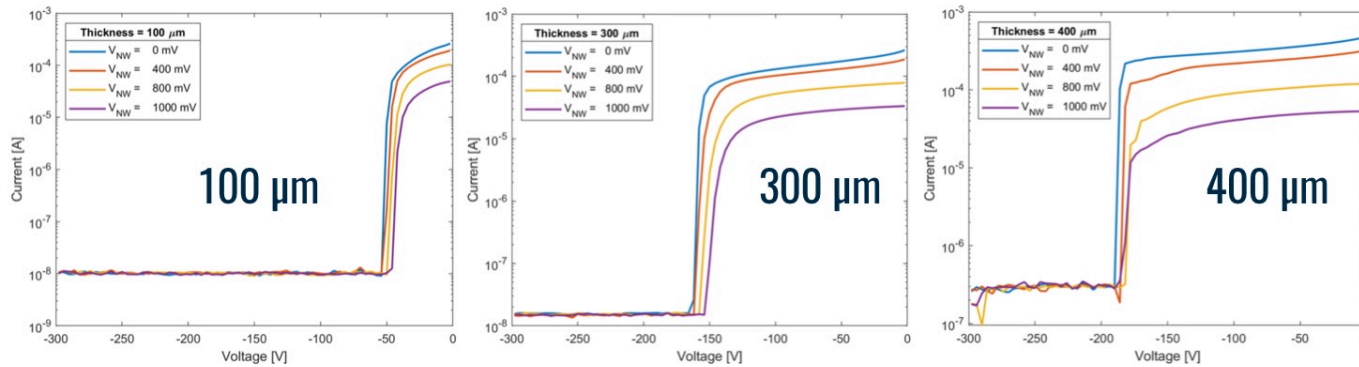


* Valery, Milko, Matti, Aneliya, Andreo, George, Milan: Thanks!



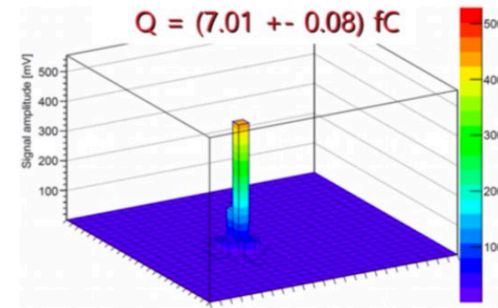
Results in a nutshell: MATISSE

Full depletion studies in 100-300-400 μm prototypes

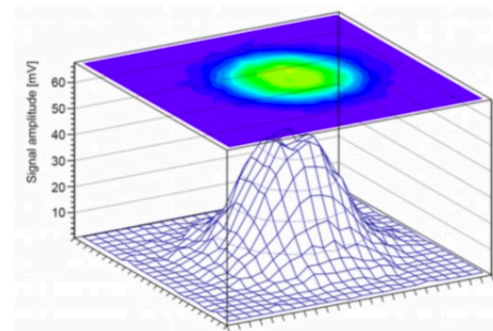


Focused pulse

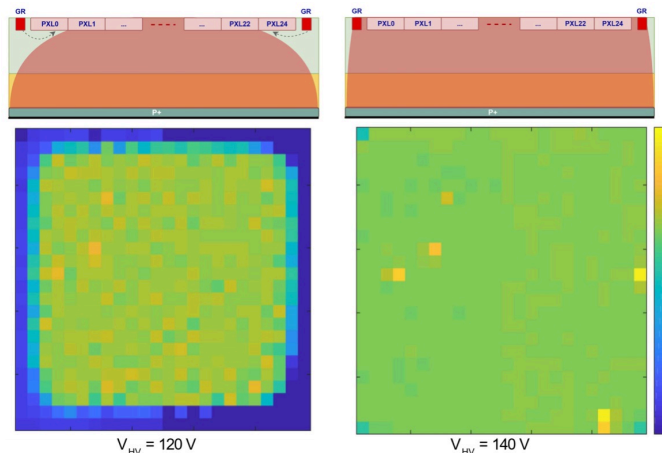
$$Q = (7.01 \pm 0.08) fC$$



Non focused pulse

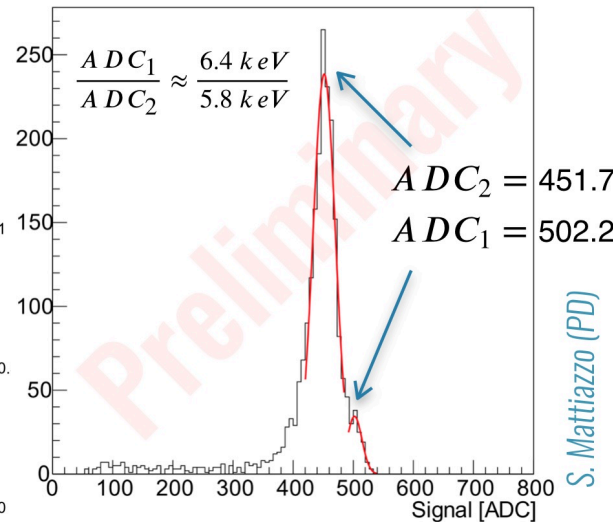


Map of pixel reset voltage (MATISSE 24x24 pixel matrix) as a function of the back-side voltage applied to the sensor. Depletion starts from the back-side.



Preliminary results with ⁵⁵Fe

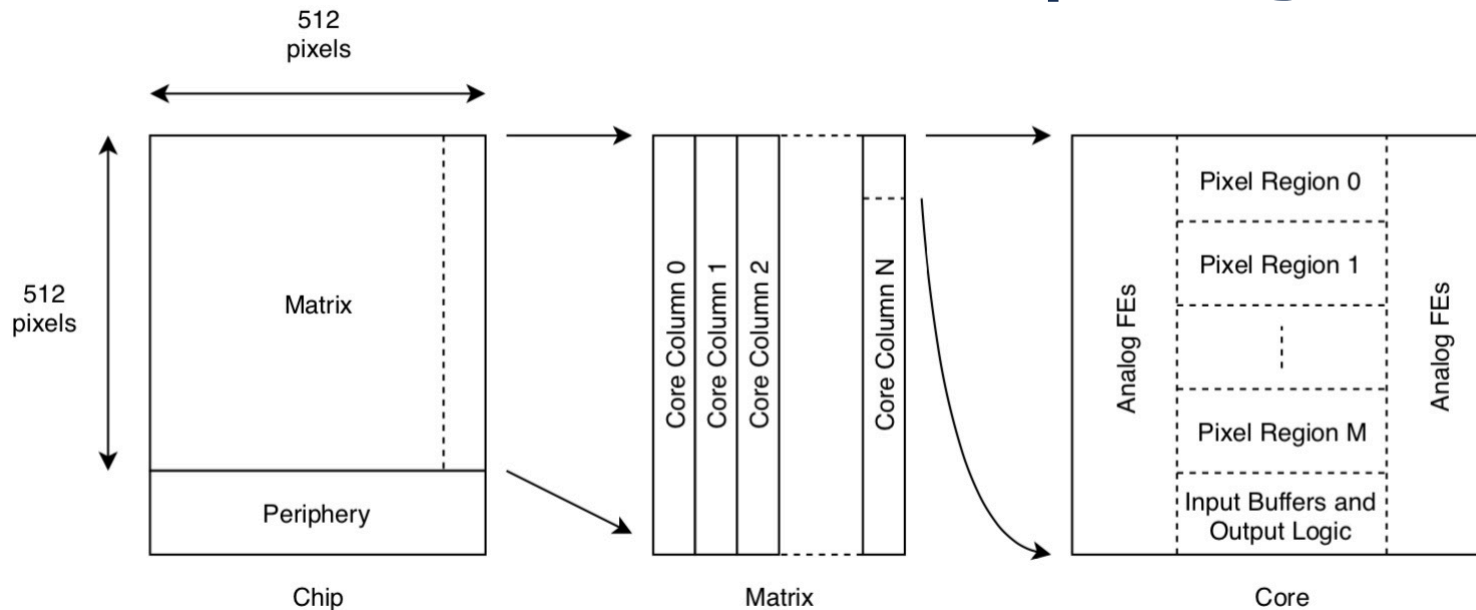
160 V, Sector 1



The ⁵⁵Fe emits monochromatic X-rays at 5.9 keV (K_α). A K_β line at 6.5 keV is also emitted with a relative probability of about 10%.

J. Olive FEE2018

ARCADIA - Demonstrator Chip Design



- * **Pixel size $25\ \mu\text{m} \times 25\ \mu\text{m}$:** process, back-side pattern and geometry validated in silicon (both MATISSE and pseudo-matrices, electrical, laser, radioactive source and microbeam)
- * **Matrix core 512×512 , “side-abutable”** to accommodate a **1024×512 silicon active area** ($2.56 \times 1.28\ \text{cm}^2$). Matrix and EoC architecture, data links and payload ID: scalable to **2048×2048** ⁽¹⁾
- * **Triggerless binary data readout, event rate up to $10\ \text{MHz}/\text{cm}^2$**
- * **“Strip-like” data-compressed column configuration**

⁽¹⁾ 1D and 2D stitching available at LFoundry

ARCADIA: ongoing activities

01/2019

01/2022

- * TCAD 2D/3D sensor simulation: geometry, p-well spacing, node capacitance, transient
- * CMOS Analogue IP block design: continuous and discrete-time VFE design; 12-bit SAR ADC IP-core, custom LVDS Tx/Rx: LF11is prototyping run September 2019

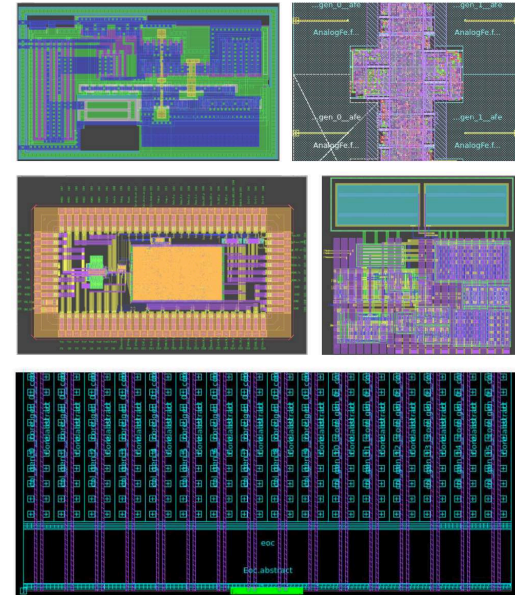
- * CMOS Digital IP block design and Chip Integration:

- ▶ SPI and Serialiser (8b/10b) soft-IP Cores 110nm ready
- ▶ PnR of full double-column, full-matrix integration ongoing

- * Data acquisition: started development of DAQ for the full-chip

- * Characterisation: laser and microbeam tests with 100-300 μm

pseudo-matrices @RBI (Zagreb), tests with Fe^{55} , new laser test setup (spot size 8 μm) under construction



Engineering run (dedicated front/back-side maskset): mid-2020

Future Roadmap and Perspective



01/2019

01/2022



- * ARCADIA will build a **design, characterisation and production framework** for fully-depleted MAPS in a CMOS commercial foundry
- * design of 2D-stitched **wafer-scale** demonstrators, **scalable DAQs**, **mechanics** and **cooling** for large systems, flexible ultra-thinned **silicon handling and assembling**, integration of **system-grade design**:
 - ▶ Eol for AIDA++: **INFN** (IT), **PSI+ETH+UZH** (CH), **Uni. Oxford** (UK), **IHEP** (CN)
- * Future collaborations, funding and resources will allow for the development of application-specific **wafer-scale sensors** for frontier detectors, medical, space and industrial applications

Monolithic fully depleted CMOS sensors for frontier vertex and silicon detectors

Thank You for your time !



Istituto Nazionale di Fisica Nucleare