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3D integration of readout chip for the SOI pixel sensors

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SOI is a CMOS LSI technology to insulate each MOSFET by using a thin oxide layer in the silicon wafer, allowing high-performance CMOS circuit because of the low parasitic capacitance. The SOI pixel sensor utilizes the silicon wafer as the radiation sensor. Because of the small detector capacitance and the industry-standard CMOS technology, high-performance pixel sensors can be developed.
In recent high-luminosity collider experiments, huge number of signal and background tracks enter the pixel detector. We have to implement a complex circuit in each pixel to reduce the hits to be read out. There is also demands to keep or reduce the pixel size from the physics view point.
A solution to this issue is the 3D integration of readout chip, where, the additional CMOS chip is produced, integrated to the sensor chip, and the circuit signals are connected pixel by pixel. With this technology, the functions of each pixel can be improved significantly. The first SOI pixel sensor with 3D integration was submitted in 2018 and the evaluation of the chip are in progress.

In this presentation, the 3D integration technology for the pixel sensors is reviewed briefly. Then the R&D status of the SOI 3D pixel sensor will be discussed.

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