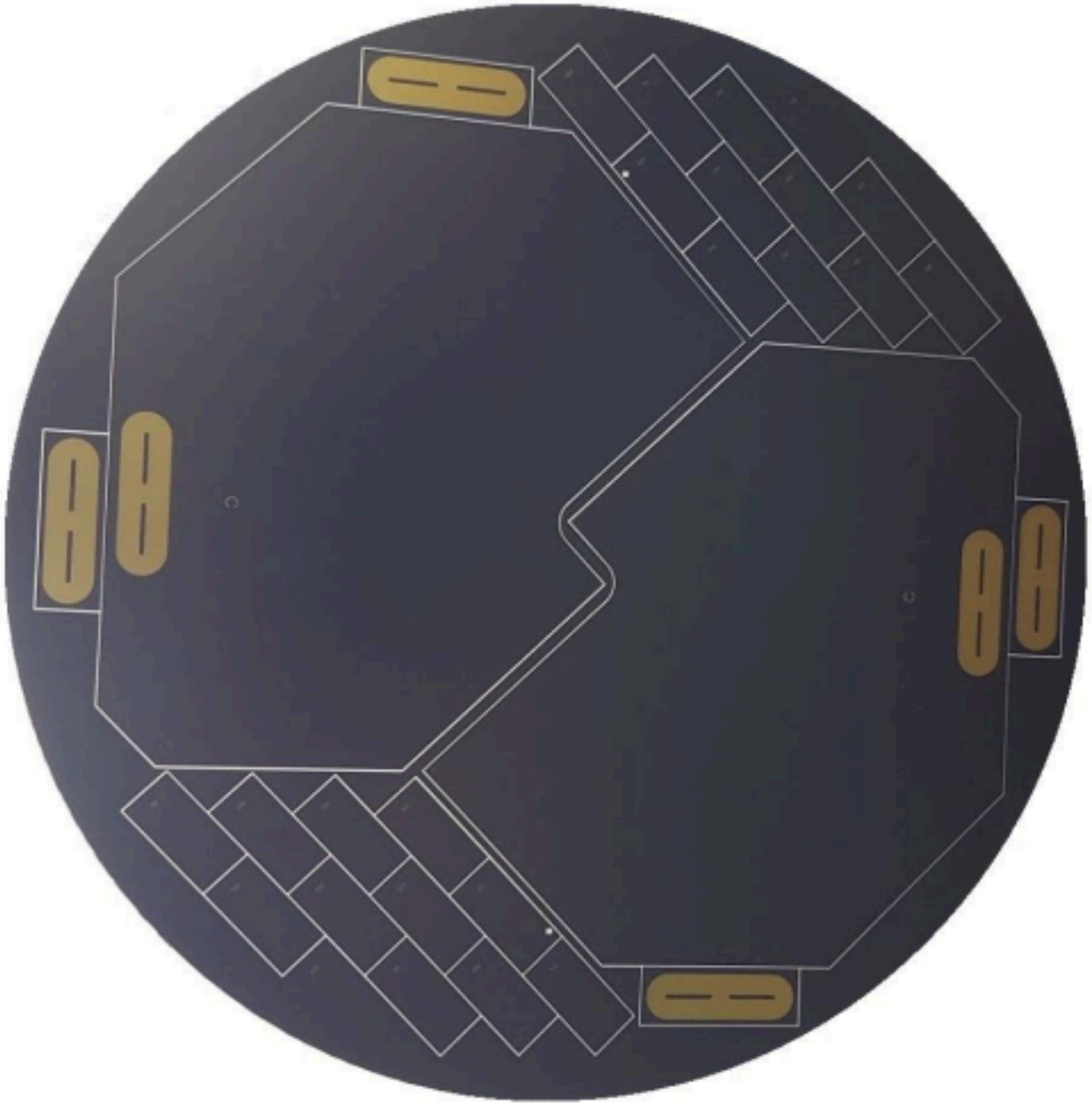
Micro-channels cooling for the LHCb VELO pixel upgrade

C. Bertella (CERN), *on behalf of LHCb VELO group*

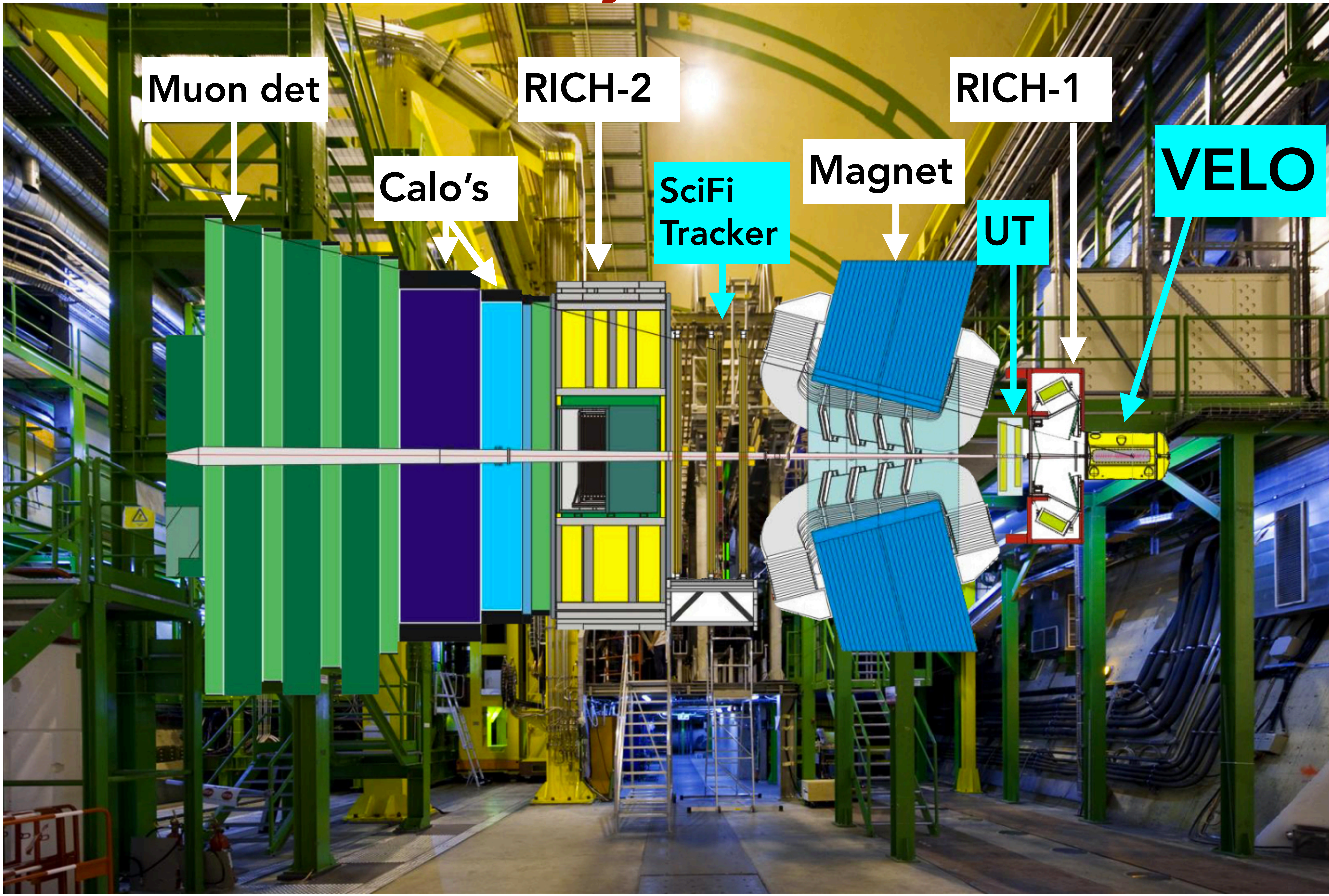
Vertex 2019: *17-October-2019*

Outline

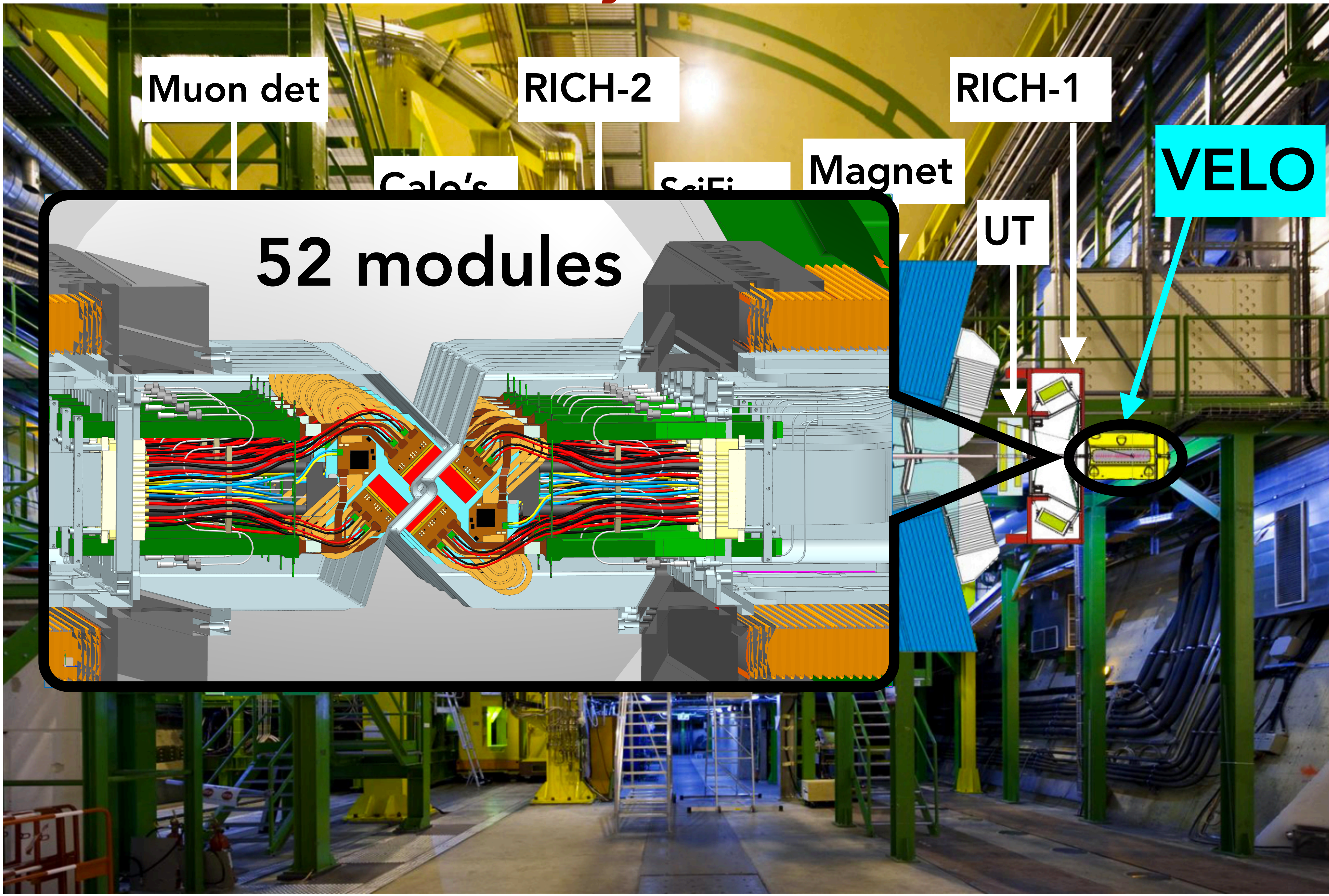
- Introduction on **VE**rtex **LO**cator (VELO)
  - K. De Bruyn talk for more details on the upgrade
  - P. Pais talk for details on past detector performances
- Silicon micro- channels cooling substrate
- Cooling performance on pre-production module



LHCb Layout in 2021



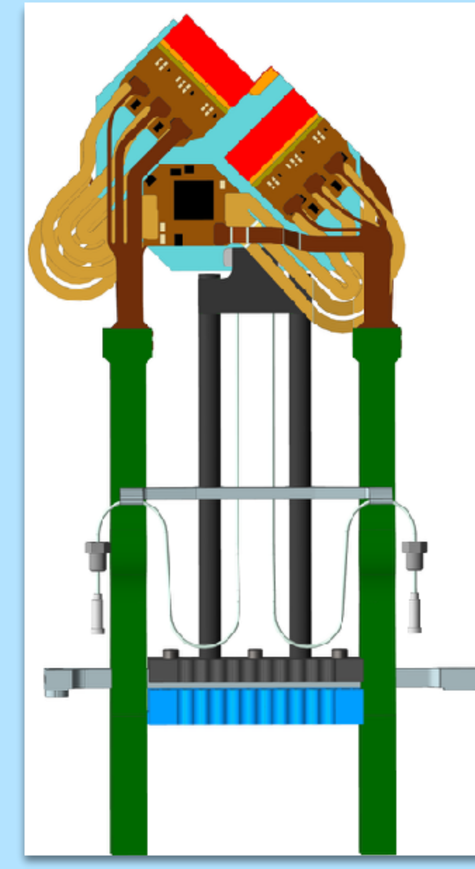
LHCb Layout in 2021

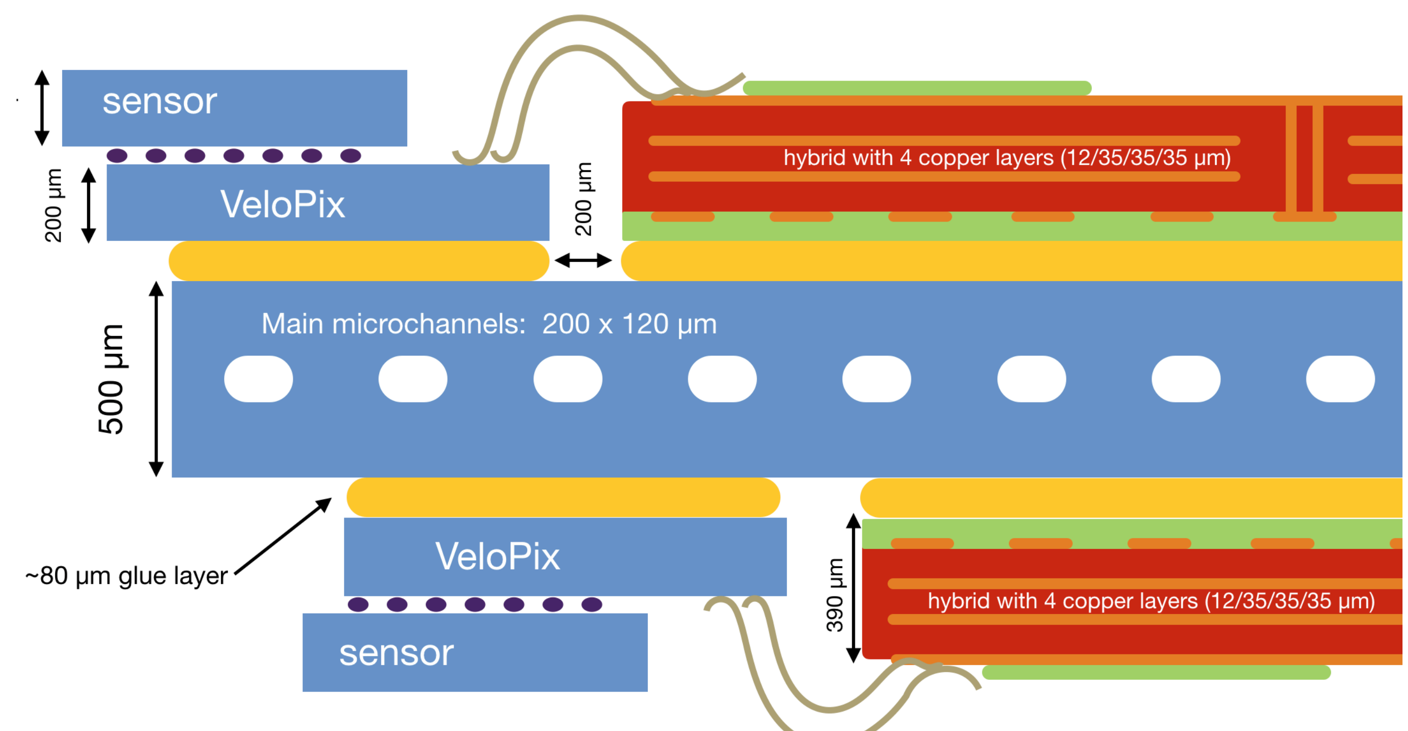


VELO for upgraded LHCb

- Silicon pixel modules around the LHC beam interaction region
  - Closest **distance to LHC beam: 5.1 mm**
- 50 fb^{-1} integrated luminosity for LHC Runs 3 & 4
- Very **high radiation** environment
  - Max. **fluence: 8×10^{15} MeV · n_{eq}/cm^2**
- LHCb has trigger-less readout - full detector readout @ 40 MHz
- Cooling requirement
  - Sensor tip temperature <**-20°C**
    - Power dissipation per module ~30W
  - Operating in **vacuum**
  - **Low material**: 5mm of the silicon sensor are not glued on the cooling substrate (innermost part)

- Four sensors per double sided module
- Each sensor (43 x 15 mm) bonded to three VeloPix ASIC's
- Detector Active area = 0.12 m^2





VELO for upgraded LHCb

- Silicon pixel modules around the LHC beam interaction region
  - Closest **distance to LHC beam: 5.1 mm**
- 5 ... C
  R
- V
  cm^2
- LI
  d
- C
  e

➡ **Solution**: **Evaporative CO_2 cooling through micro-channels etched in silicon**

- Excellent thermal efficiency
- No thermal expansion mismatch with silicon ASICs and sensors
- Radiation hardness of CO2
- Very low contribution to the material budget

  - Operating in **vacuum**
  - **Low material**: 5mm of the silicon sensor are not glued on the cooling substrate (innermost part)

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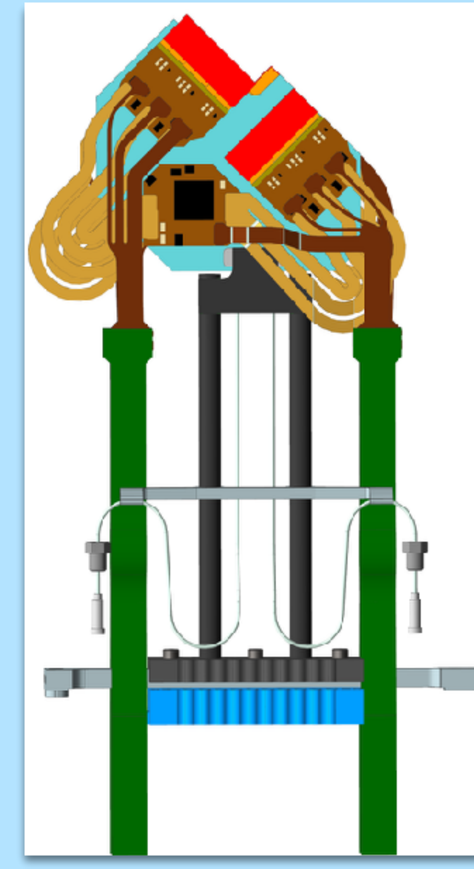
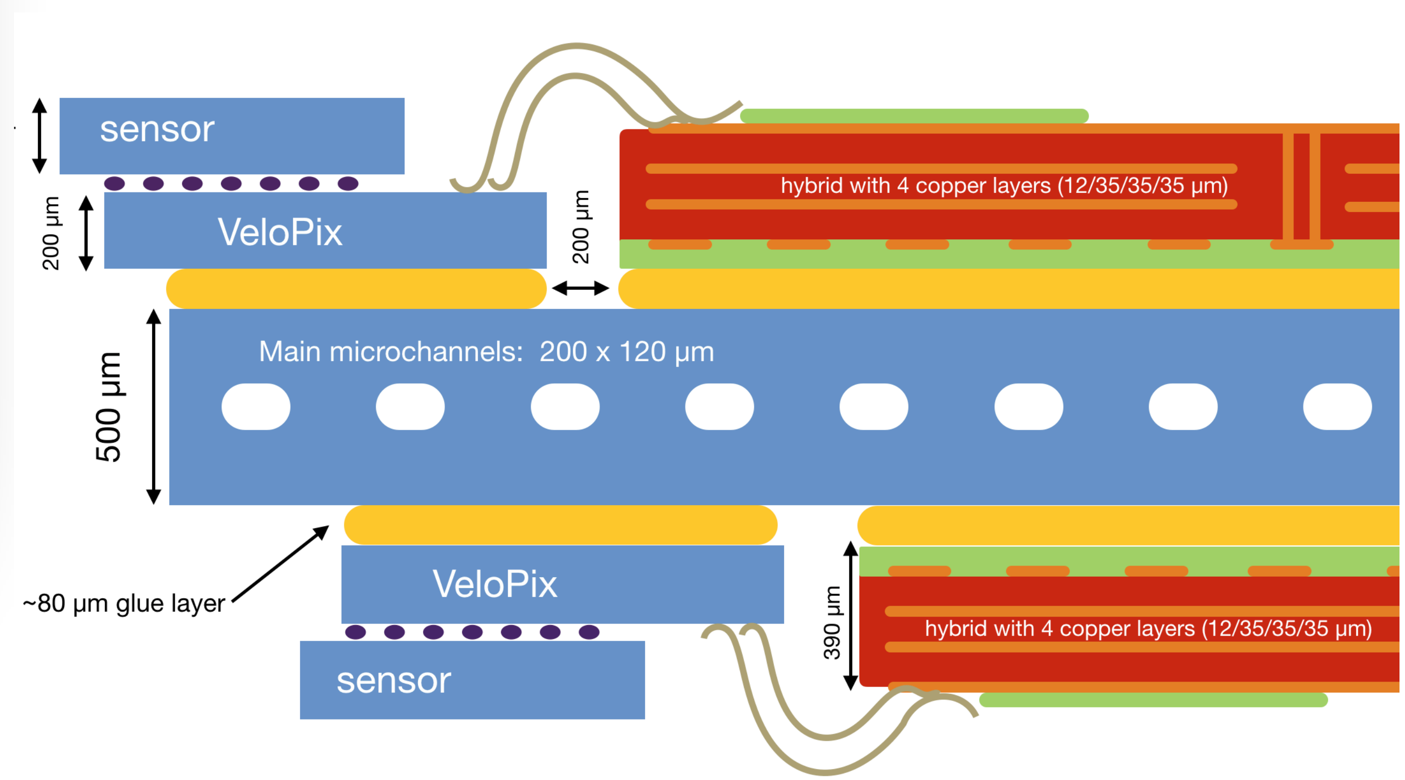
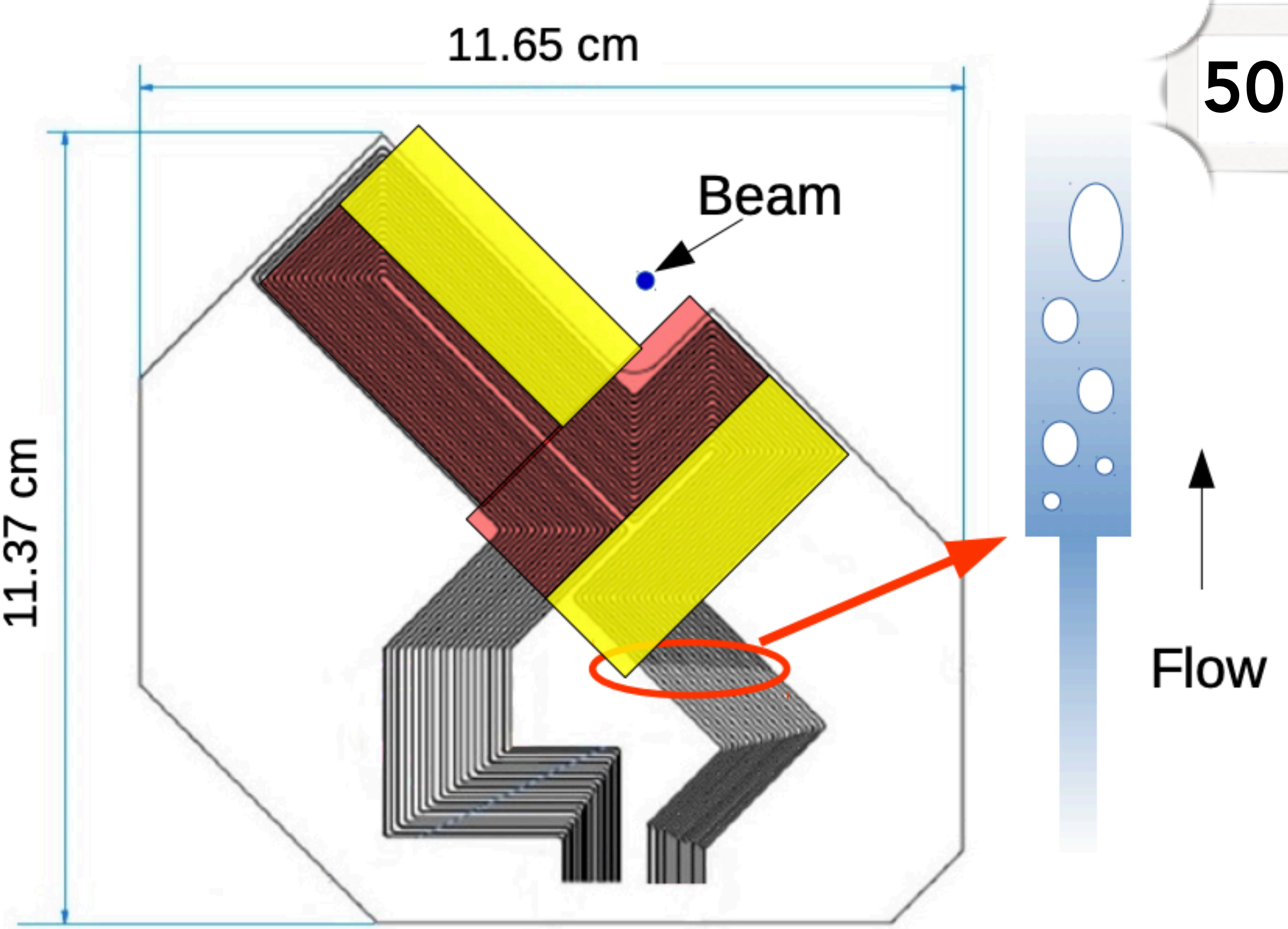




Micro-channel cooling



ASIC on front

ASIC behind

500 µm thick silicon substrate

Input restrictions:

- 60 x 60 µm , 40 mm long
- Dominant pressure drop
- Prevent instabilities among the channels

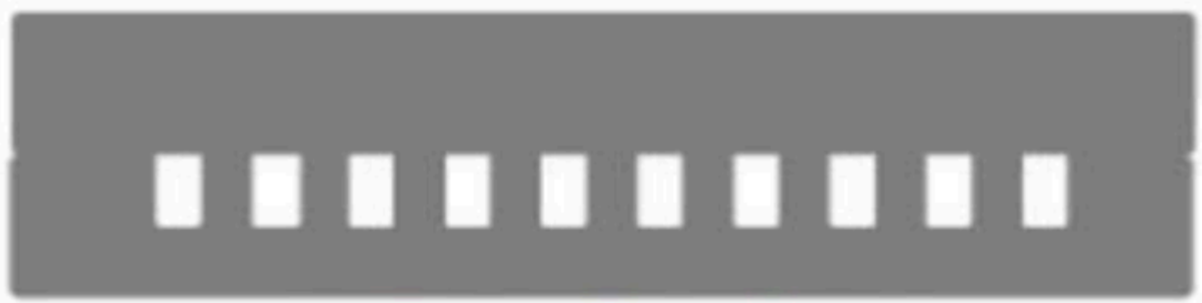
Main channels

- 120 x 200 µm
- [230, 290]mm long
- Heat is absorbed by the CO_2: change in gas/liquid ratio

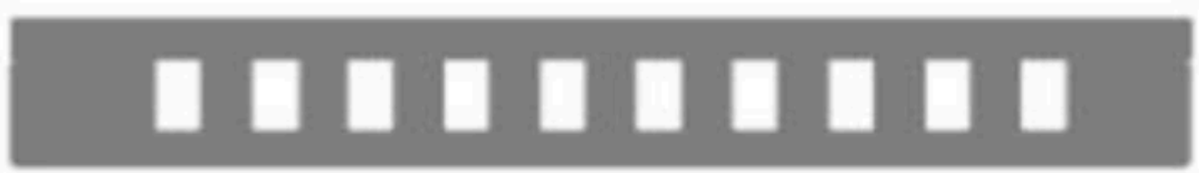
Increase in cross section between the restriction and the main channels triggers the boiling

Micro-channel manufacture

DRIE etching of the channels



Si cover bonding

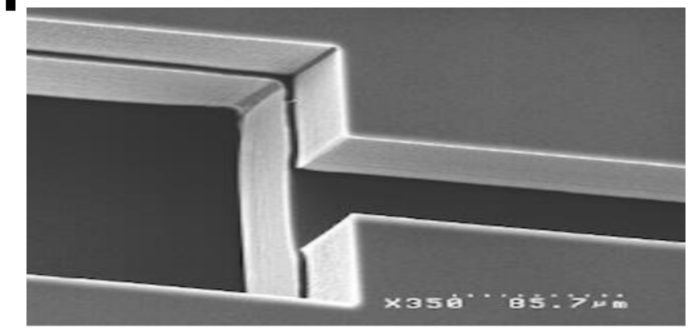


Thinning

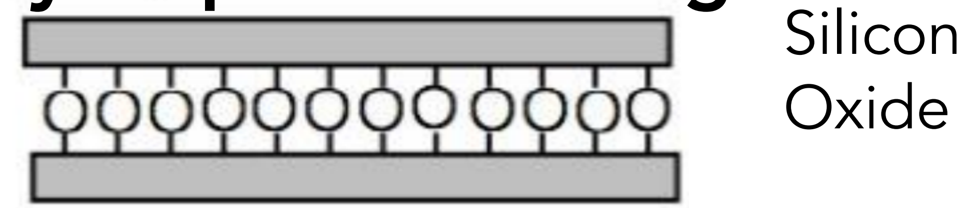
Plasma etching of fluidic inlets

Metallisation for soldering connectors

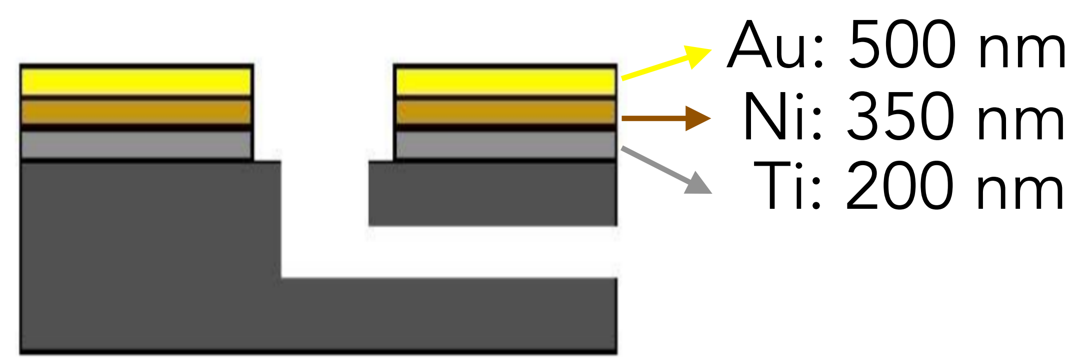
Deep Reactive Ion Etching

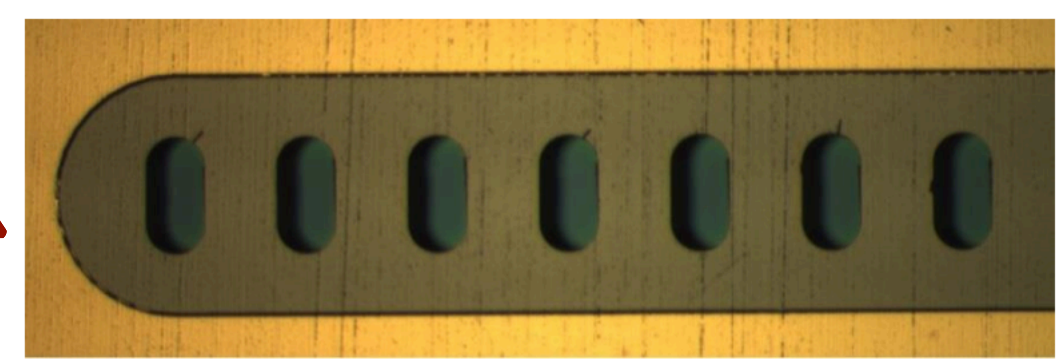


Hydrophilic bonding



Metallisation

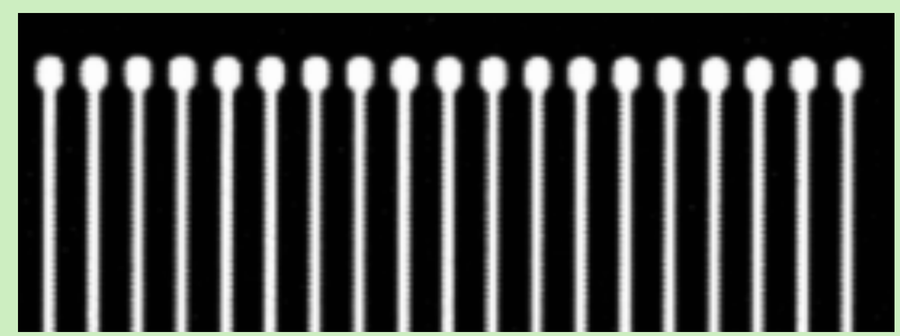




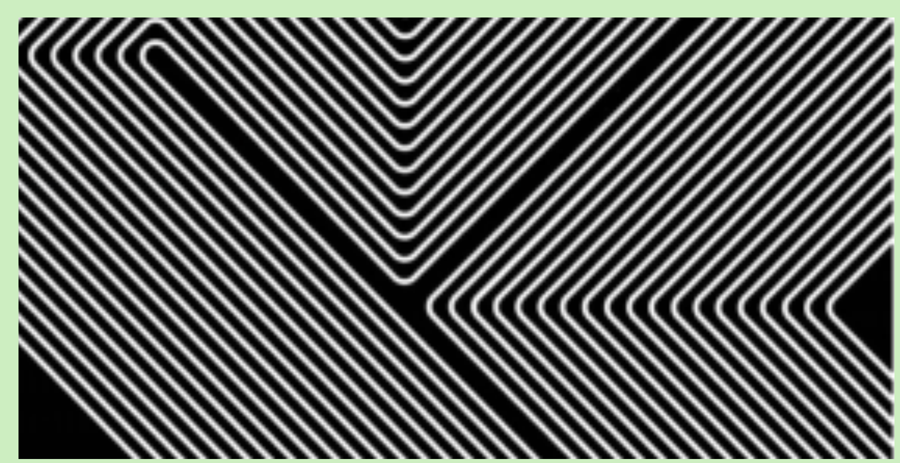
Micro-channel substrate grading

- **Grade A**: no defects
- **Grade B**: defects close to input/output
- **Grade C**: defect near channels
- **Grade P**: dicing defects

Scanning Acoustic microscope (SAM)



No defects: Input manifold



No defects: Channels

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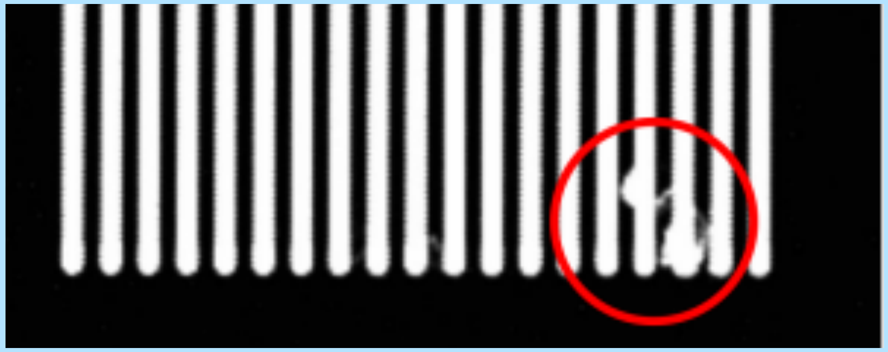
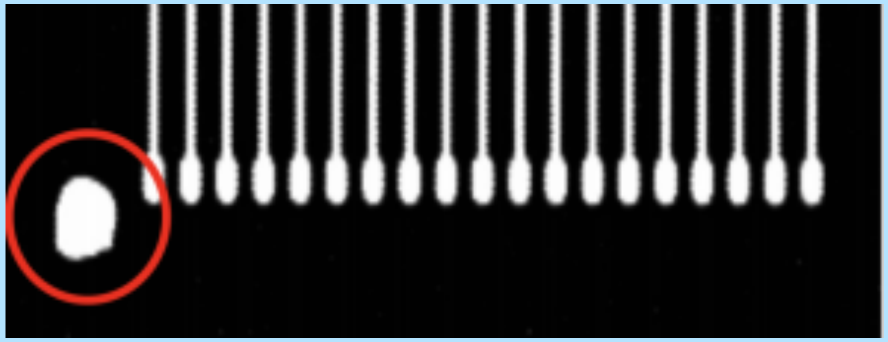


Connected channels, output manifold



Defect close to the input manifold

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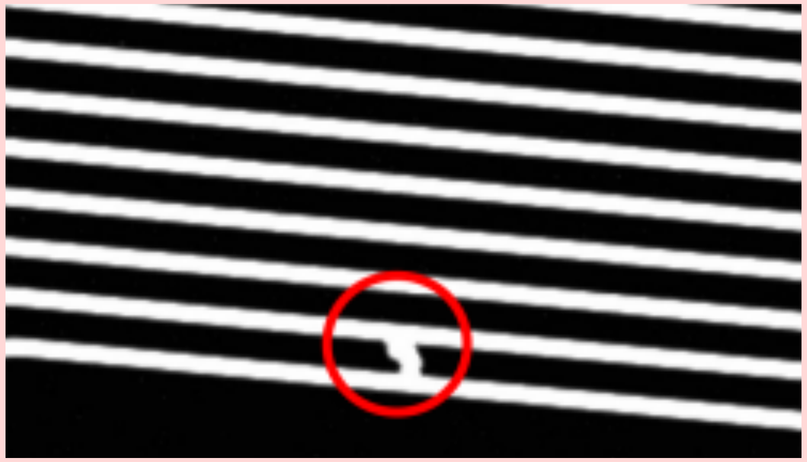
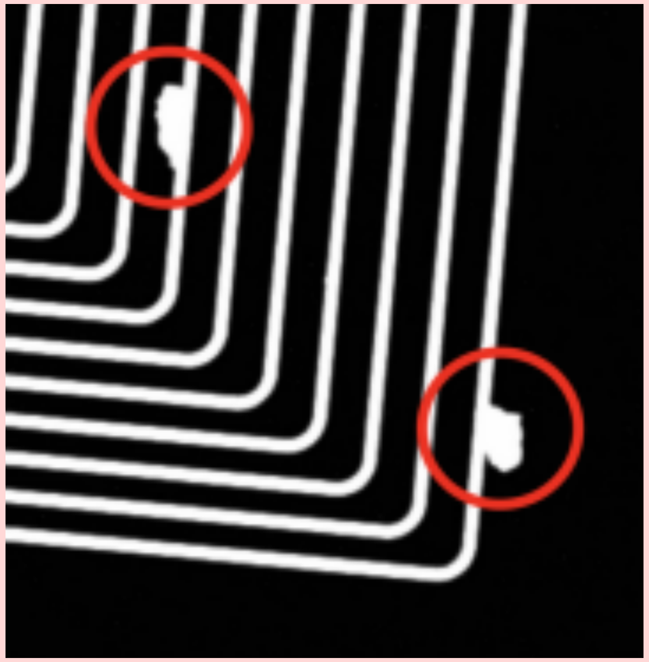
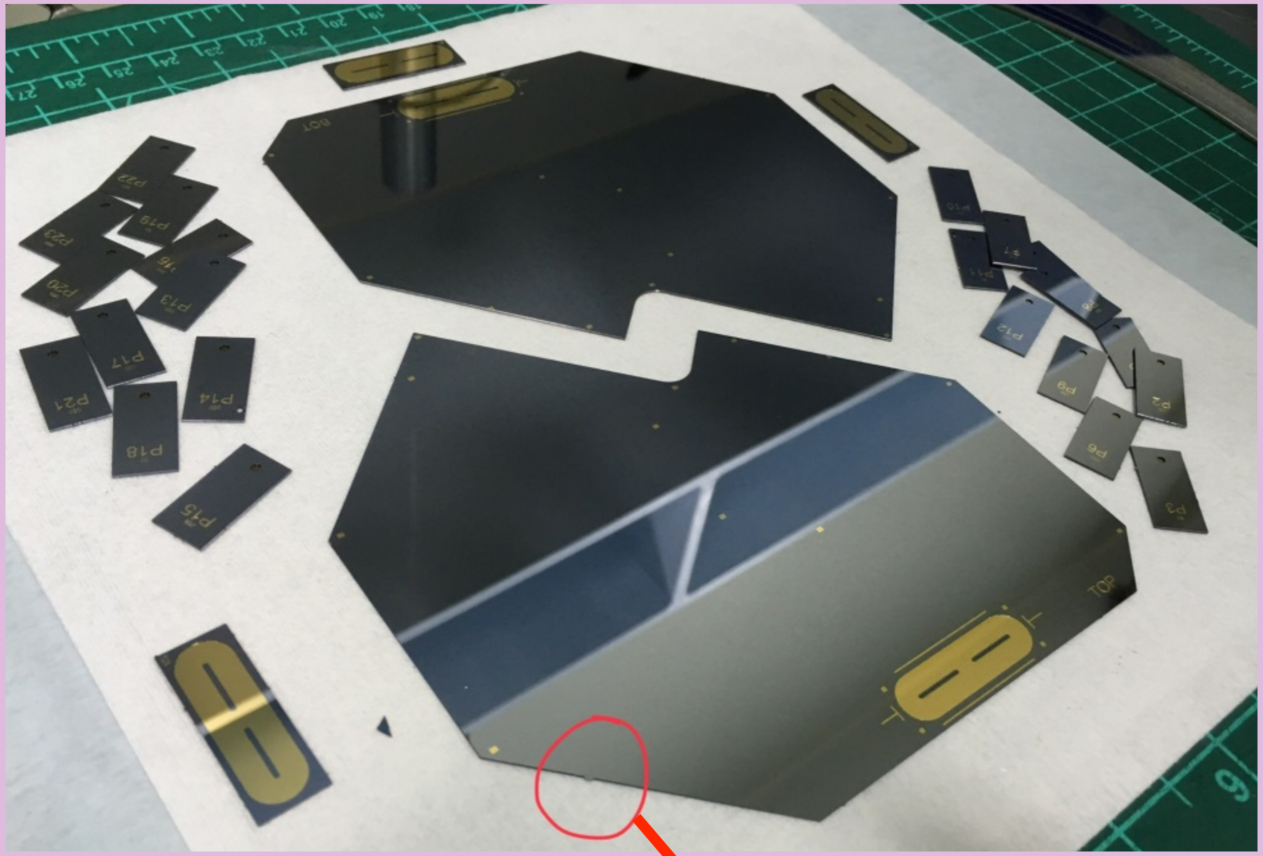


Connected channels



Defects connected to the channels

Micro-channel substrate grading



"**Pont**"

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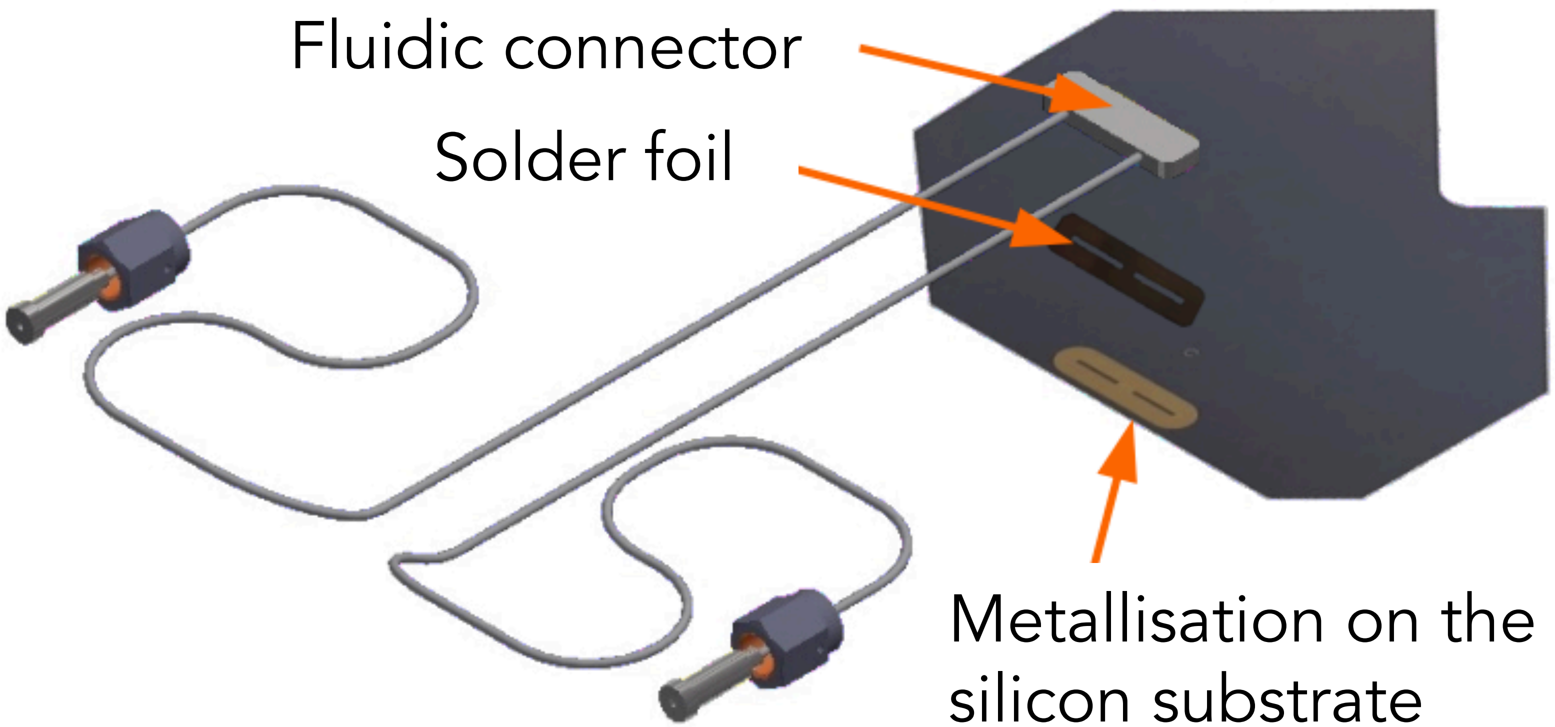
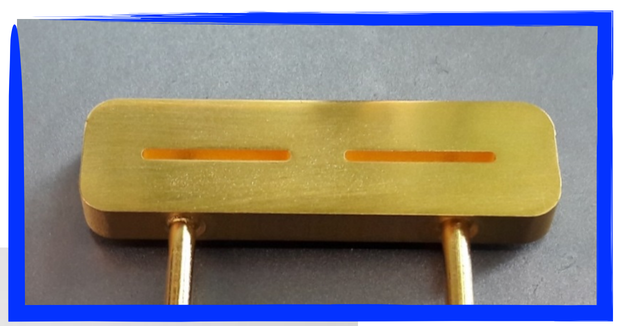
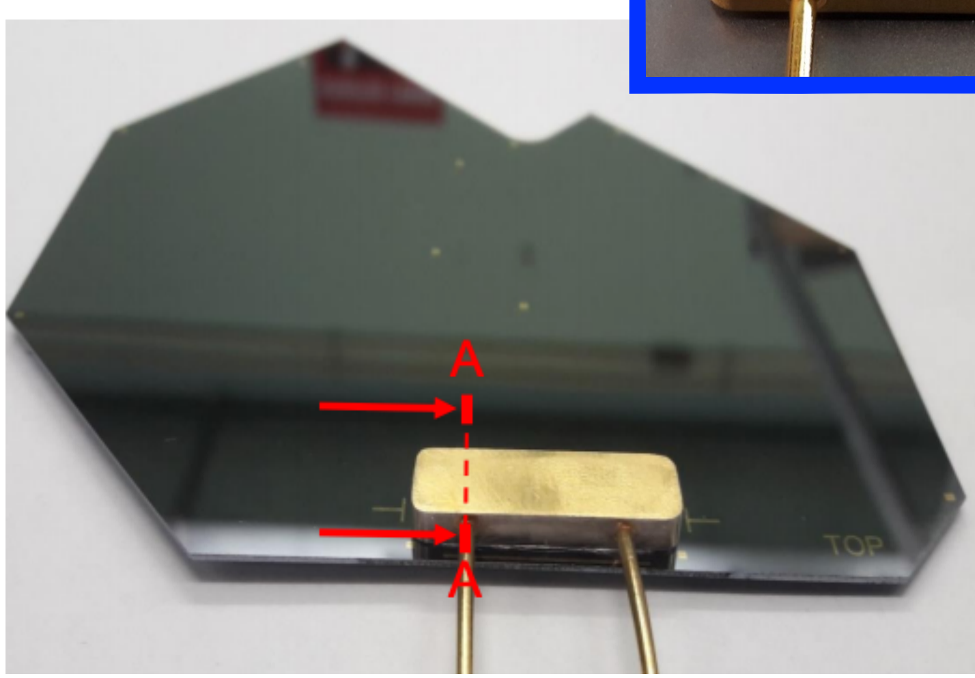
Attachment of the fluidic connector

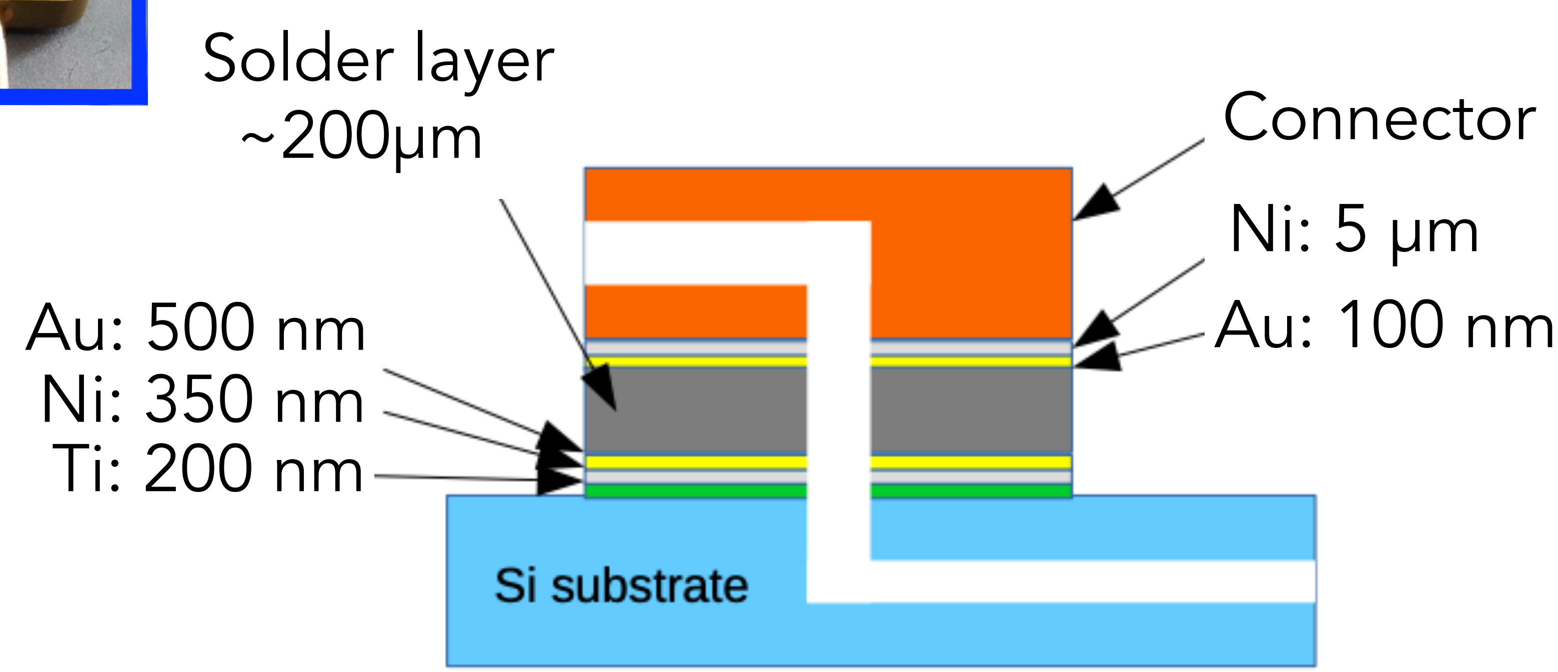


Challenges

- Leak tightness
- Planarity
- Minimum voids in the solder layer
- No Flux
- High pressure







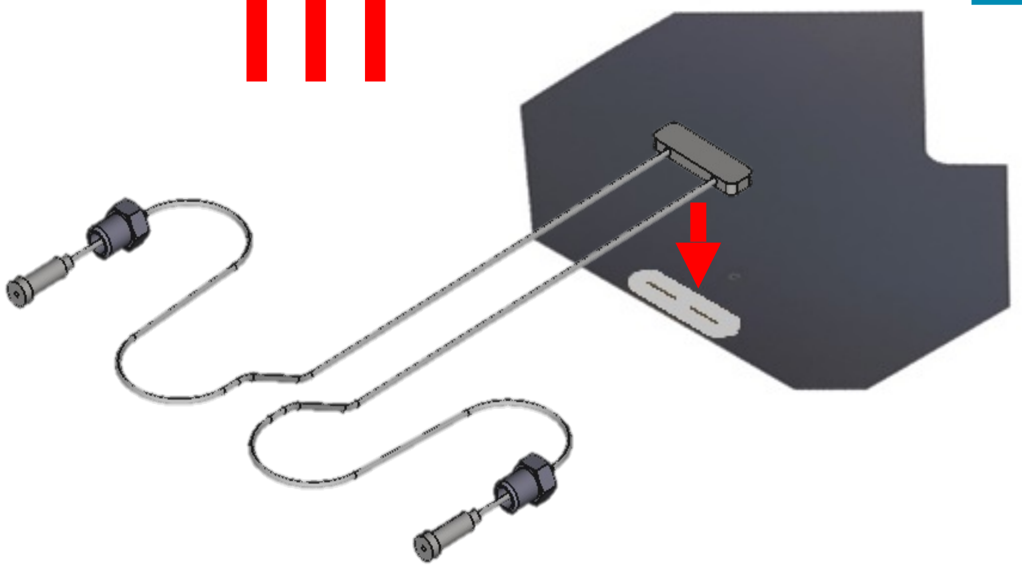
Substrate assembly

Silicon pre-tinning

I

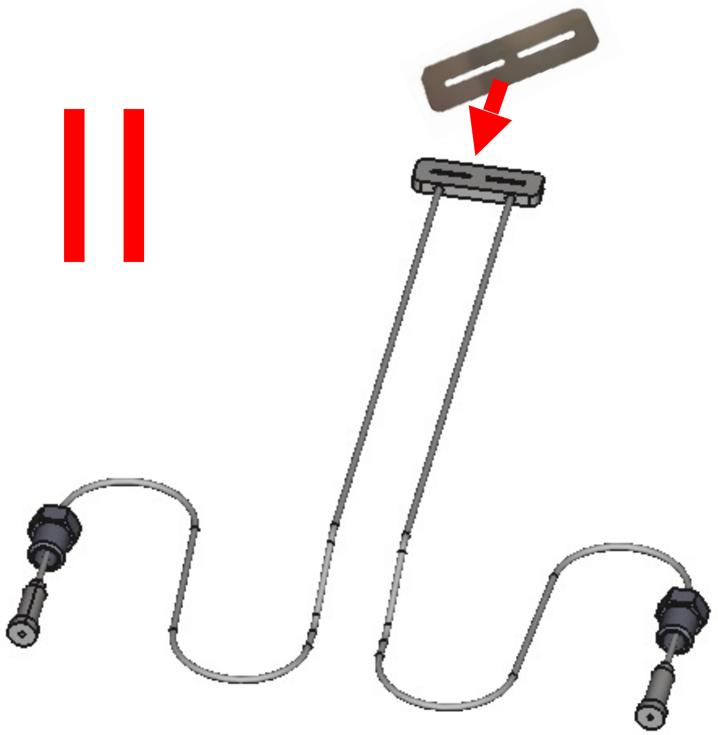
III

Alignment



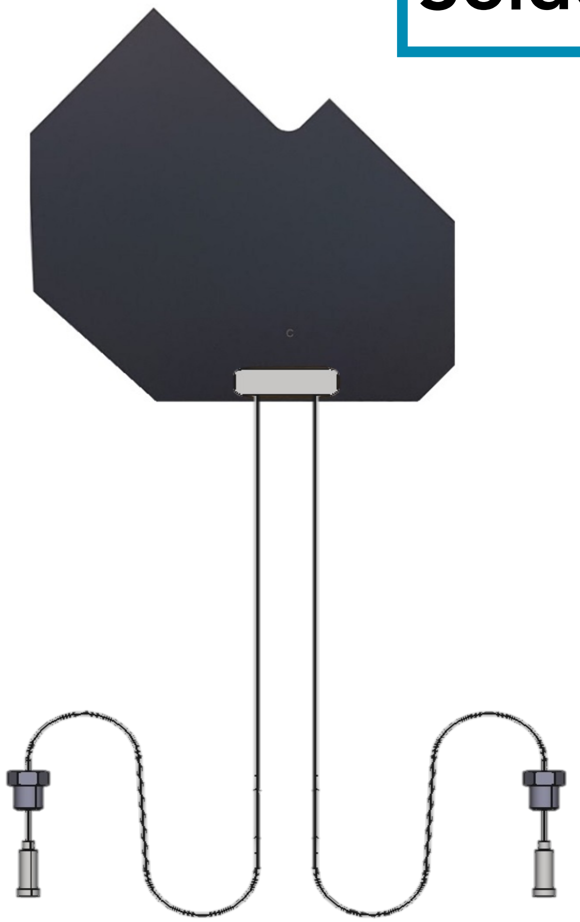
Connector pre-tinning

II



IV

Soldering



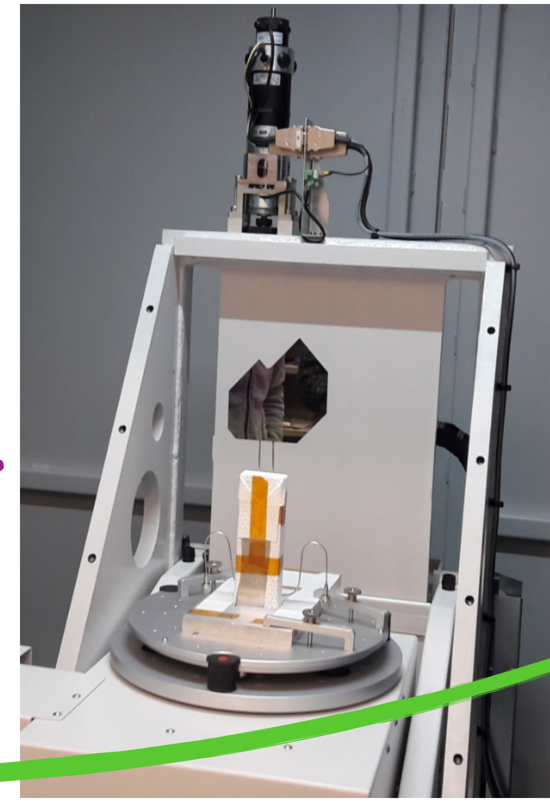
Quality assurance after connector soldering

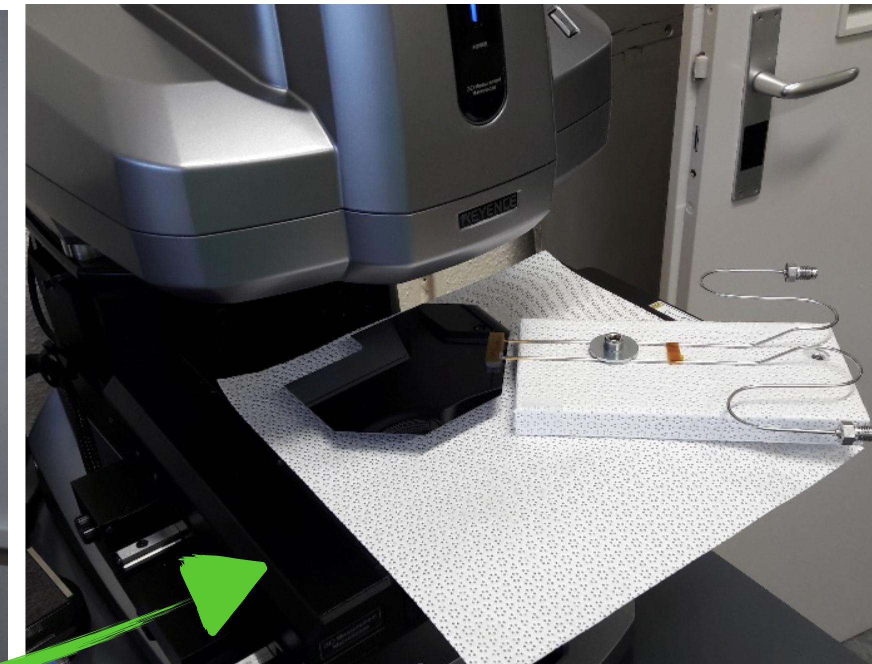
Qualification

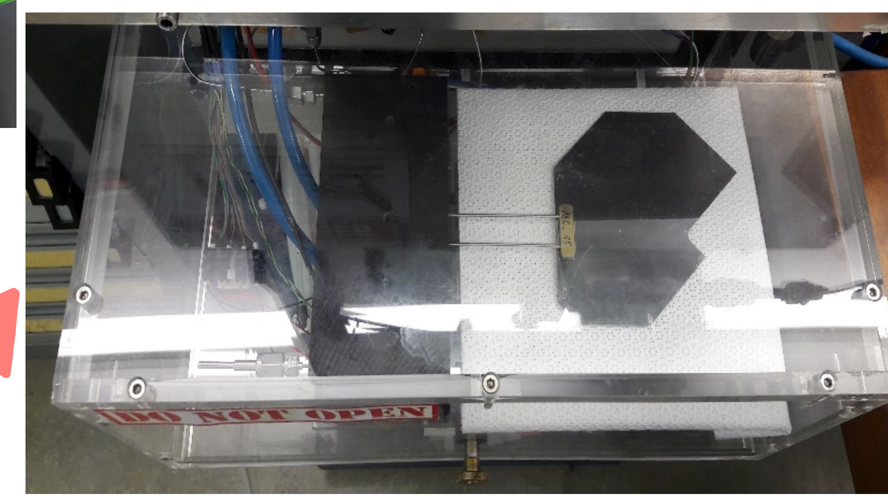
- Visual inspection
- 2D x-ray projection or 3D x-ray tomography
- Substrate flatness measurement

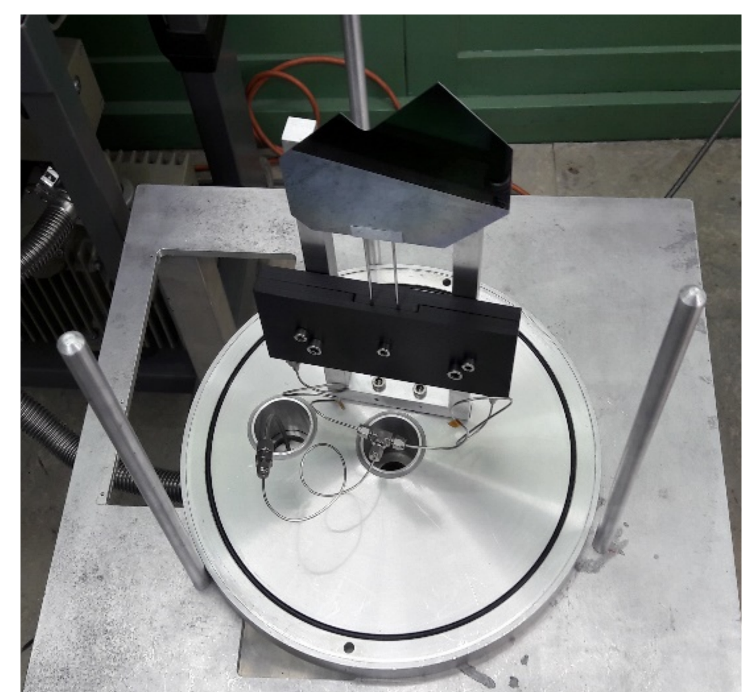
Robustness test

- Leak test
- Highest pressure test: up to 186 bar
- High pressure helium leak test: 60 bar







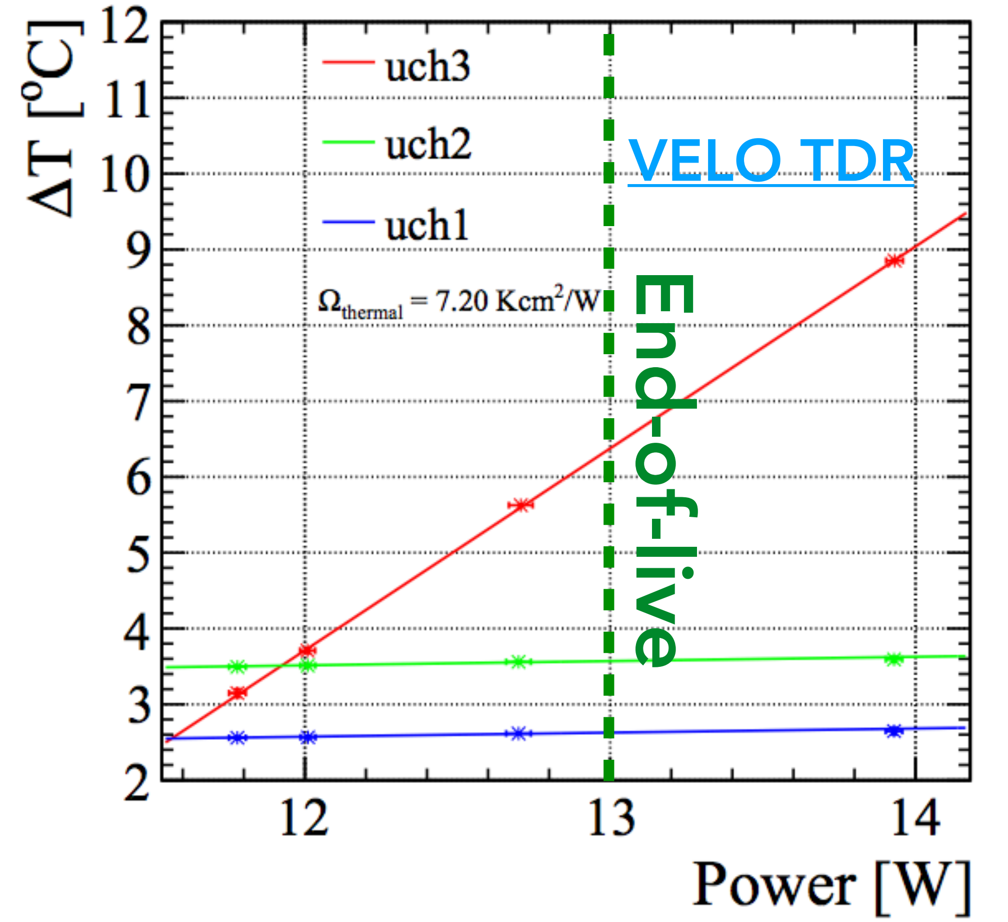


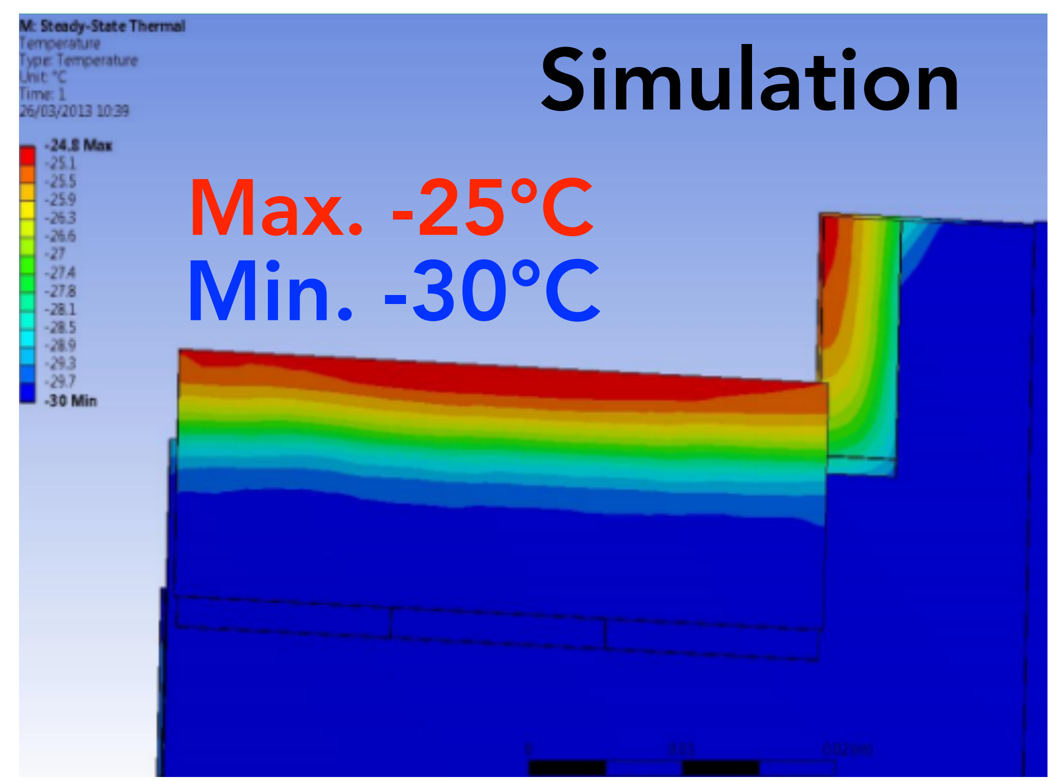
Cooling performance

Cooling performance has been evaluated using thermal mockups emulating half pixel module

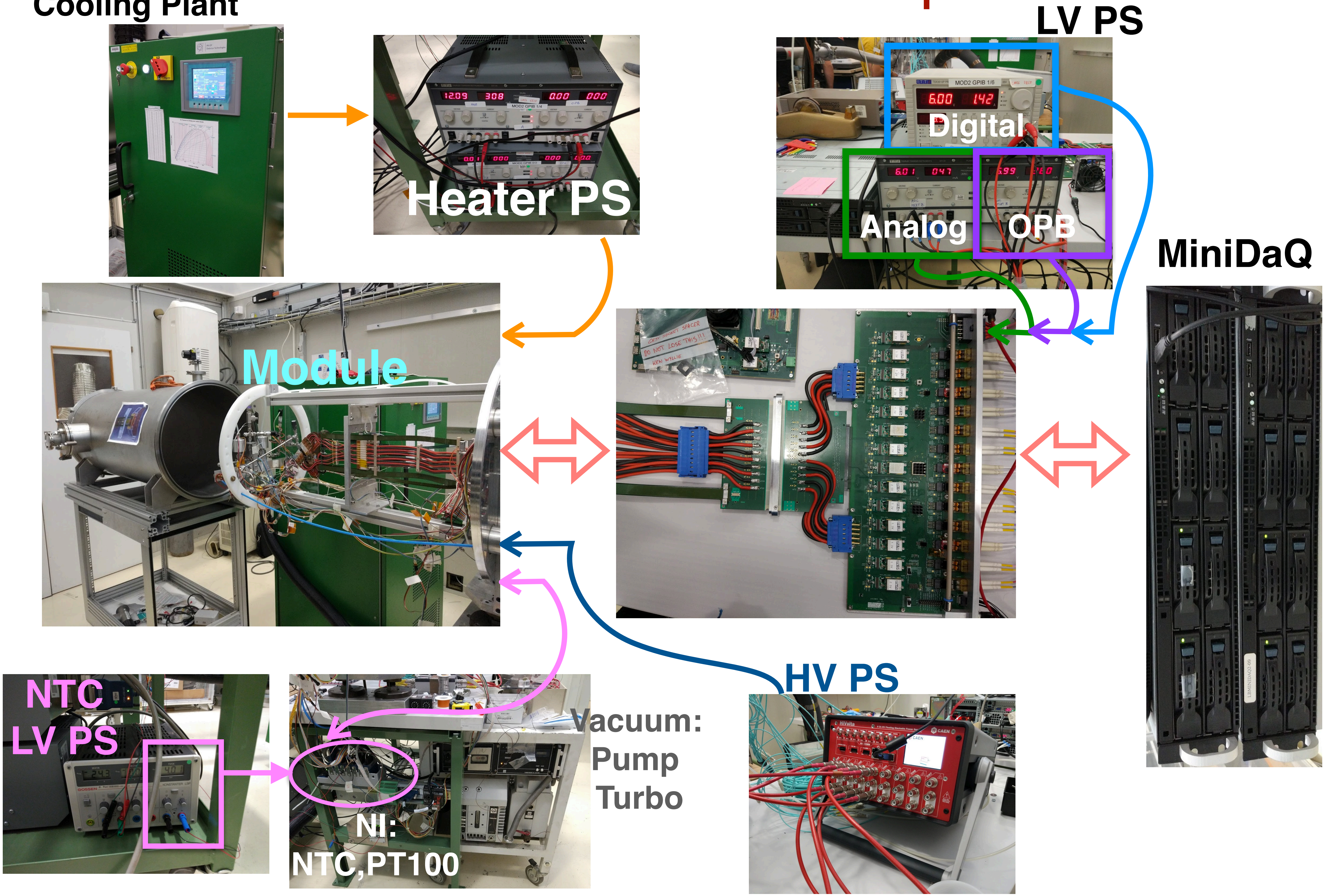
- In nominal conditions, expected 12 W
- The end of-lifetime expectation is 13 W
  - **ΔT** between sensor tip and experiment output **around 6°C**
  - Effectiveness of the substrate at providing local cooling
  - ASIC power is concentrated at the part more remote from the silicon tip
- CO_2 normal operation at -30°C corresponds total pressure of 14.28 bar
  - At room temperature the pressure rises to 57.29 bar
  - Operational temperature range is between -30°C and +15°C

Placed at the tip of the mock-sensor





VELO test setup



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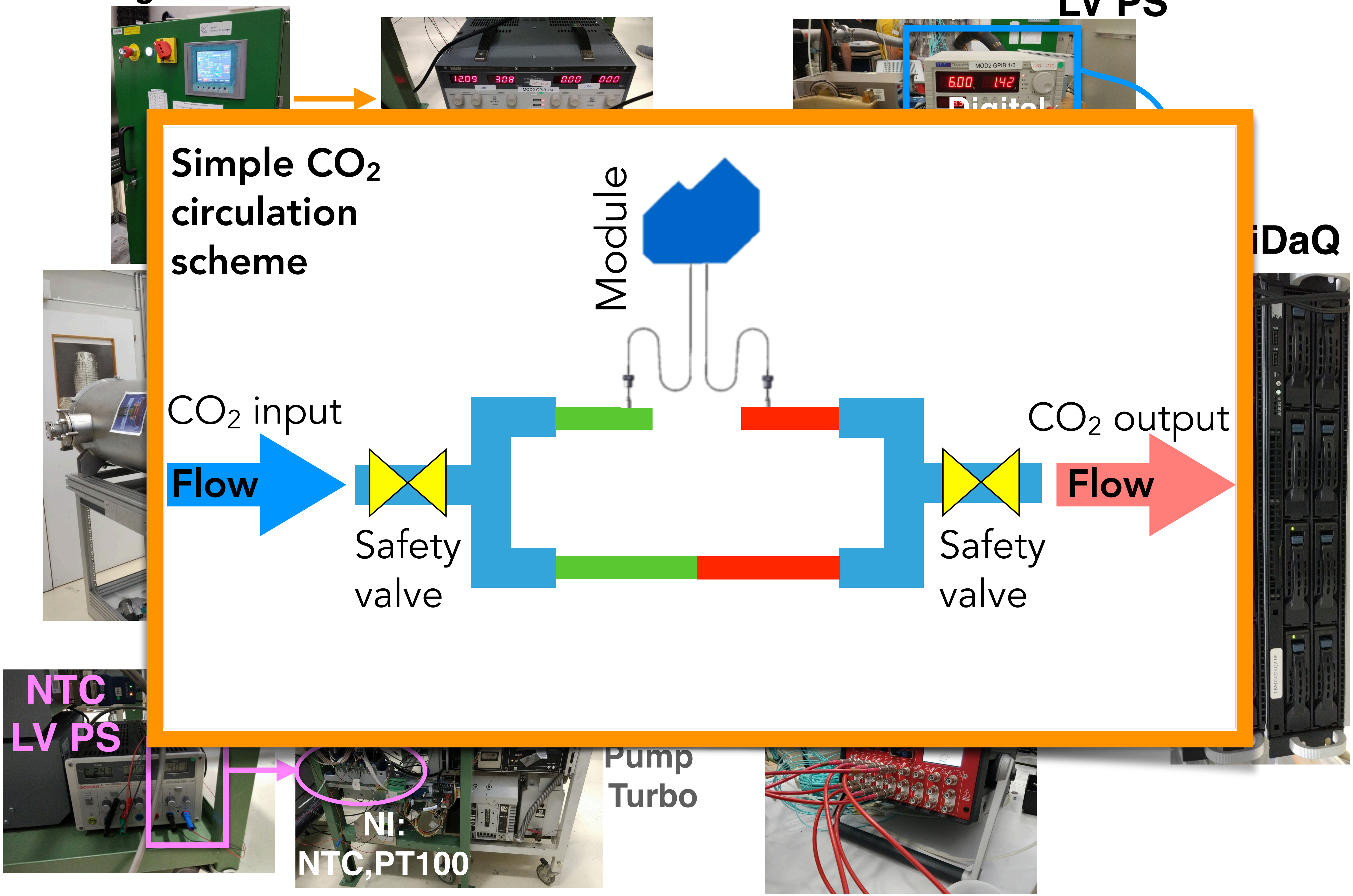
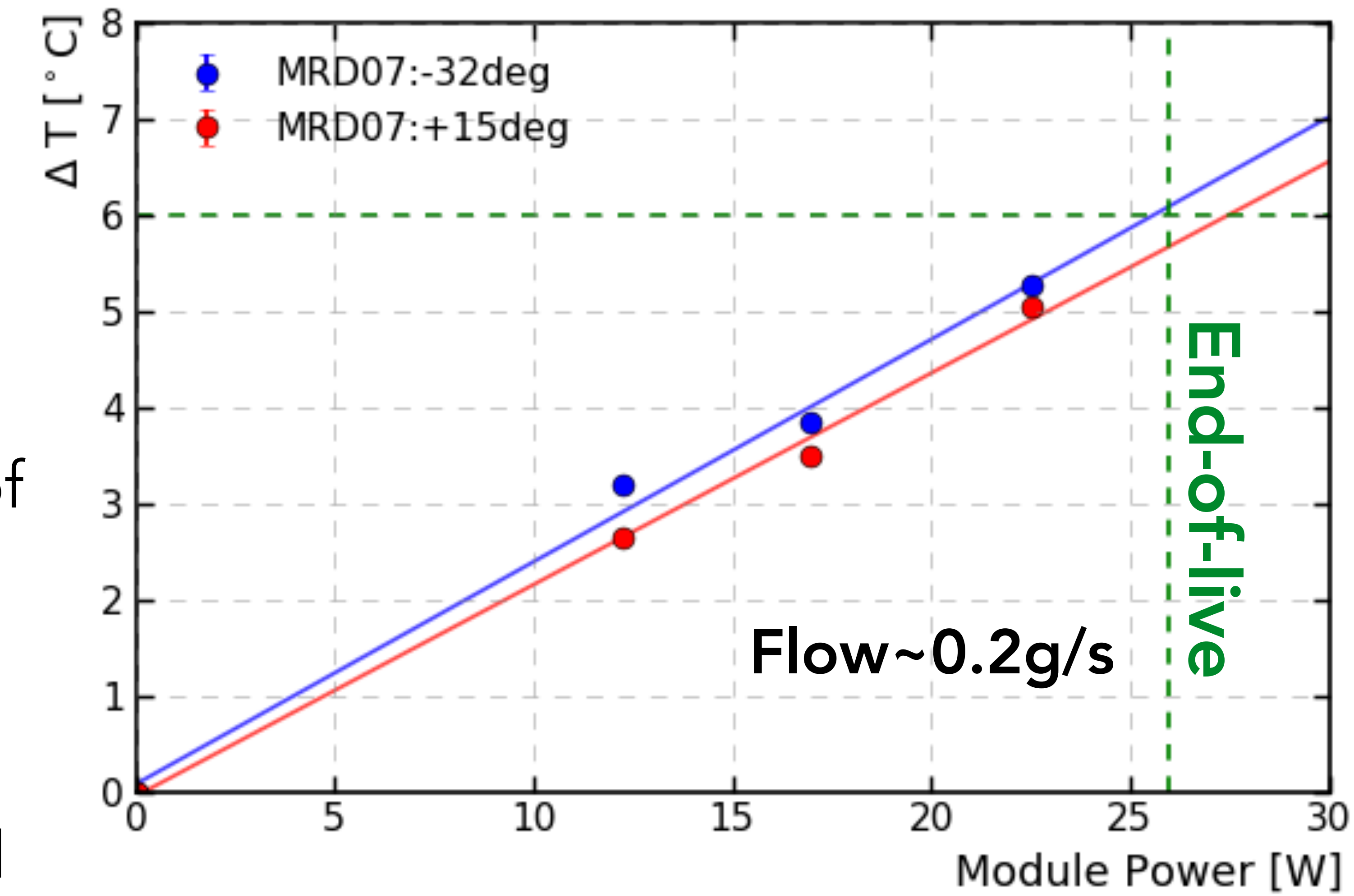


Cooling performance

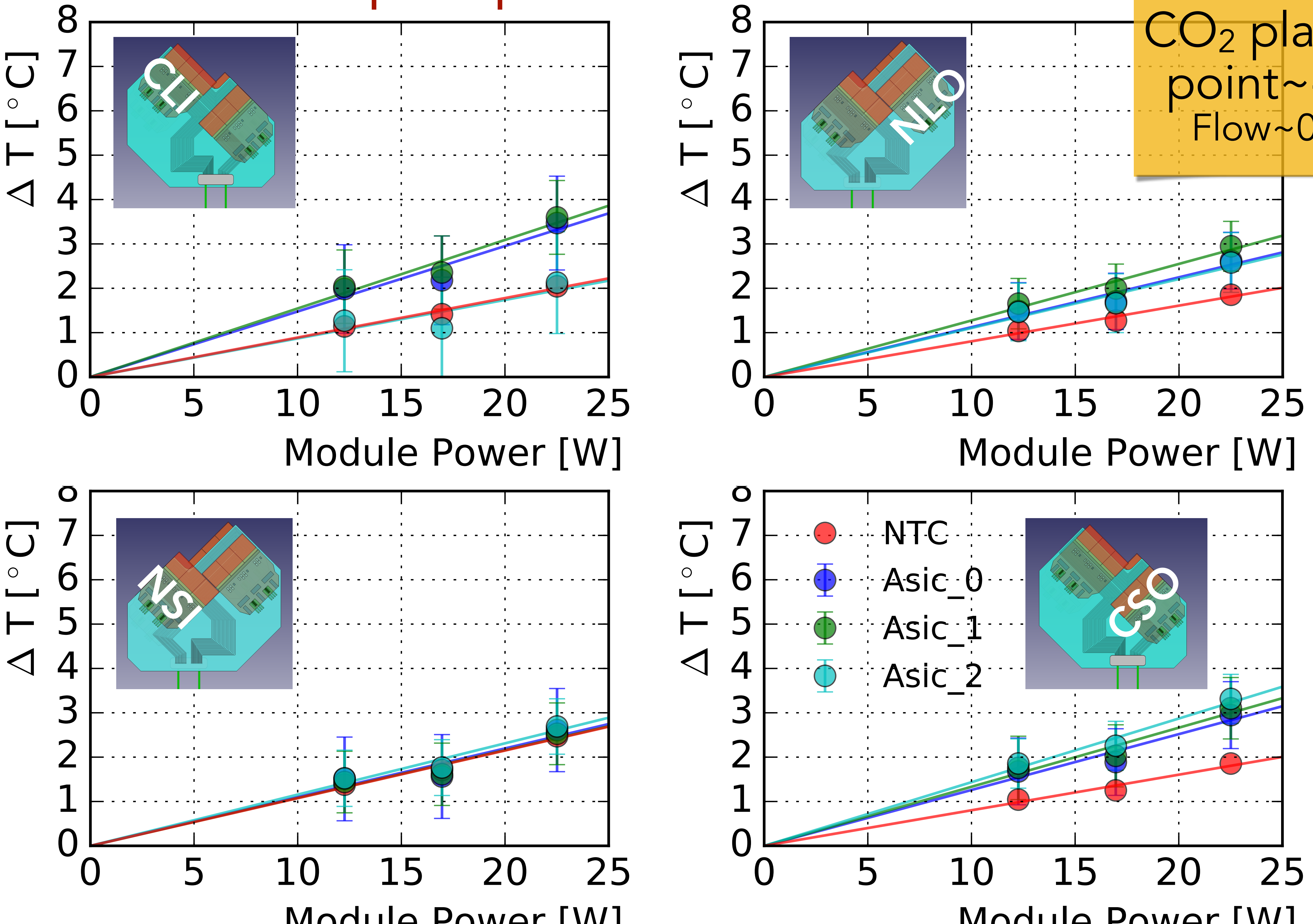
- Full module power consumption ~**23 W**
  - Expected end-of-lifetime power dissipation on the sensor ~1W: **27W**
- To reduce material innermost part of the sensor is not in contact with the cooling substrate
  - **Overhang power~1.6W**
- ***ONLY*** during power dissipation and thermal load study, temperature sensor were located on the tip of the innermost tile
  - Final module will not have the sensor
  - Study performed to correlate the temperature on the tip with the one measurement by the Asics



ΔT measurement procedure

- Temperatures registered by each Asic/NTC/PT100 for each power scenarios
- Made a linear fit of the temperature versus module power
- Normalise the point to the fit result and extrapolate to (0,0)

Power dissipation performance of a pre-production module



CO_2 plant set-point~-32℃
Flow~0.3g/s

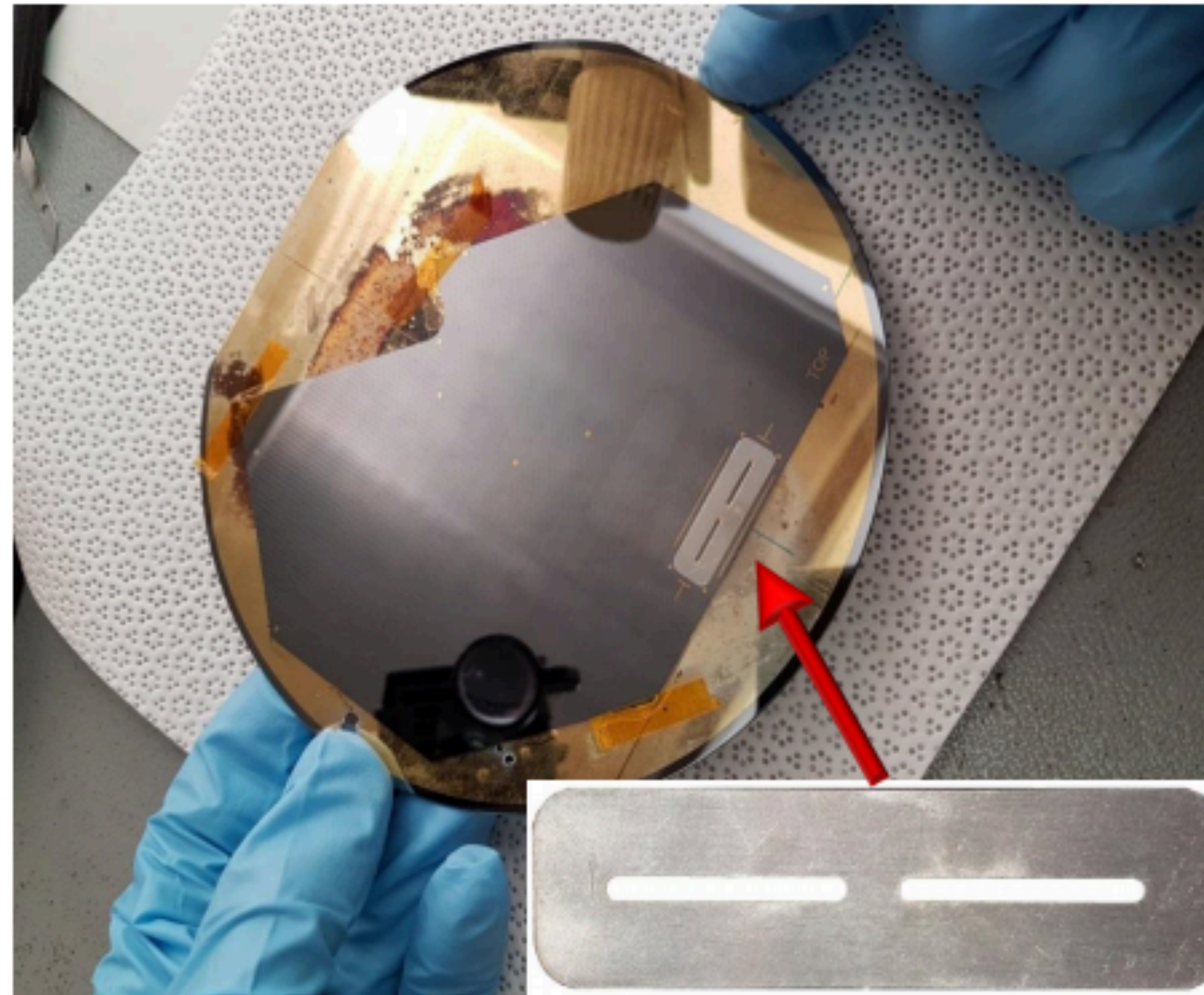
Conclusion

- **Micro-channels cooling substrate is an ideal option to reduce the material** near the interaction point and hence allow for better physics performance
- Long R&D campaign proved **great robustness and quality** of the substrate
- Many steps and qualification tests are performed during the production phase to insure high quality of the final module
- Cooling substrate is able to **dissipate the module power** (up to 30 W) and provide a ΔT on the module smaller the 6℃ in nominal power condition
- Production of the micro-channel substrates finalised
- **VELO modules production has started**: expected to be ready by next year

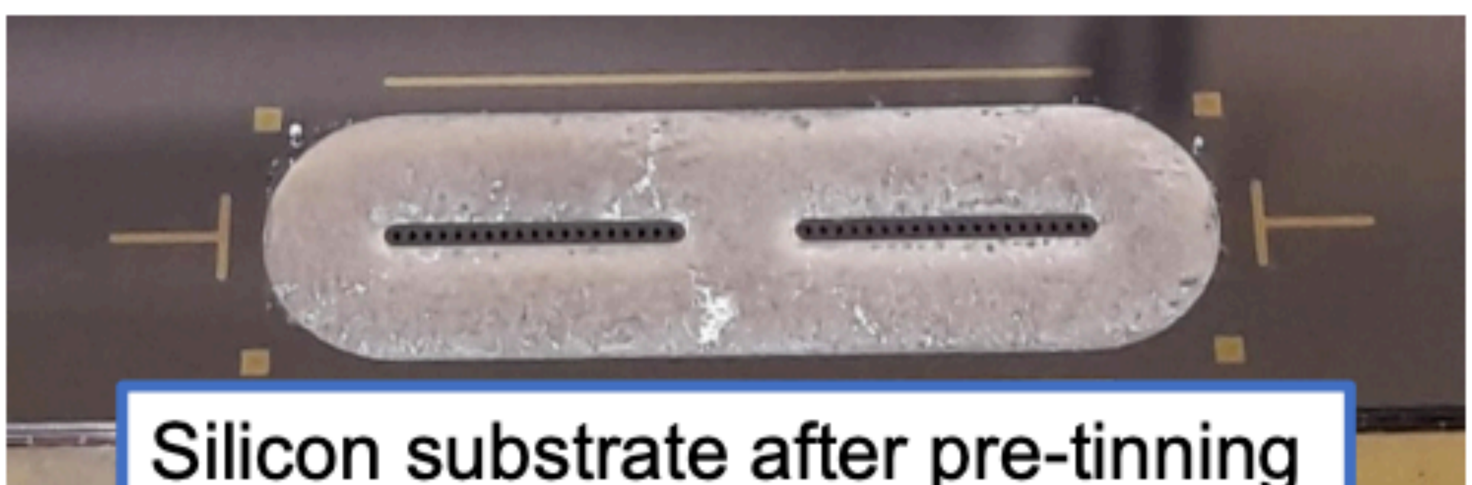
Back up

I Silicon pre-tinning

Substrate plasma cleaning

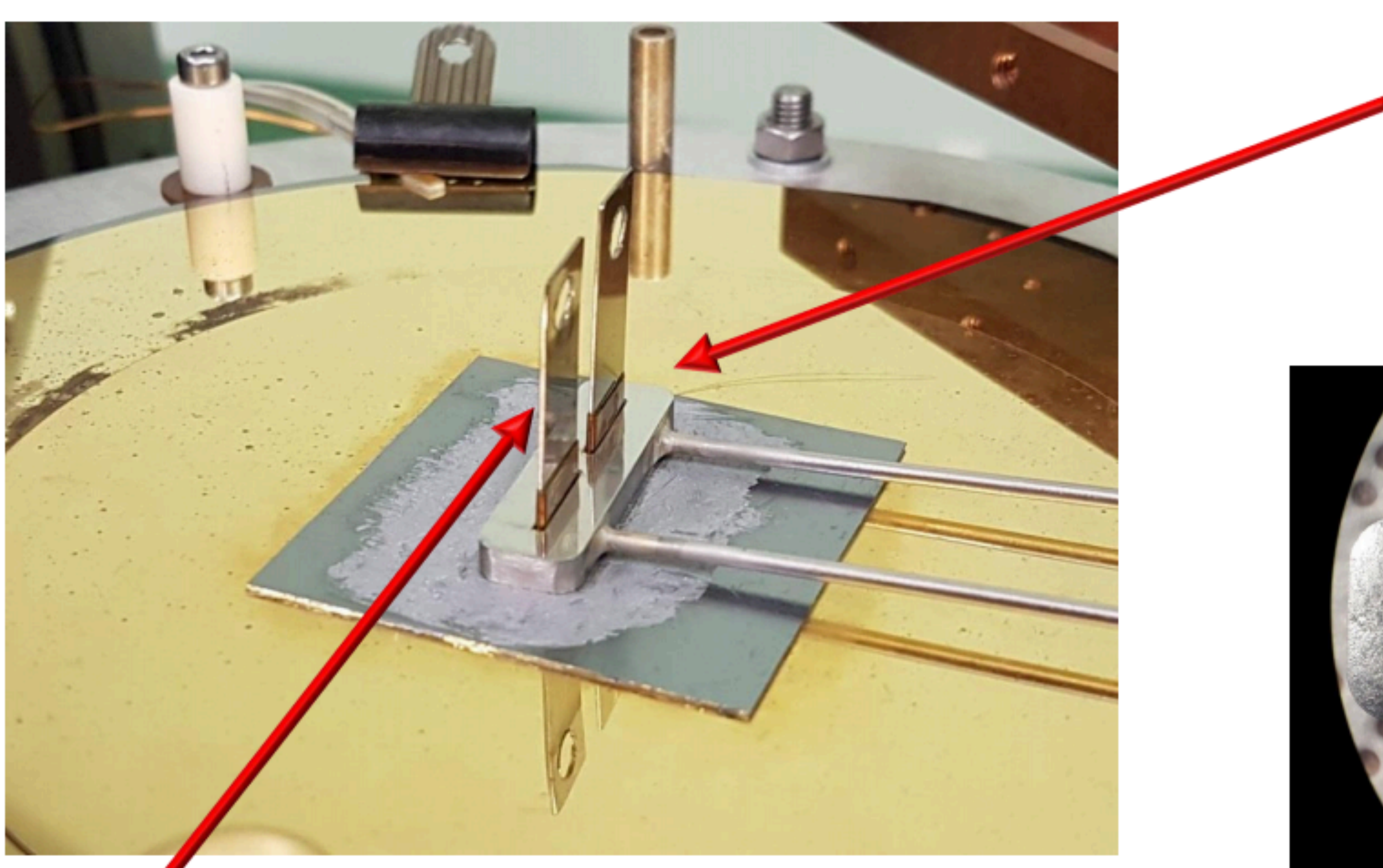


62Sn36Pb2Ag
100 [μm] preform

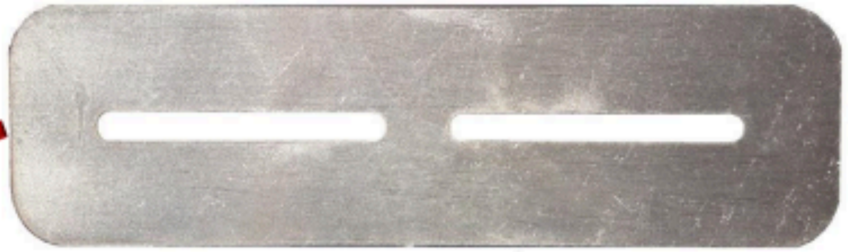


Silicon substrate after pre-tinning

II Connector pre-tinning



Slits protectors



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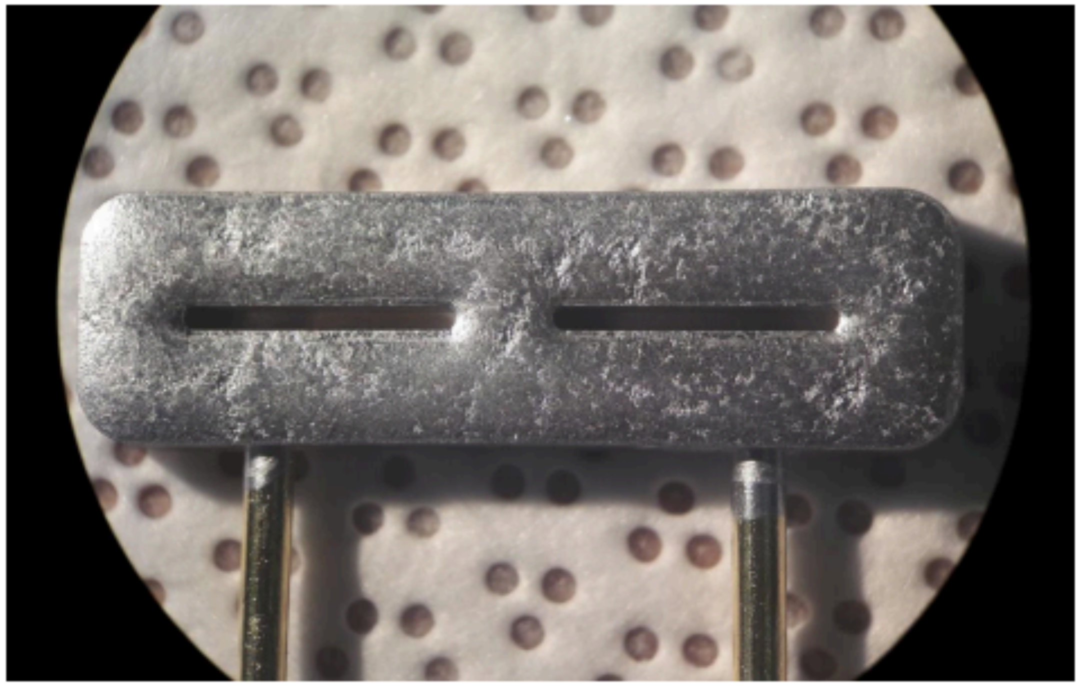
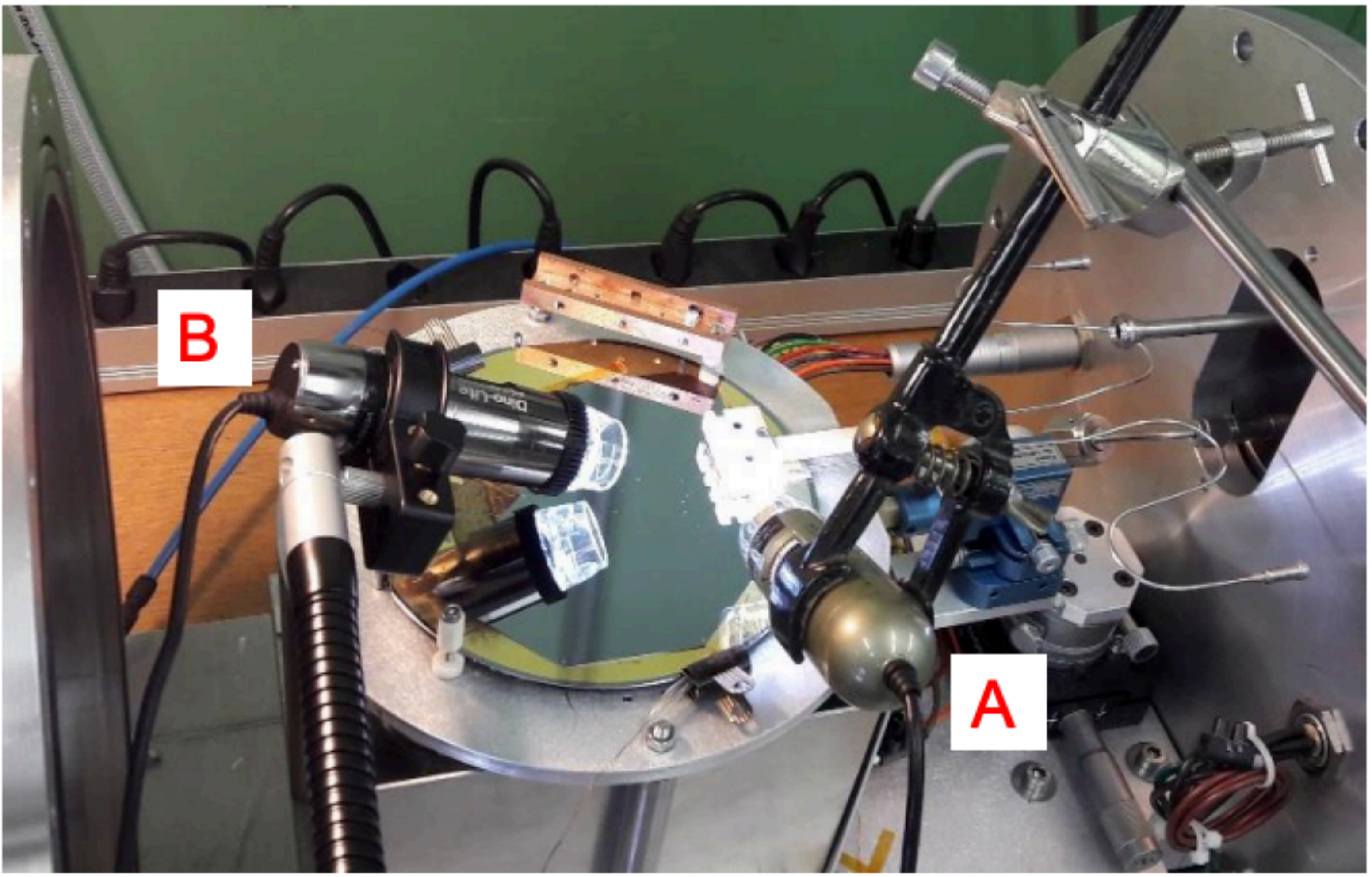
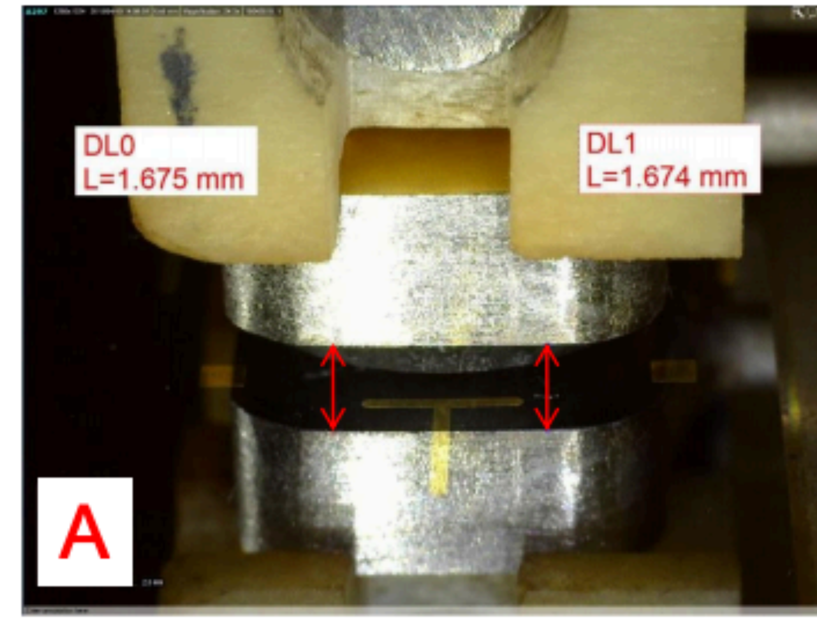


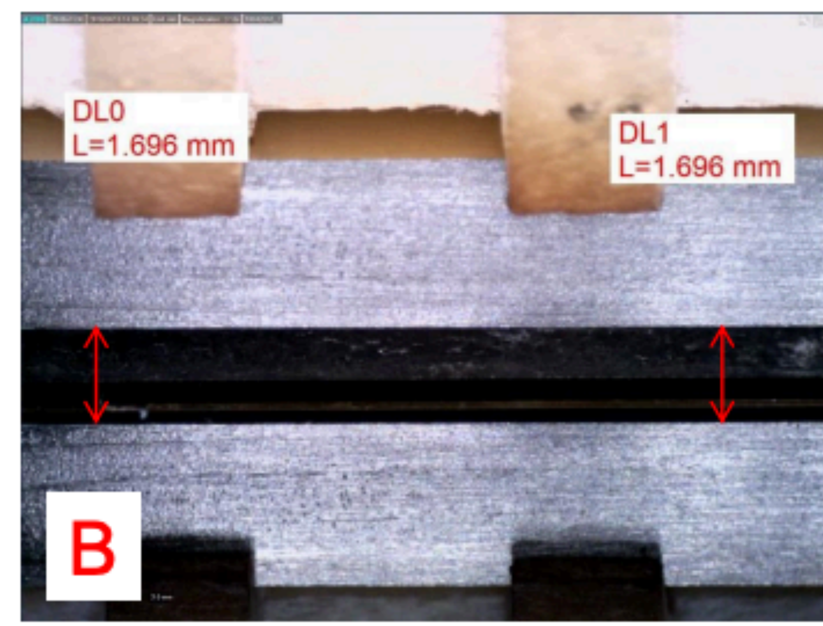
Fluidic connector after pre-tinning

III Alignment-parallelism: 1/3

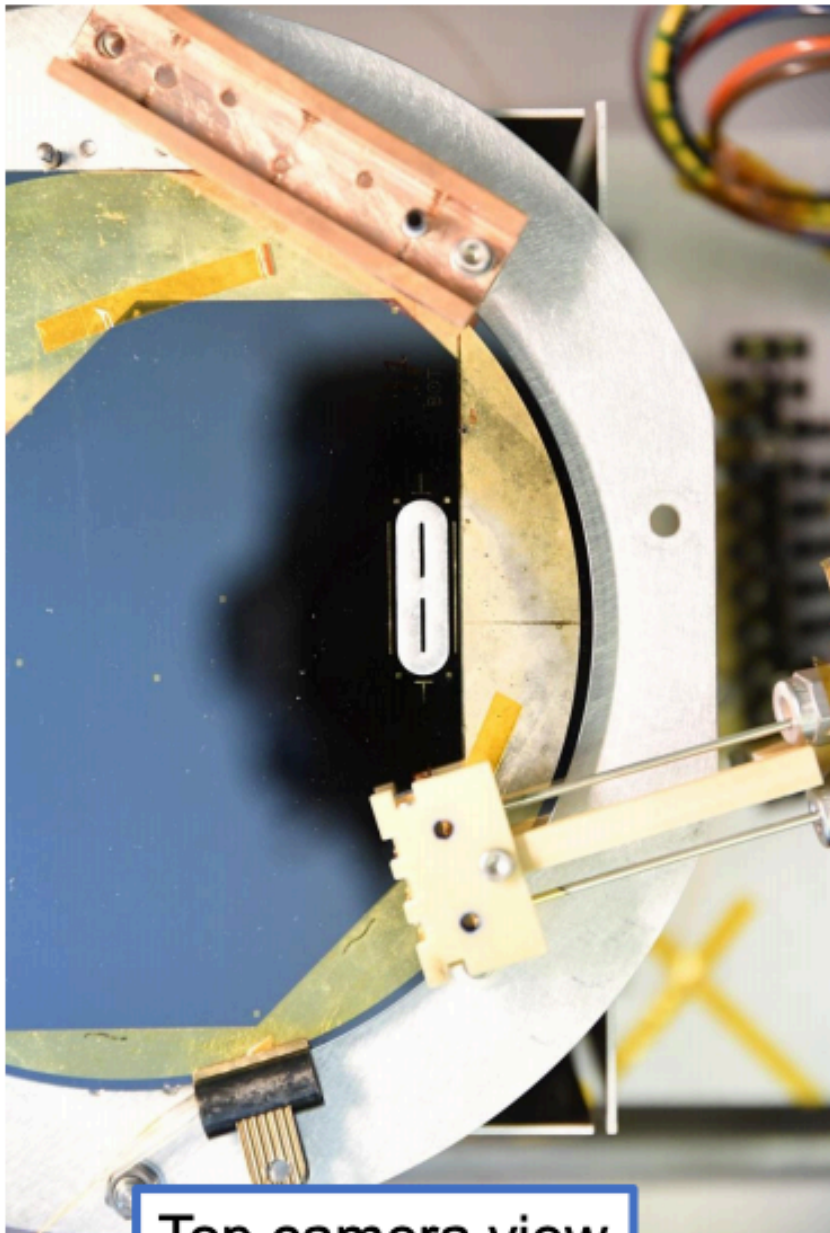


Distance between connector and its reflection measured by two USB microscopes.

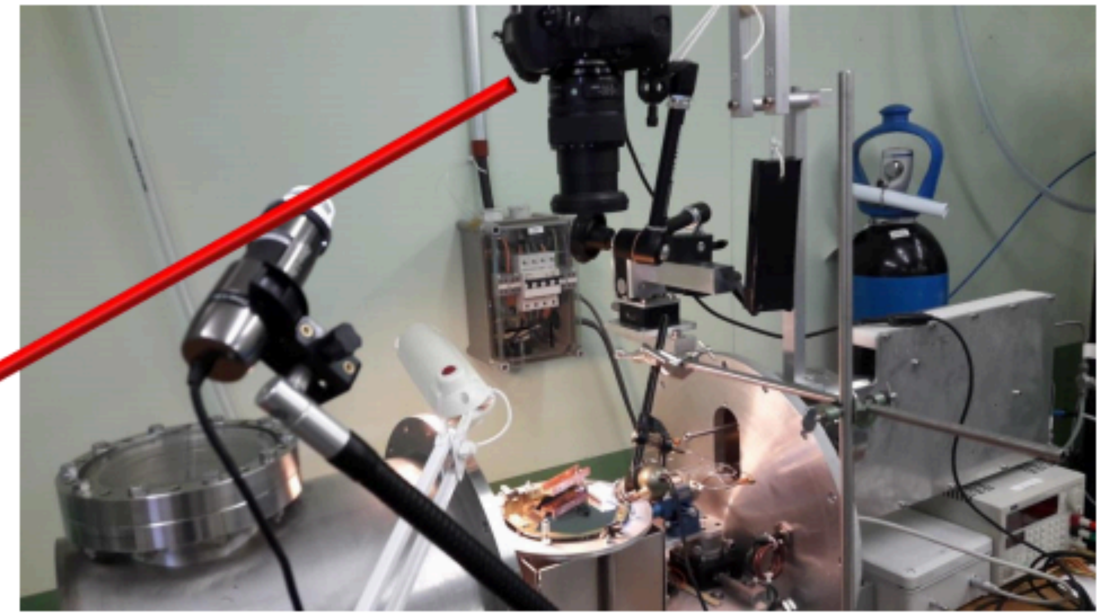




III Horizontal alignment: 2/3



Top camera view



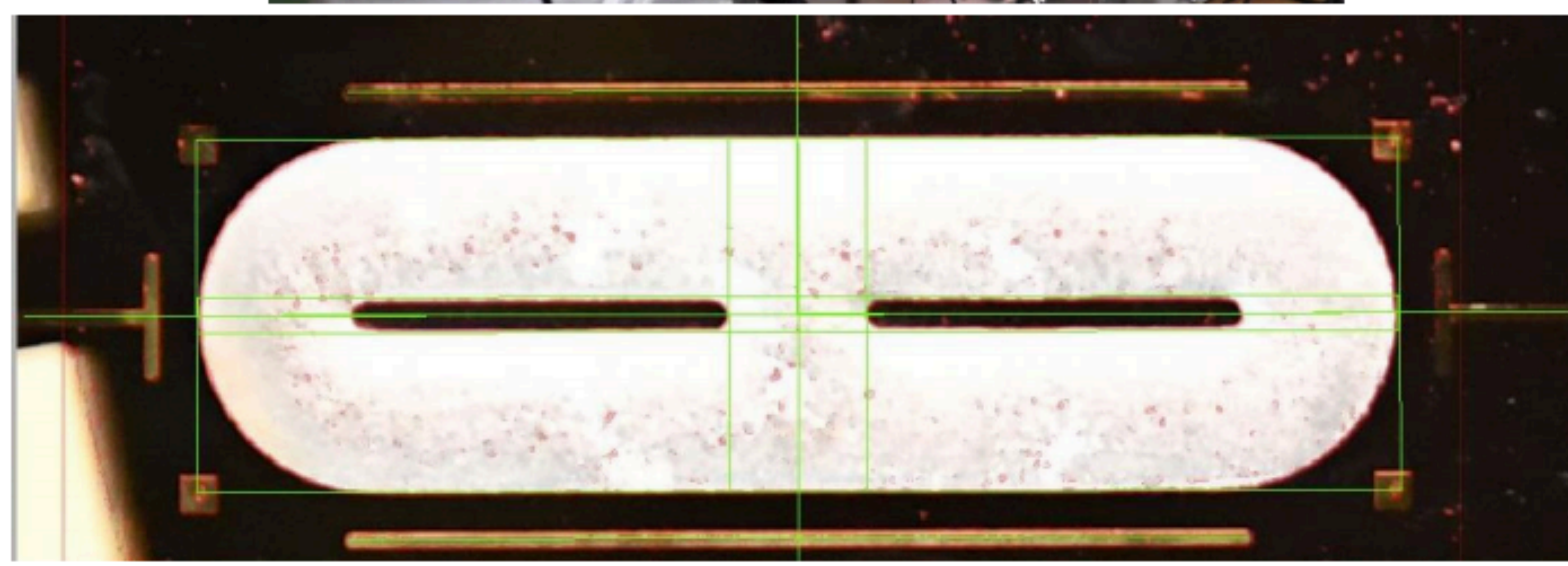
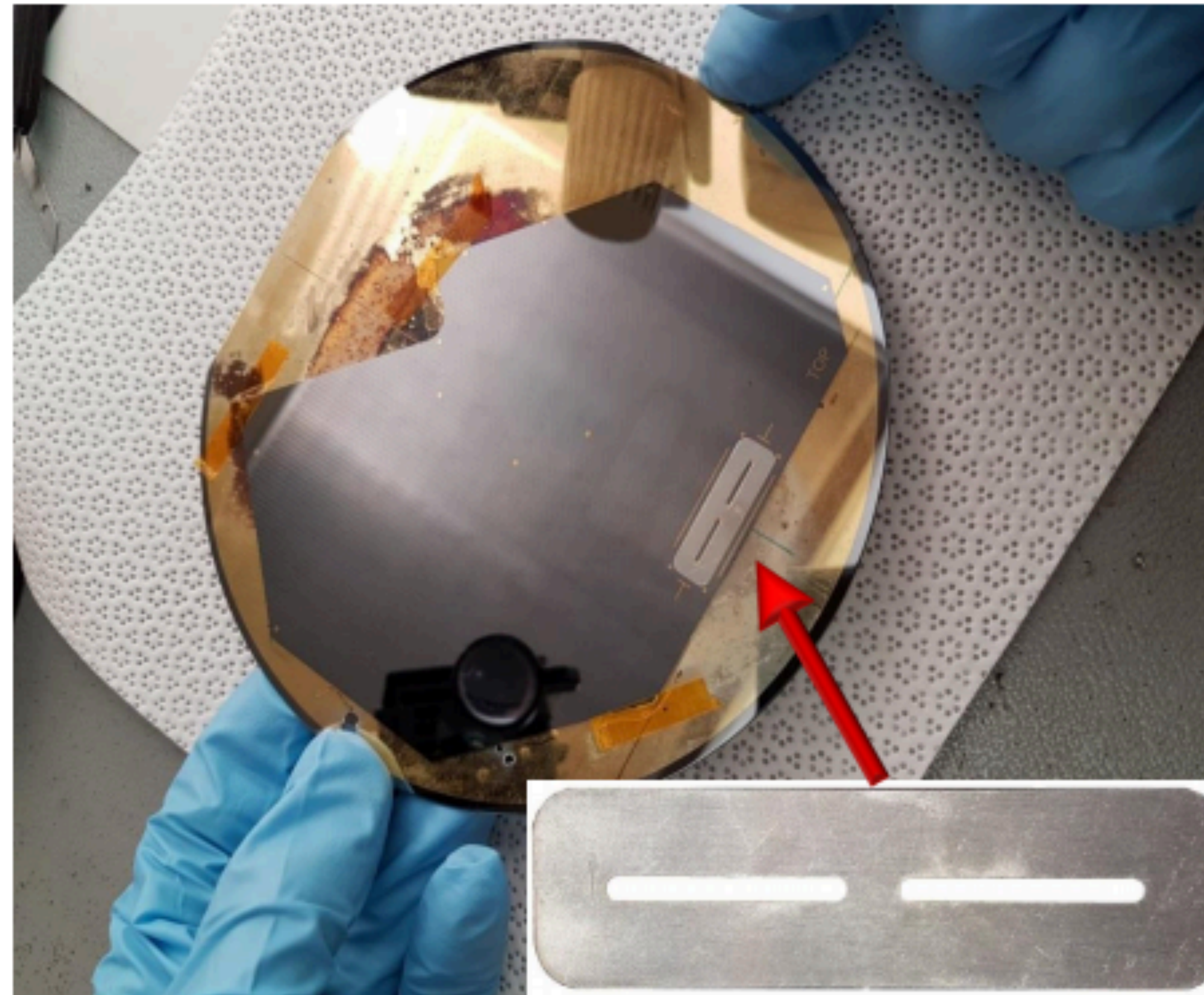


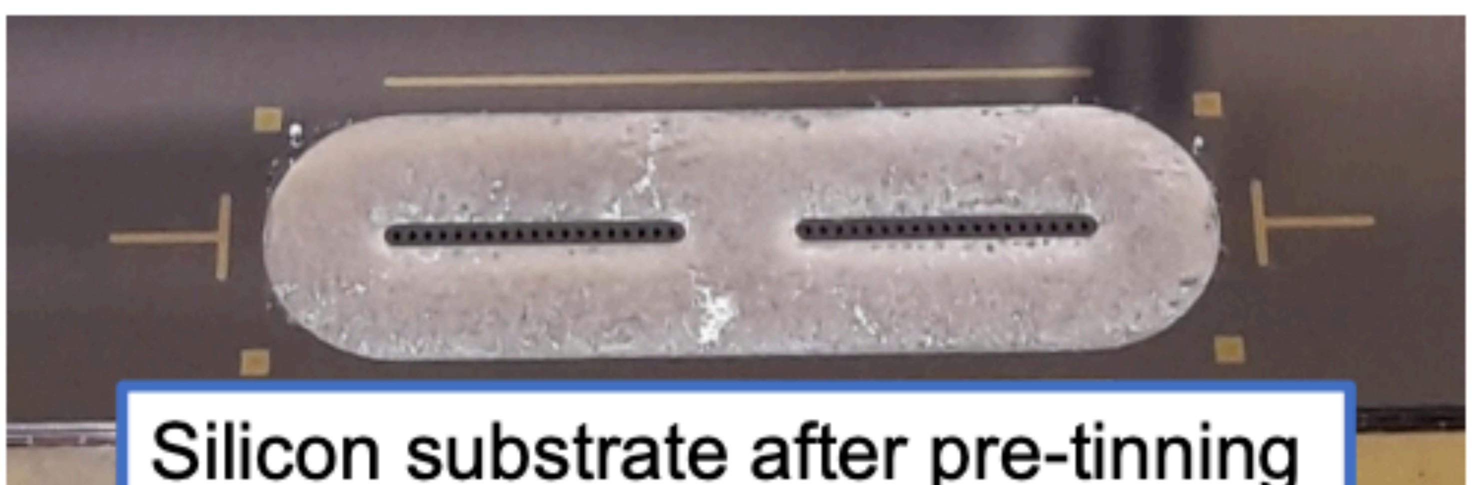
Photo processing software – **shape matching**

III Horizontal alignment: 3/3

Substrate plasma cleaning

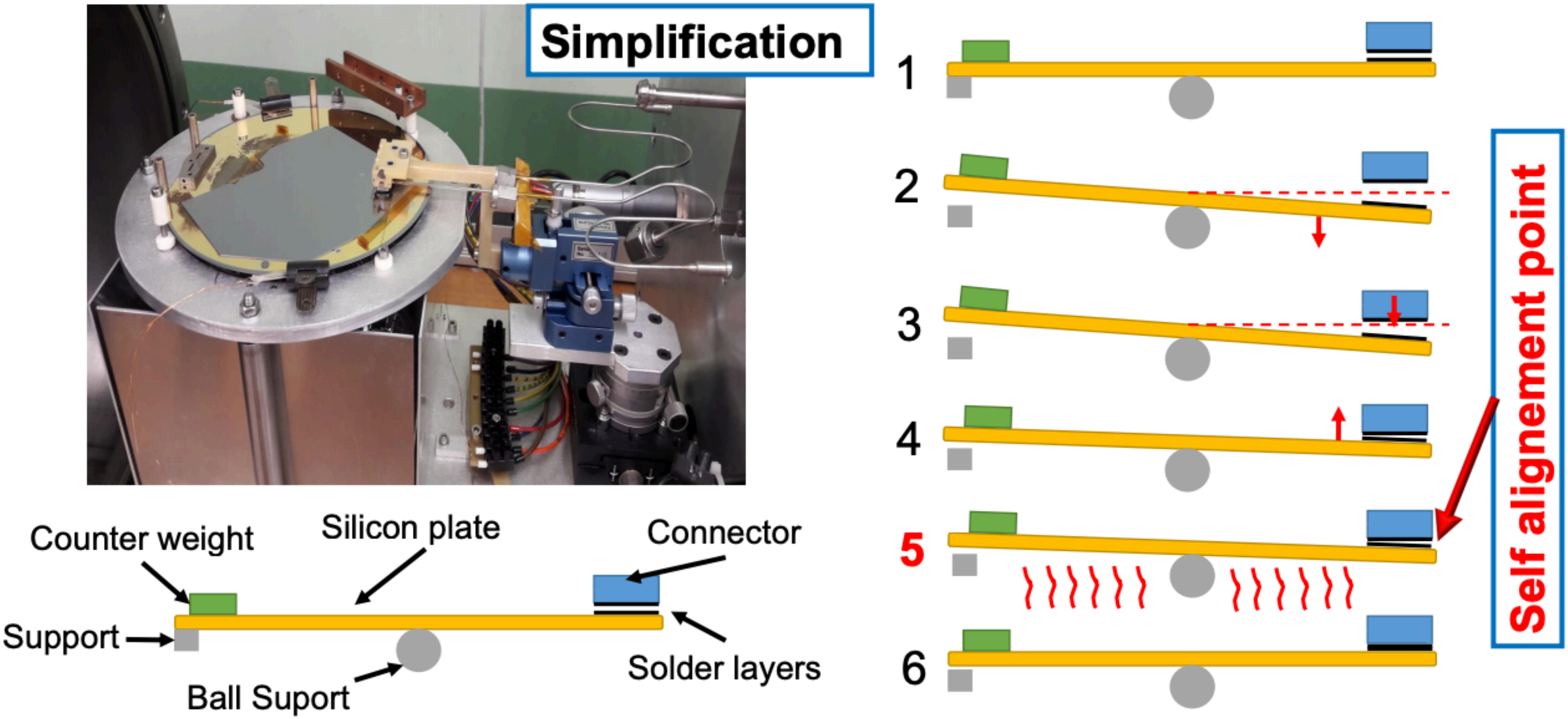


62Sn36Pb2Ag
100 [μm] preform

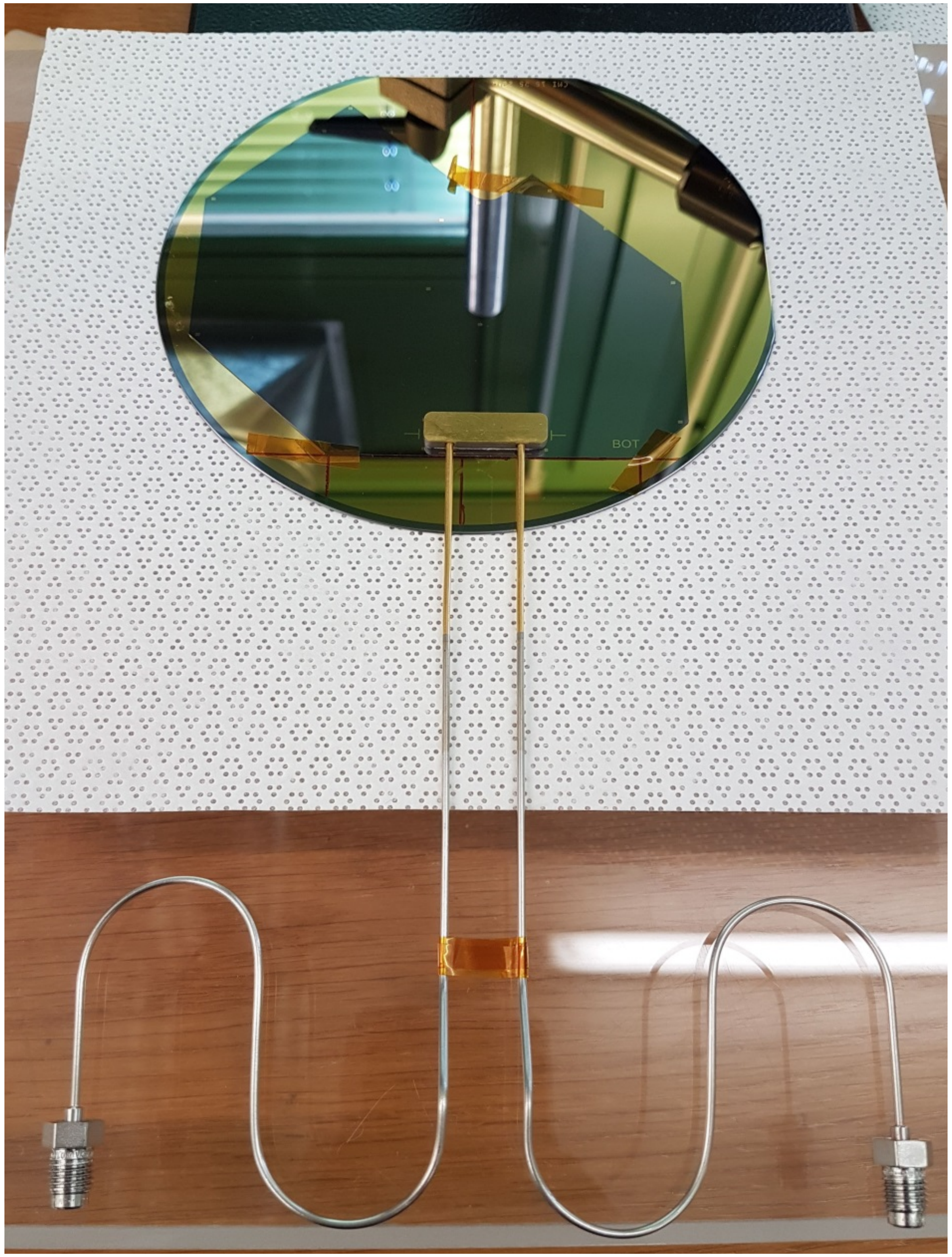


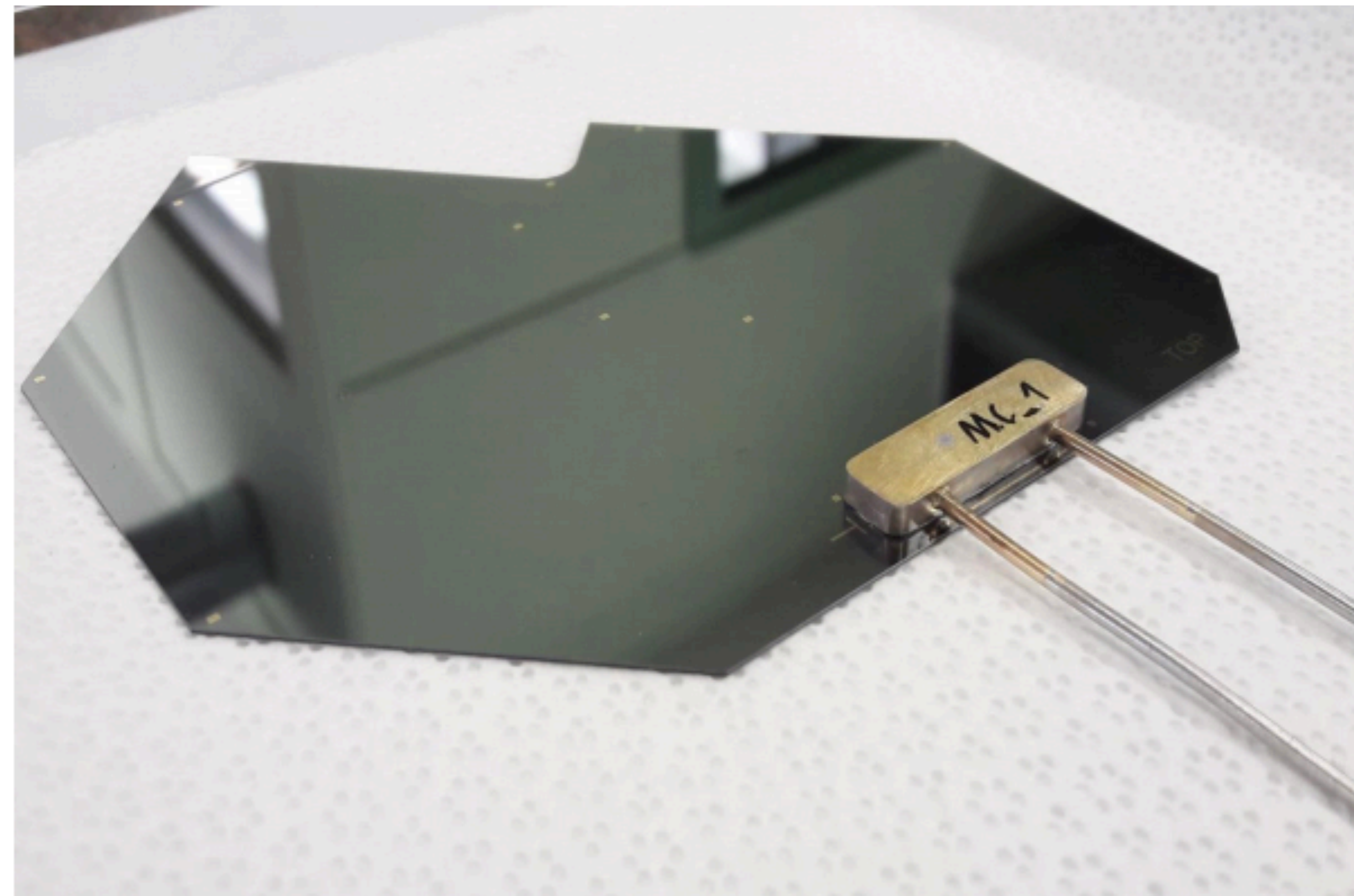
Silicon substrate after pre-tinning

IV Final soldering- self alignment



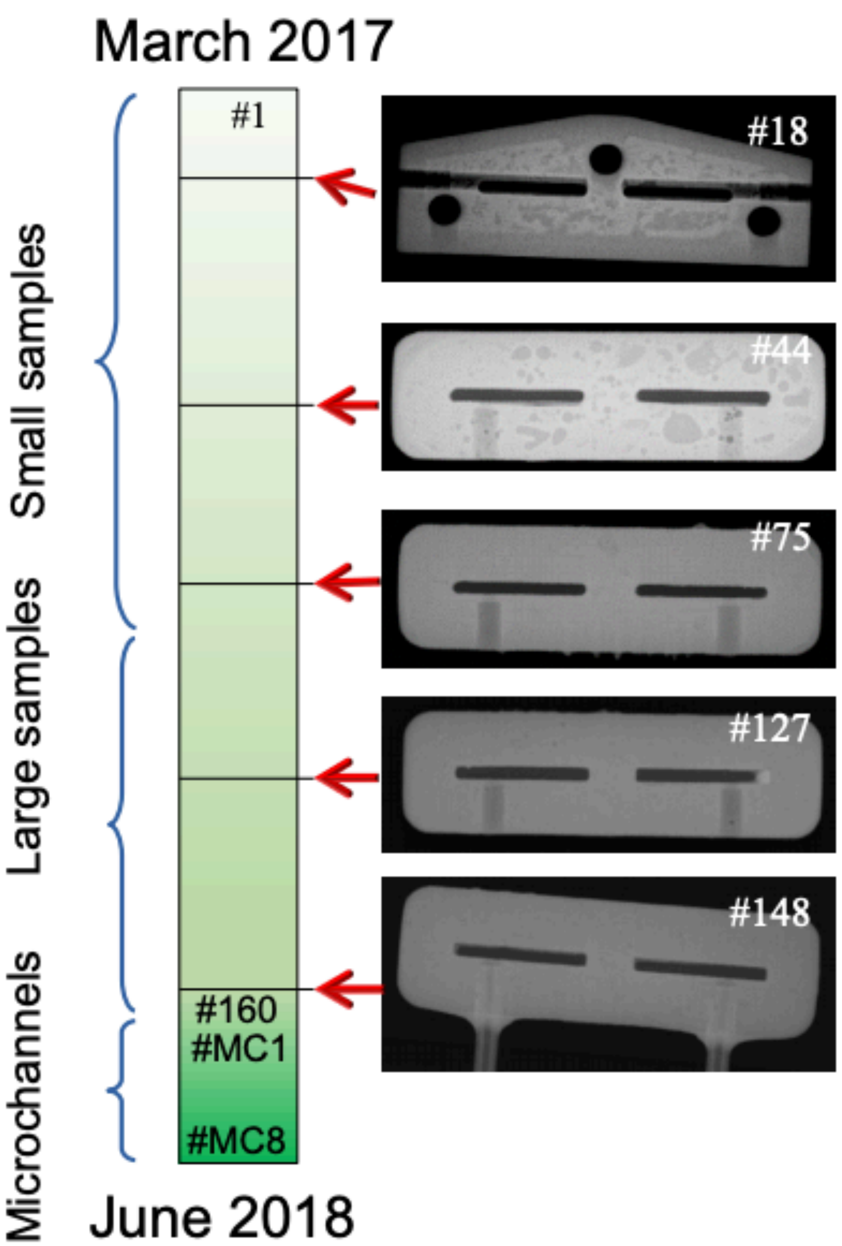
Substrate after soldering

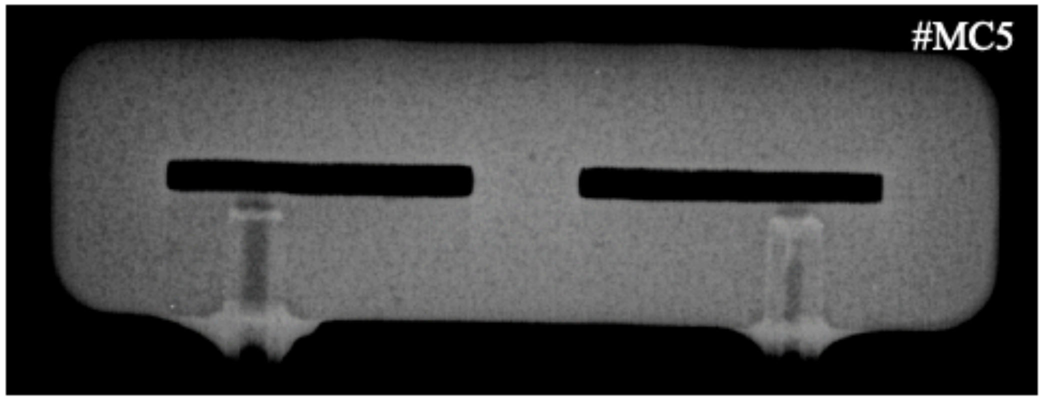




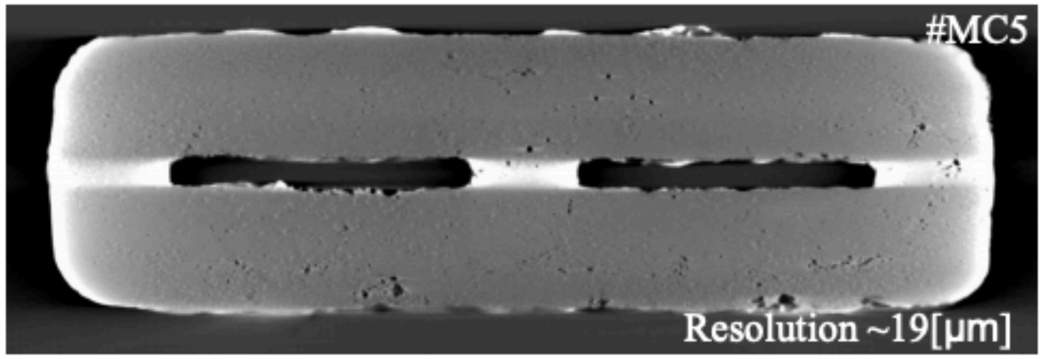
First substrate soldered 01/09/2017

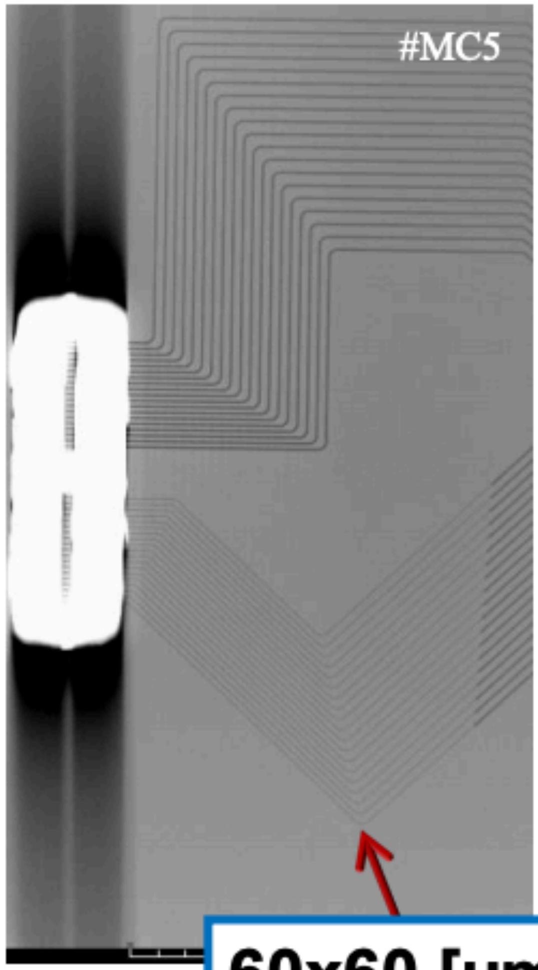
Soldering Results





X-ray

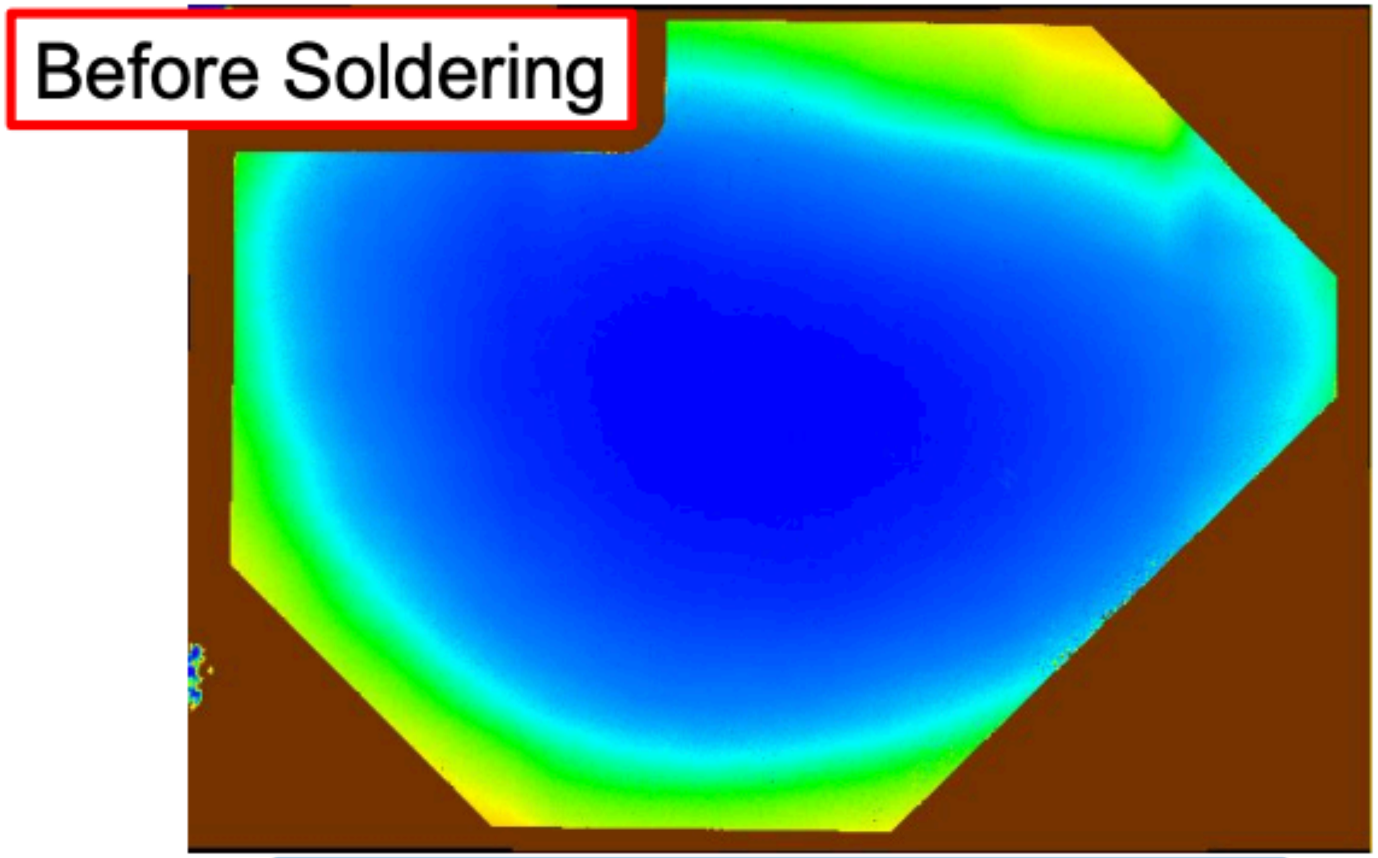


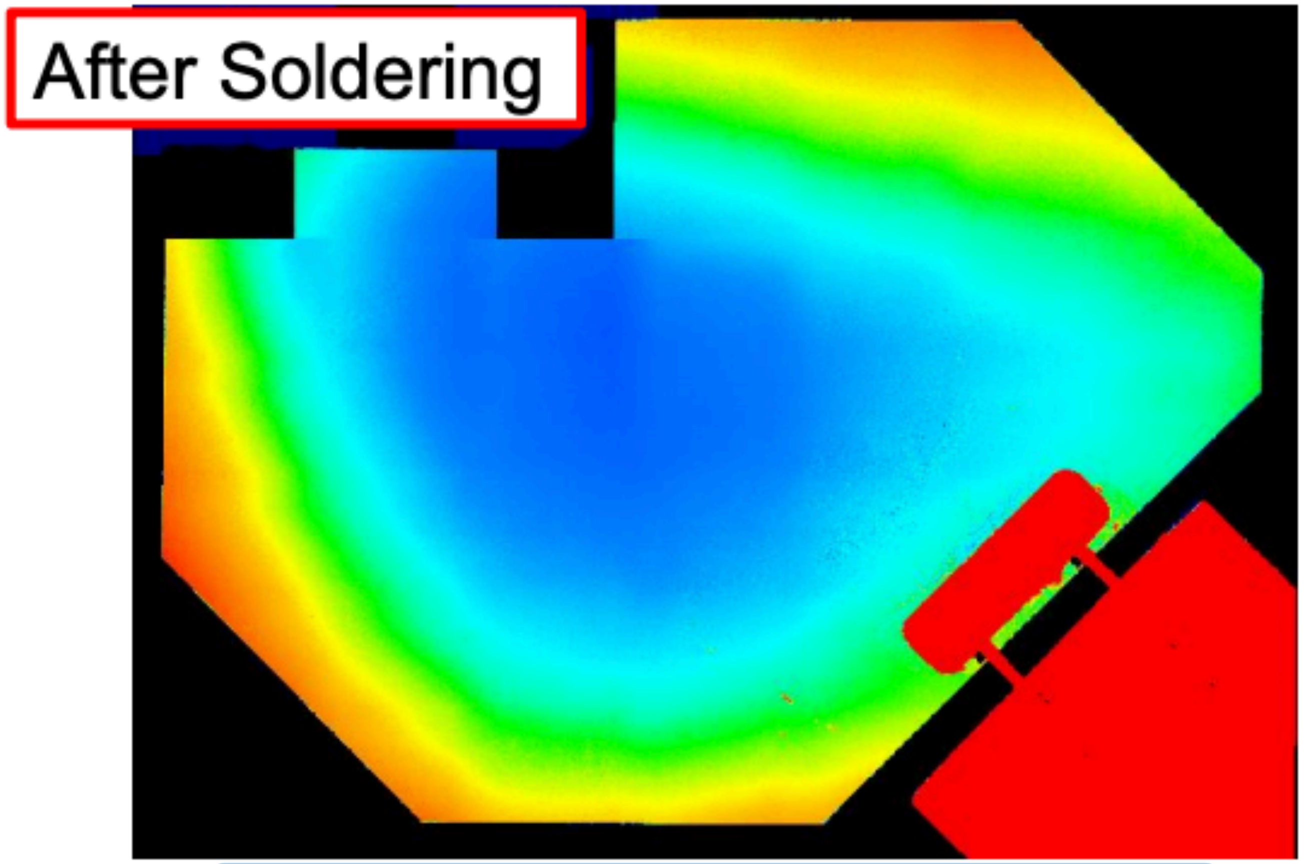


60x60 [μm]

3D X-ray tomography

Substrate Planarity



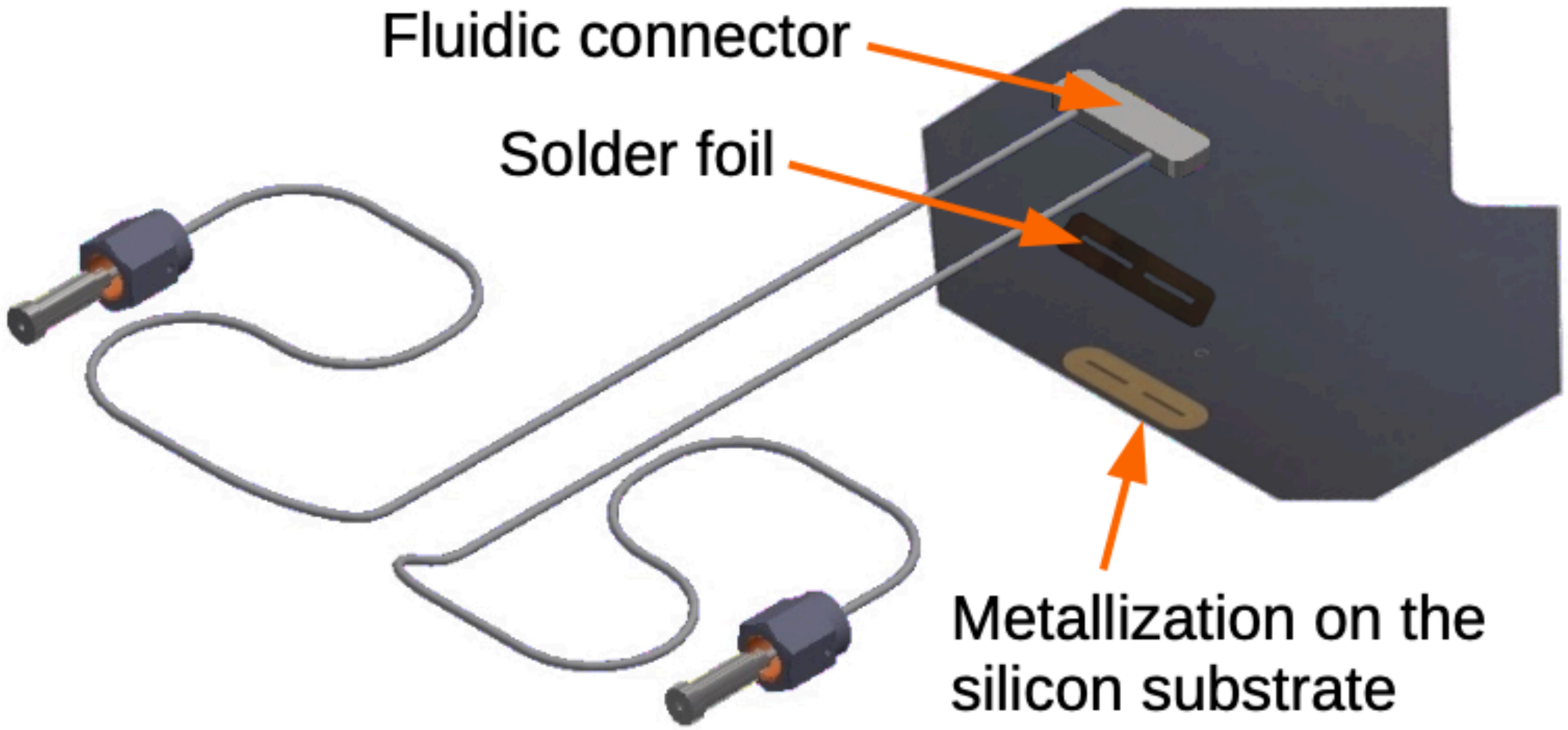


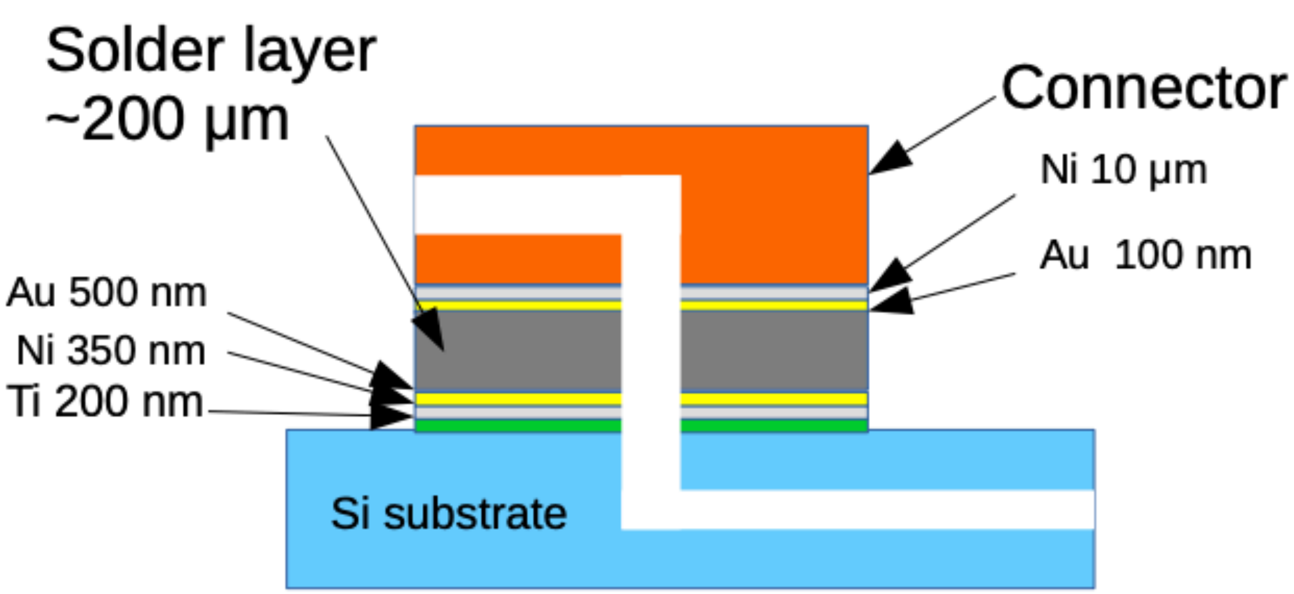
Before Soldering	
Max deviation:	+26 [μm]
Min deviation:	-60 [μm]
Total variation:	**86 [μm]**

After Soldering	
Max deviation:	+25 [μm]
Min deviation:	-50 [μm]
Total variation:	**75 [μm]**

No significant change on the planarity of the silicon plate.
Therefore, no significant stress generated by the soldering procedure.

Attachment of the fluidic connector





Challenges involved:
- Leak tight (modules are in the secondary vacuum)
- Planarity
- Voids on the solder layer
- No flux
- High pressure (up to 186 bar)

Experimental setup

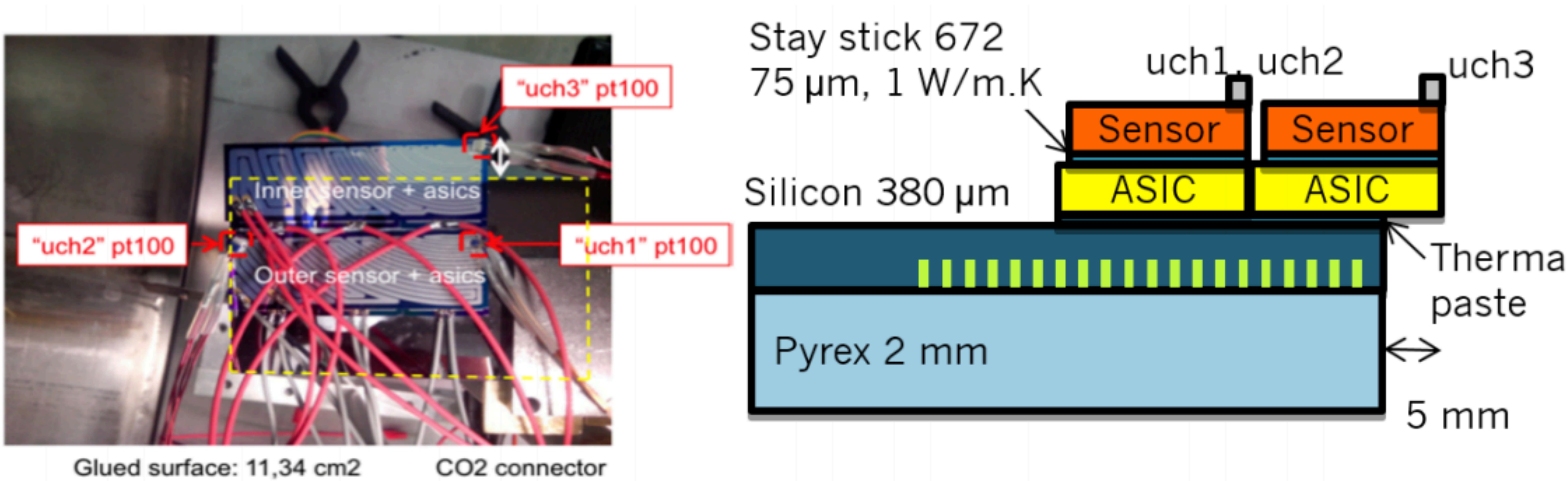
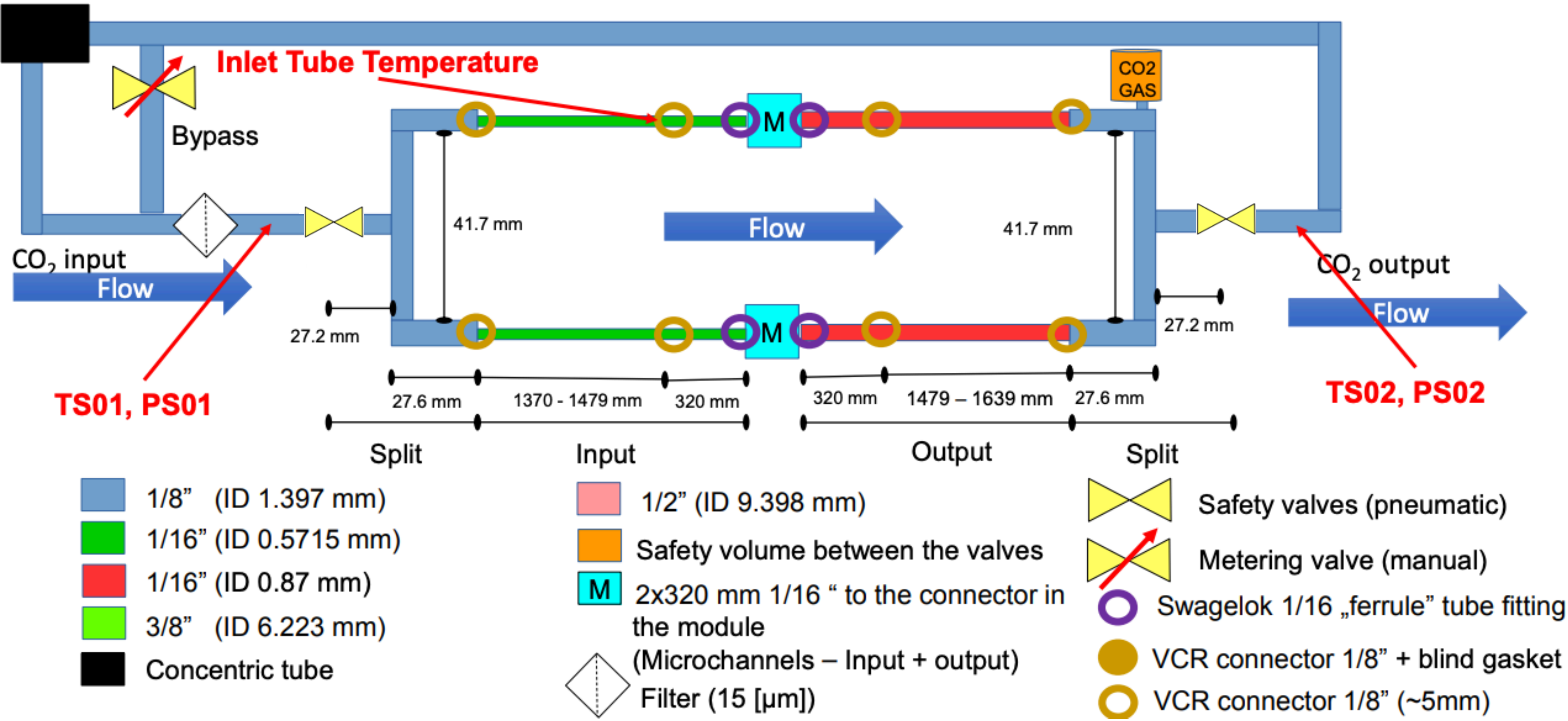
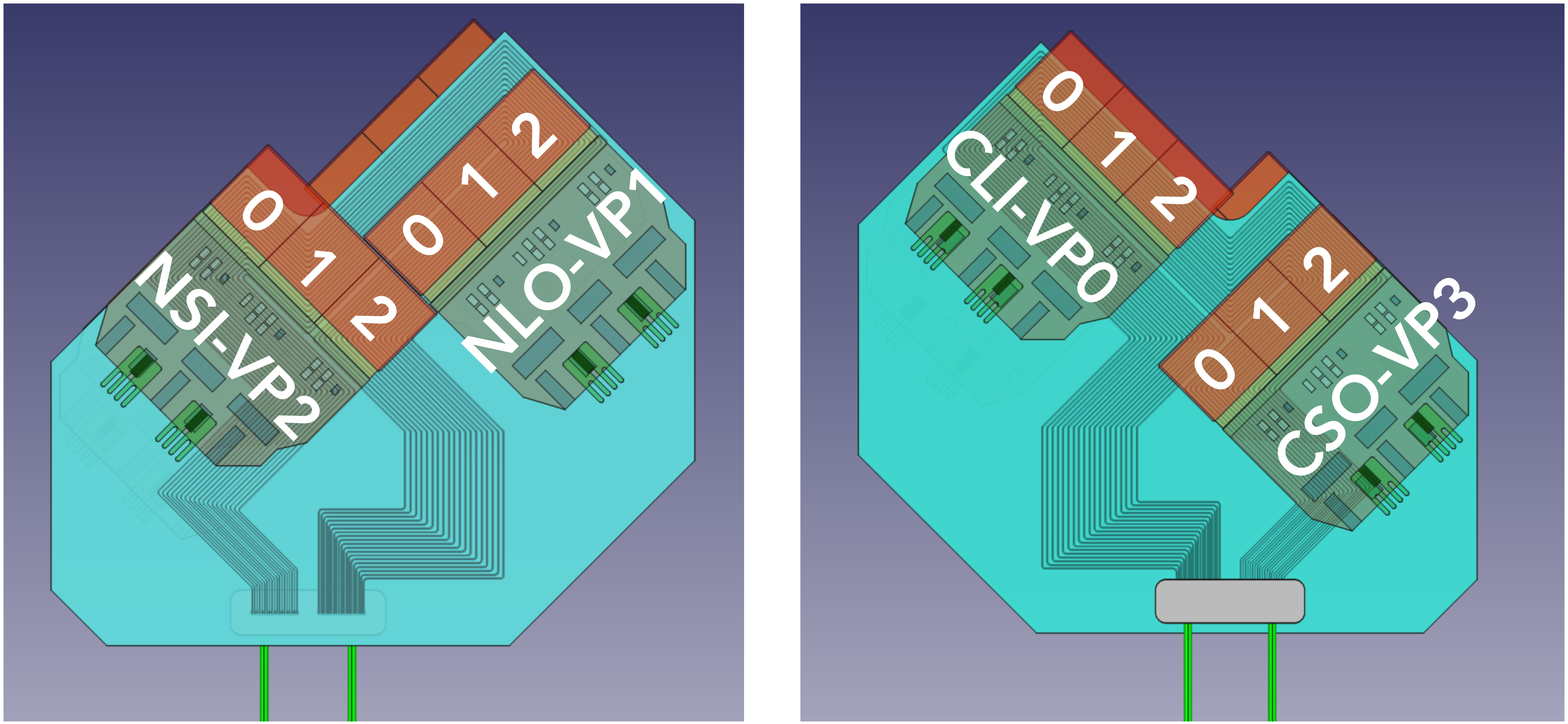


Figure 6: Experimental setup used to evaluate the cooling performance of the micro-channels.

Setup design



Module schematic



VeloPix: temperature monitoring

- The Band-Gap circuitry is used to generate a stable voltage reference for the DACs
- A PTAT circuit is used to monitor the temperature on-chip
- A simulation of this circuit shows a **~1.9 mV/°C** temperature dependent slope

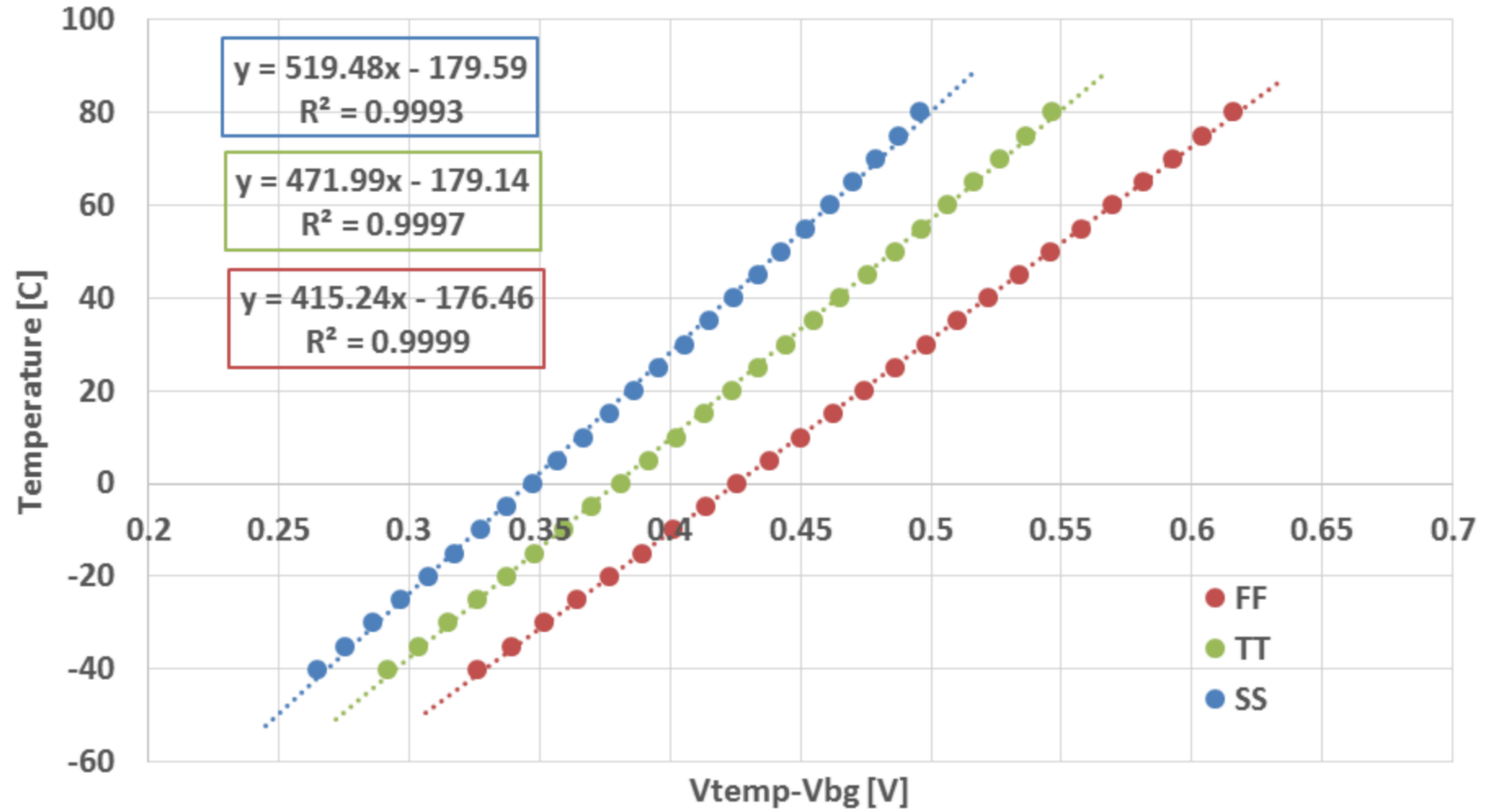


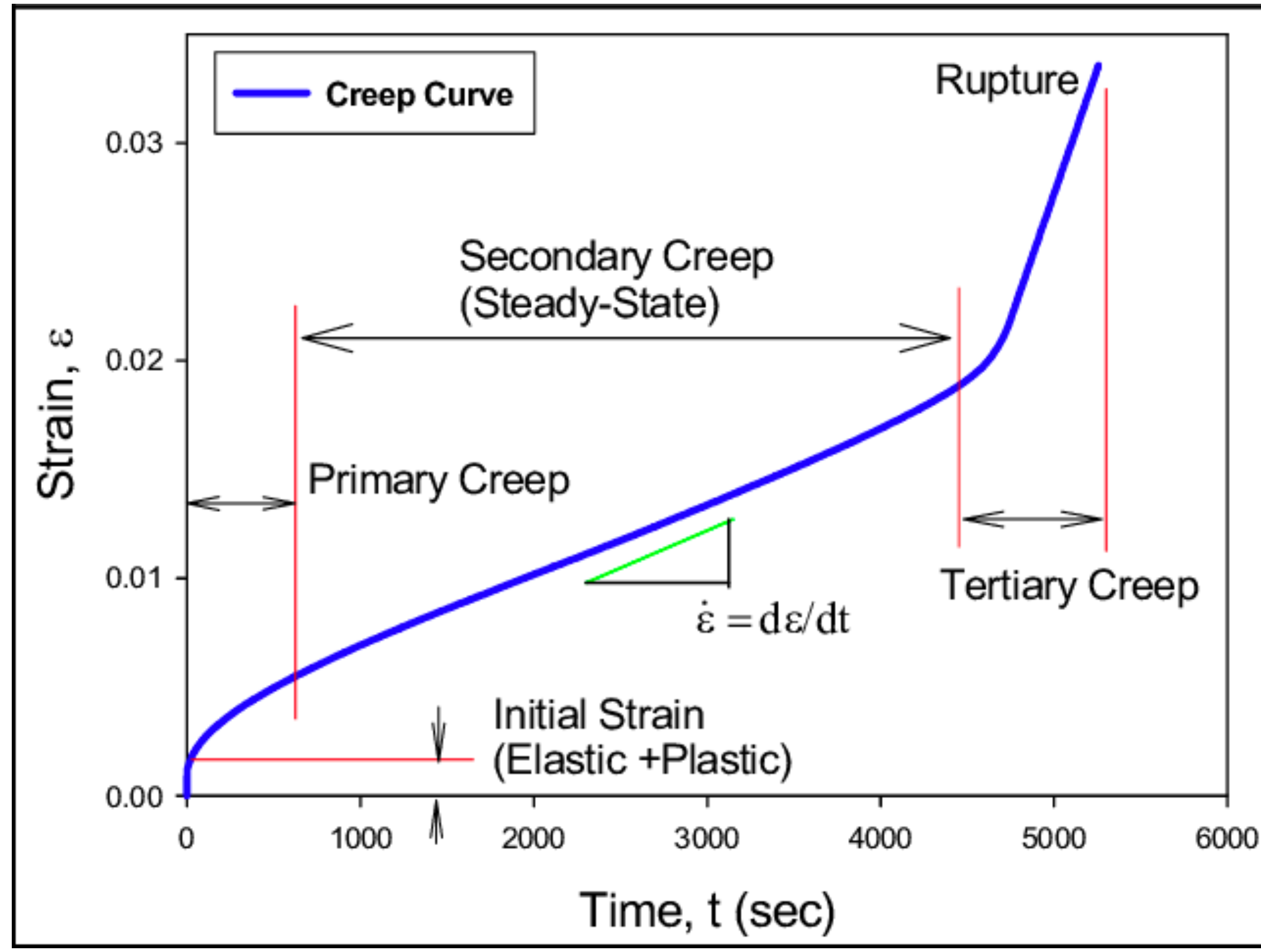
Figure 5. Simulated temperature measurement in VeloPix.

- The on-chip Velopix temperature is calculated by measuring the PTAT temperature (Band gap temperature voltage output) and the Band gap voltage output internal monitoring voltages
- From simulations the slope and offset has been extracted

Creep effect in the solder joint

"Plastic deformation of a material at very low mechanical stress levels"

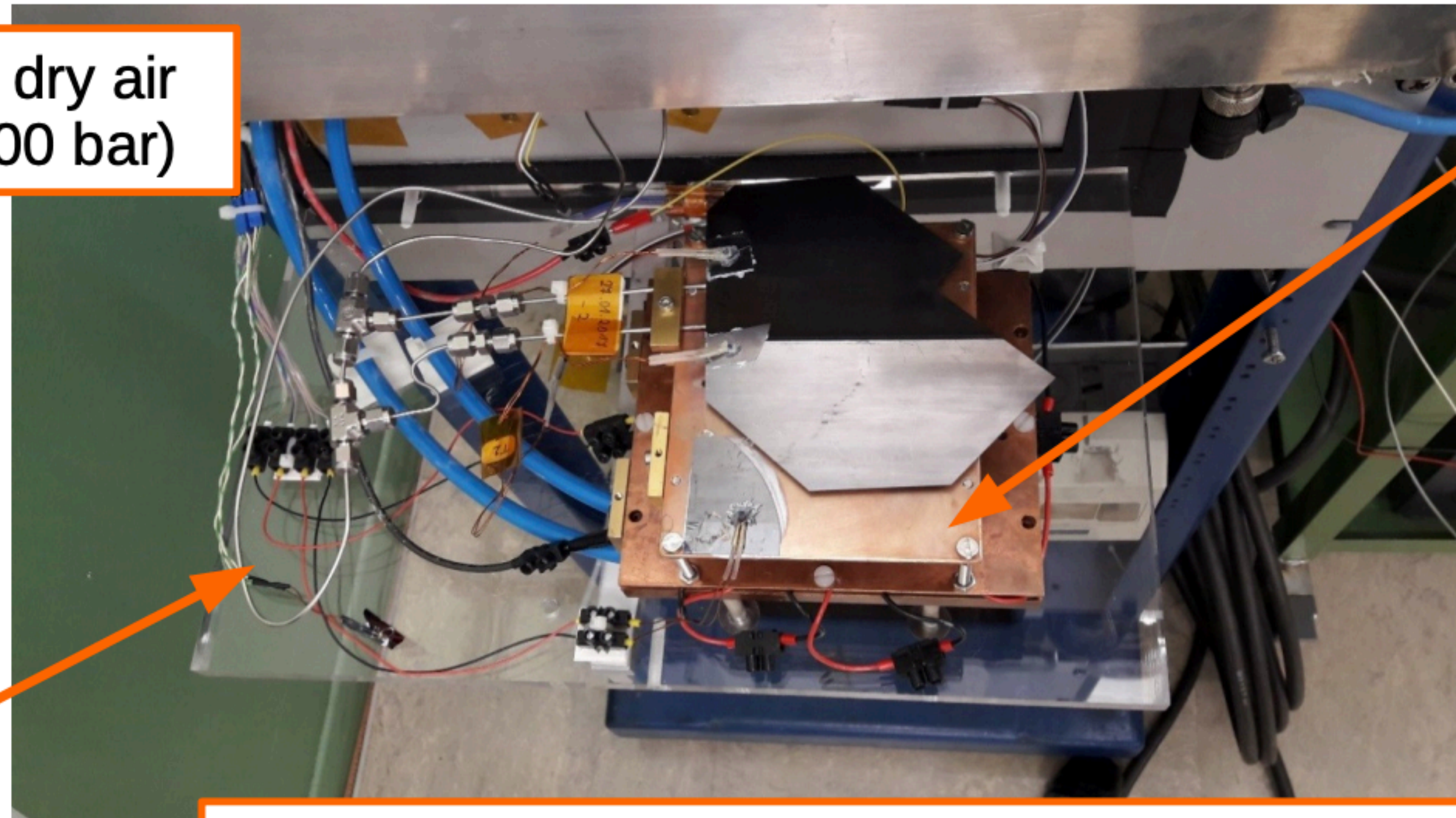
- Present in many materials. Stress can be caused by its own weight (e.g. glaciers or glass windows)
- Can lead to failure after long time
- Typically can be neglected only if: Temperature < T-critical T-critical = 50% of absolute melting Temperature
- For SnPb: T-critical = - 46 [°C]
- VELO should be at - 30 [°C], so expect very small creep effects.



Models exist for linear (secondary) region : e.g. *"A new creep constitutive model for eutectic solder alloy."* Shi, Wang, Zhou, Pang, Yang , 2002. Transactions of the ASME page 84, Vol124, June 2002.

Creep test

High pressure dry air bottle (up to 200 bar)



2 heaters of 50 W under the plate

Typically, this test was run at 60 bar and 120 ºC

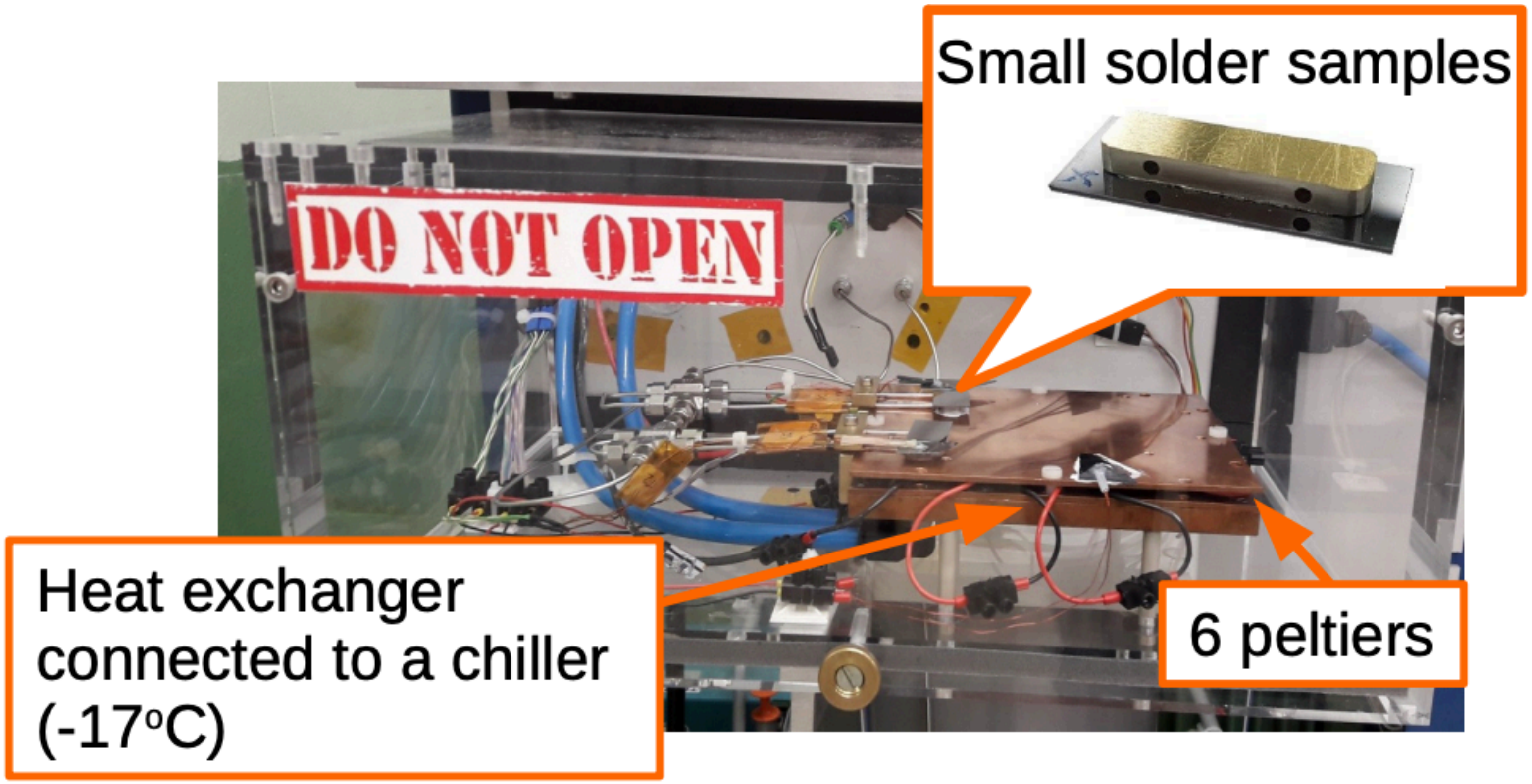
Summary of the test campaing:
Total number of samples: 18
Total number of hours: 2630 hours
Total number of hours: ~ 110 days

Fatigue test

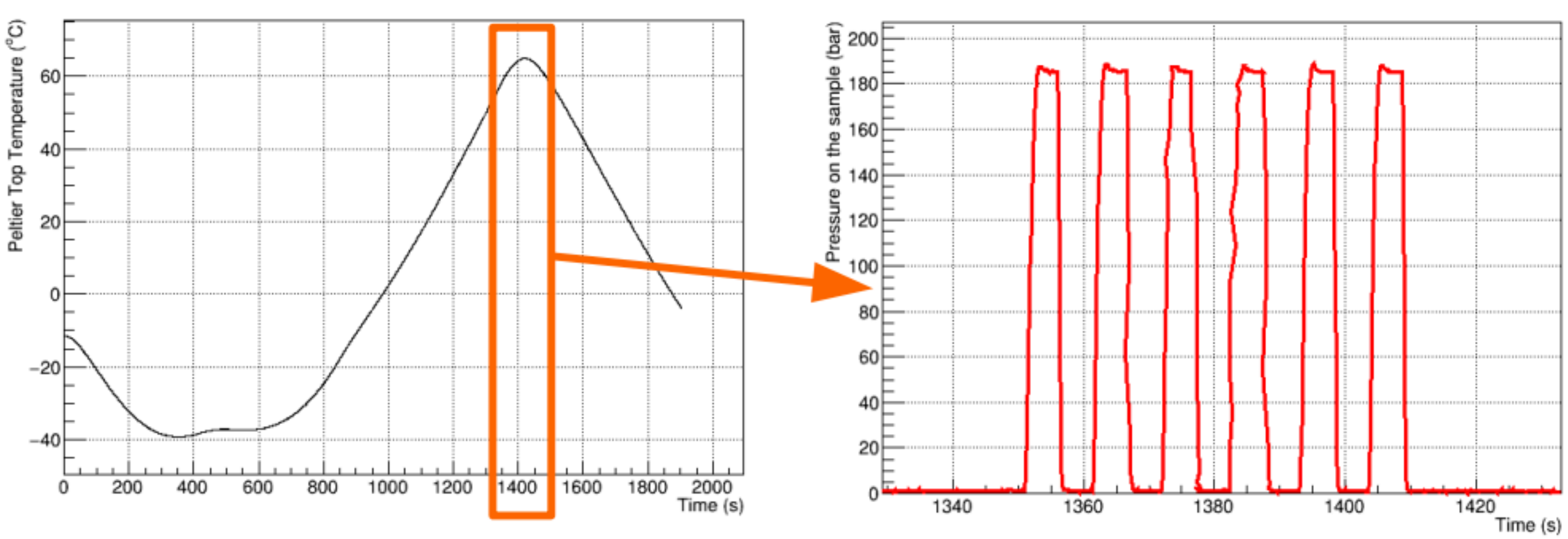
"**Fatigue is the weakening of a material caused by repeatedly applied loads.**"

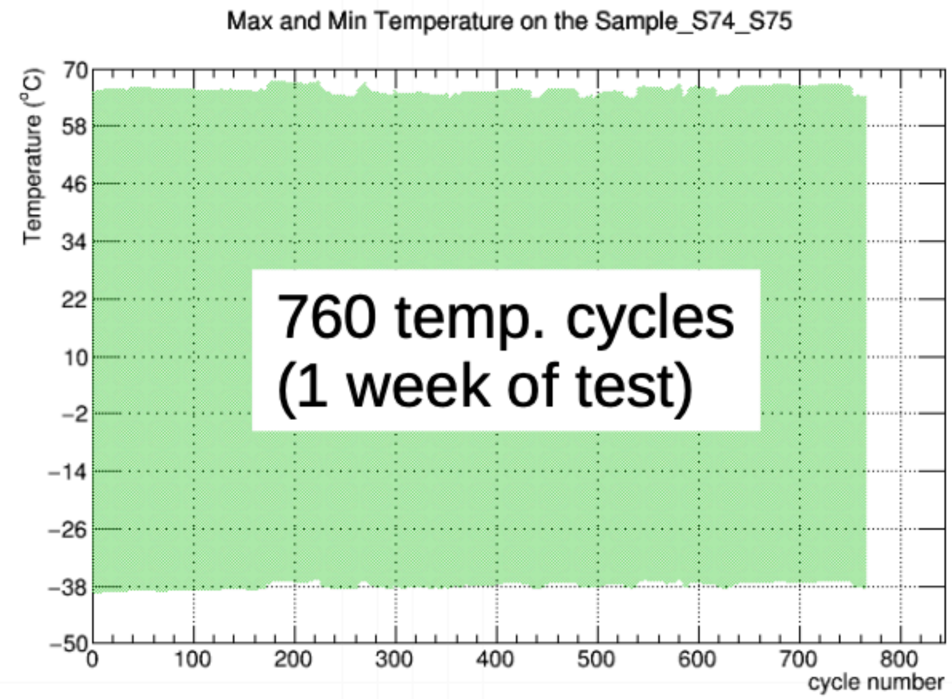
Effect occurs when a material is subjected to repeated loading and unloading.

Past Velo – Few hundred Temperature and Pressure Cycles (300 roughly)



Simultaneous temperature cycles and pressure cycles





Summary of tests:
Samples: 9
Total number of temp. cycles: 5232