AIDA2020 WP4

Task 4.4 Interconnections and TSVs

Main goal: produce Through-Silicon Vias in RD53A 65 nm CMOS wafers

Formal deadlines:

Deliverable D4.3 Through Silicon Vias production

(fabrication of TSV in wafers of RD53A engineering run)

M54 (October 31, 2019)

Milestone MS97 Test Report of Deliverable D4.3.

(test results on Through-Silicon Via (TSV) interconnects in RD53A 65 nm CMOS wafers)

M58 (February 28, 2020)

- AIDA2020 purchase of 4 CMOS 65nm wafers from RD53 was formally agreed in December; wafers should be available soon.

- In the end, if we get 1 working wafer with TSV we may consider that the AIDA2020 goal is accomplished.

- TSV process setup is connected with destructive inspection at wafer level. The gds2 layout data of M1-2 BEOL-layer with location of TSVs is needed and the backside RDL design with contact pads.

- For AIDA2020 goals, it is not strictly needed to assemble finally complete modules with these chips

- In the WP4 CERN budget, we have 81,600 CHF that we agreed to spend for wafer purchase and TSV processing. We should get a quote for TSV processing soon.

- To avoid duplicating the effort to demonstrate the feasibility of TSVs in 65 nm chips, AIDA2020 could make the 4 RD53A wafers available to Bonn for TSV studies, and also give additional support using the money that we have for this in WP4.