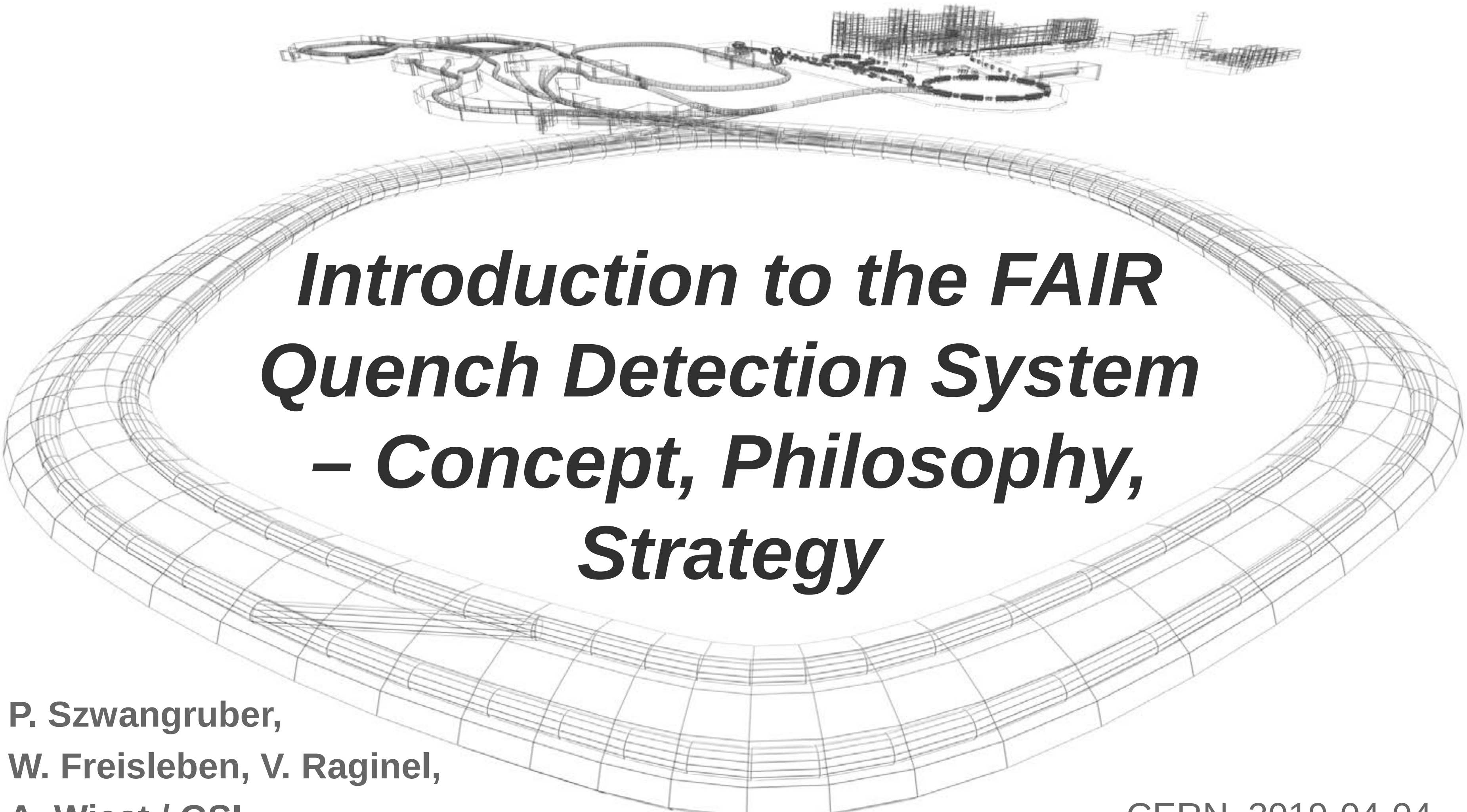

Introduction to the FAIR Quench Detection System – Concept, Philosophy, Strategy

P. Szwangruber,
W. Freisleben, V. Raginel,
A. Wiest / GSI

CERN, 2019-04-04

Outline

- FAIR Project
- Super-FRS
  - large aperture super-ferric magnets
  - magnet protection
- SIS100
  - main superconducting magnet circuits and their protection
  - bus-bars and main current leads
  - correctors magnets their bus-bars and local current leads
- FAIR Quench Detection Electronics
- Summary

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- FAIR Project
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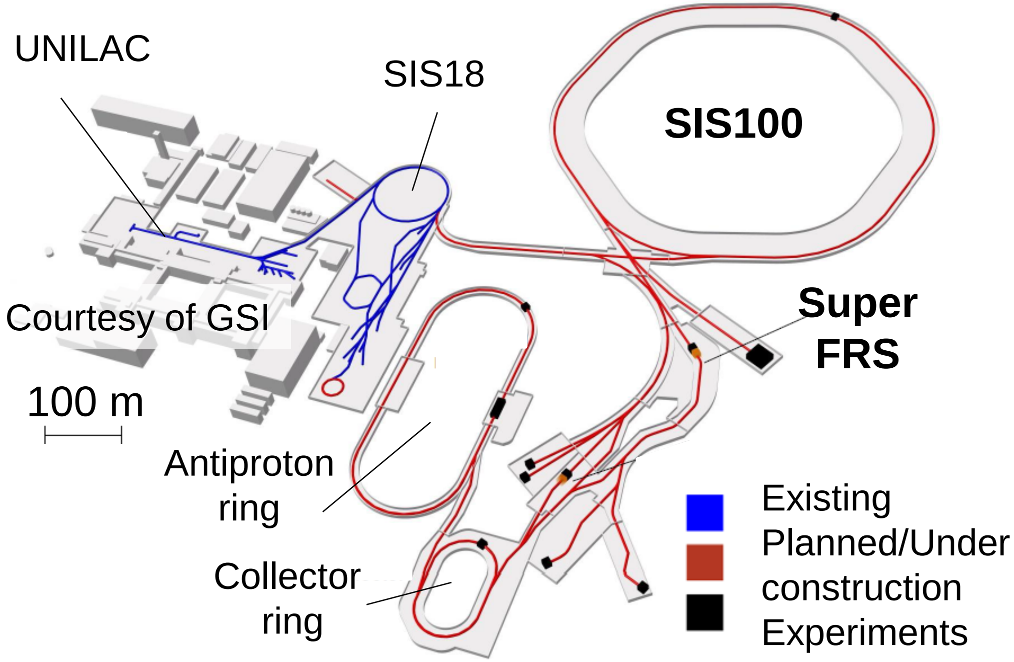
- Summary

FAIR Project – a new international accelerator facility in Darmstadt, Germany.

Physics research program addresses broad variety of topics ranging from fundamental questions of the evolution of the universe to the structure of matter.

Linear acc. UNILAC (GSI) **upgrade↑**
NC synchrotron SIS18 (GSI) **upgrade↑**

pre-acceleration

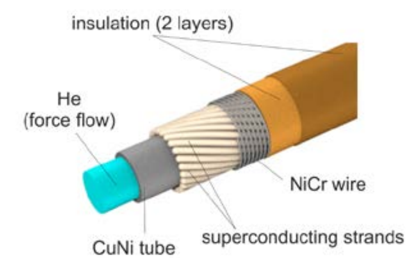


injection to → sc synchrotron **SIS100**

- ❑ fast cycling machine (2 T, 4 T/s)

→ experiments
→ storage rings

Nuclotron-type cable



Antiproton and collector rings – beam storage and modification for various experiments

→ **Sc FRagment Separator Super-FRS**

- ❑ magnetic spectrometer for the study of exotic particles.

Super-FRS

World's Superconducting Fragment Separators

A1900 at National Superconducting Cyclotron Laboratory (NSCL), Michigan State University (MSU), USA

BigRIPS at Institute of Physical and Chemical Research (RIKEN) in Japan

Super-FRS at FAIR, Darmstadt, Germany

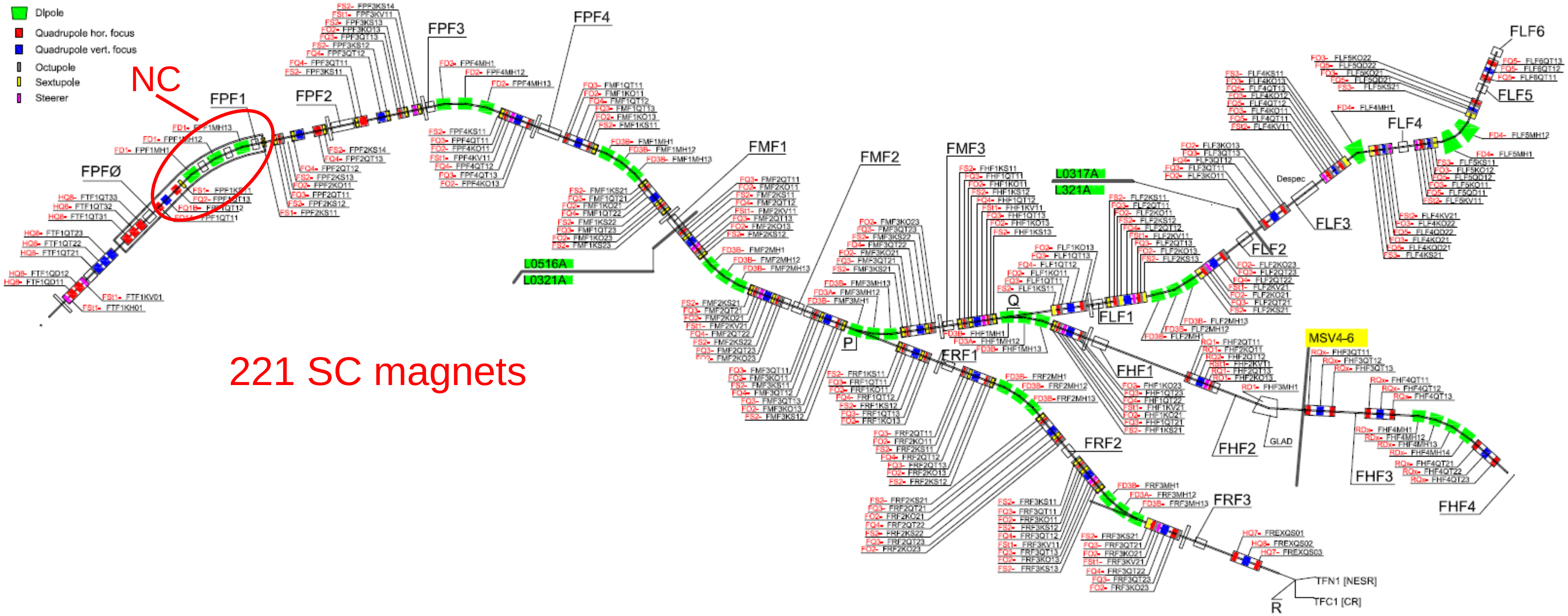
Dipoles

	A1900	Super-FRS
B_{gap} (T)	2	1.6
Gap (mm)	90	140
Bend Angle (°)	45	9.75
ϱ (m)	3.1	12.5
$B\varrho$ (T·m)	6.2	20
I_{n} (A)	171	245
L (H)	36.25	15
E_{mag} (kJ)	530	450

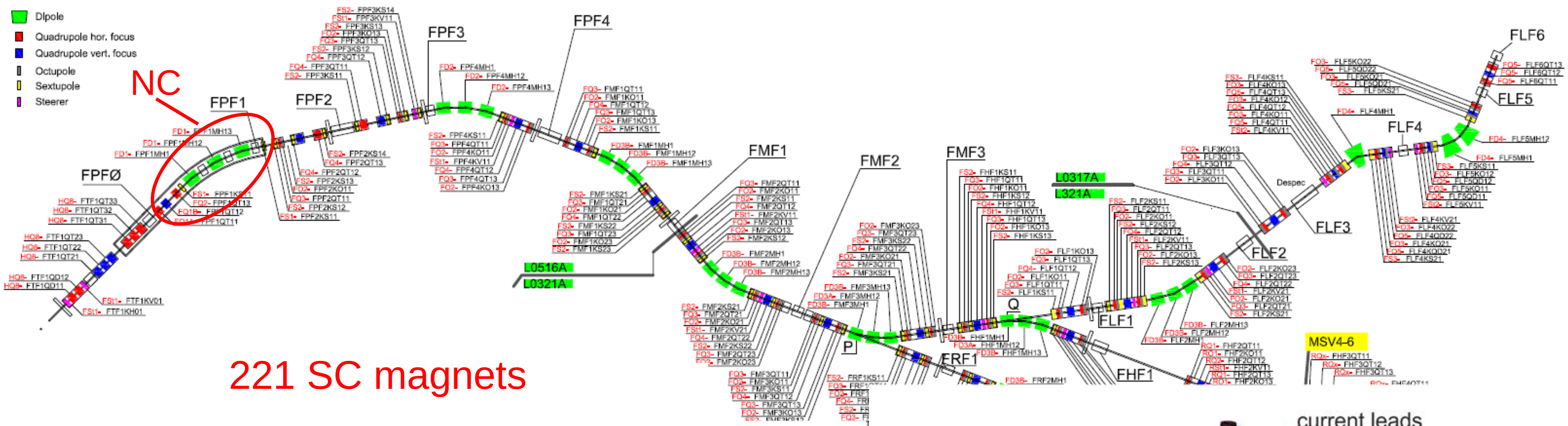
Quads

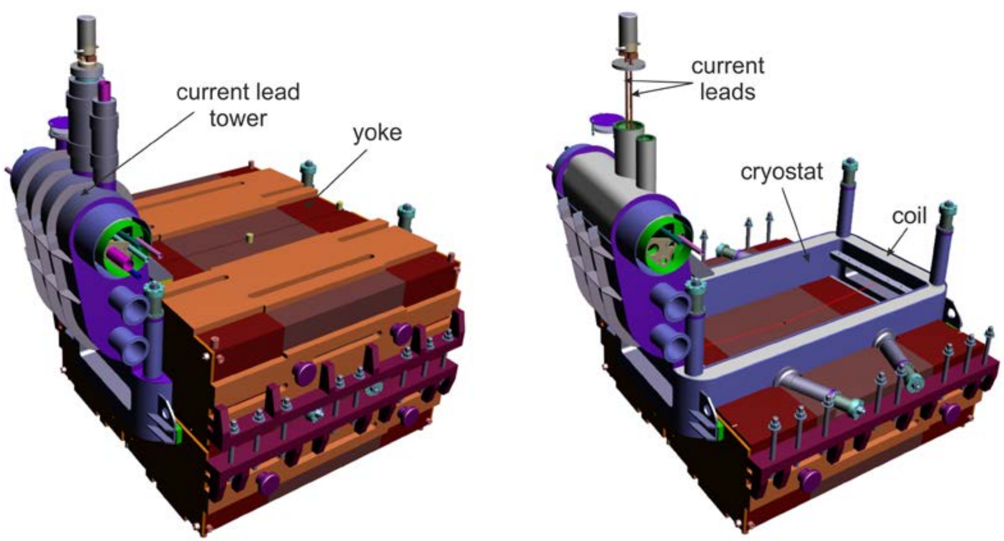
Machine	Field Grad. (T/m)	I_{n} (A)	L (H)	E_{mag} (kJ)
A1900 Type QD	11	404.5	5.08	372
BigRIPS Q1000	14.1	135	18-33	270
Super–FRS "long"	10	291	26.5	1120

Super-FRS

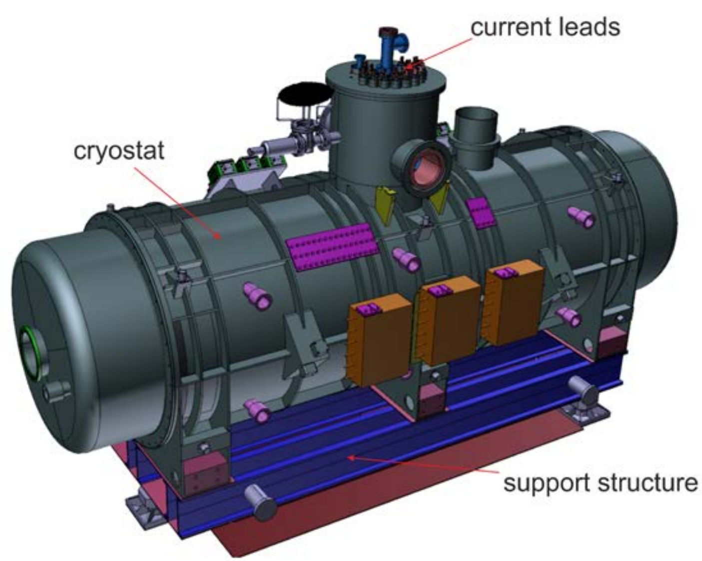

Dipole
Quadrupole hor. focus
Quadrupole vert. focus
Octupole
Sextupole
Steerer
NC
FPFØ
FPF1
FPF2
FPF3
FPF4
FMF1
FMF2
FMF3
L0516A
L0321A
L0317A
L321A
P
Q
FRF1
FRF2
FRF3
FLF1
FLF2
FLF3
FLF4
FLF5
FLF6
Despec
FHF1
FHF2
FHF3
FHF4
GLAD
MSV4-6
TFN1 [NESR]
TFC1 [CR]
R
221 SC magnets

Super-FRS


Dipole
Quadrupole hor. focus
Quadrupole vert. focus
Octupole
Sextupole
Steerer
NC
FPFØ
FPF1
FPF2
FPF3
FPF4
FMF1
FMF2
FMF3
L0317A
L321A
L0516A
L0321A
Despec
FLF1
FLF2
FLF3
FLF4
FLF5
FLF6
MSV4-6
P
Q
ERF1
FHF1
221 SC magnets

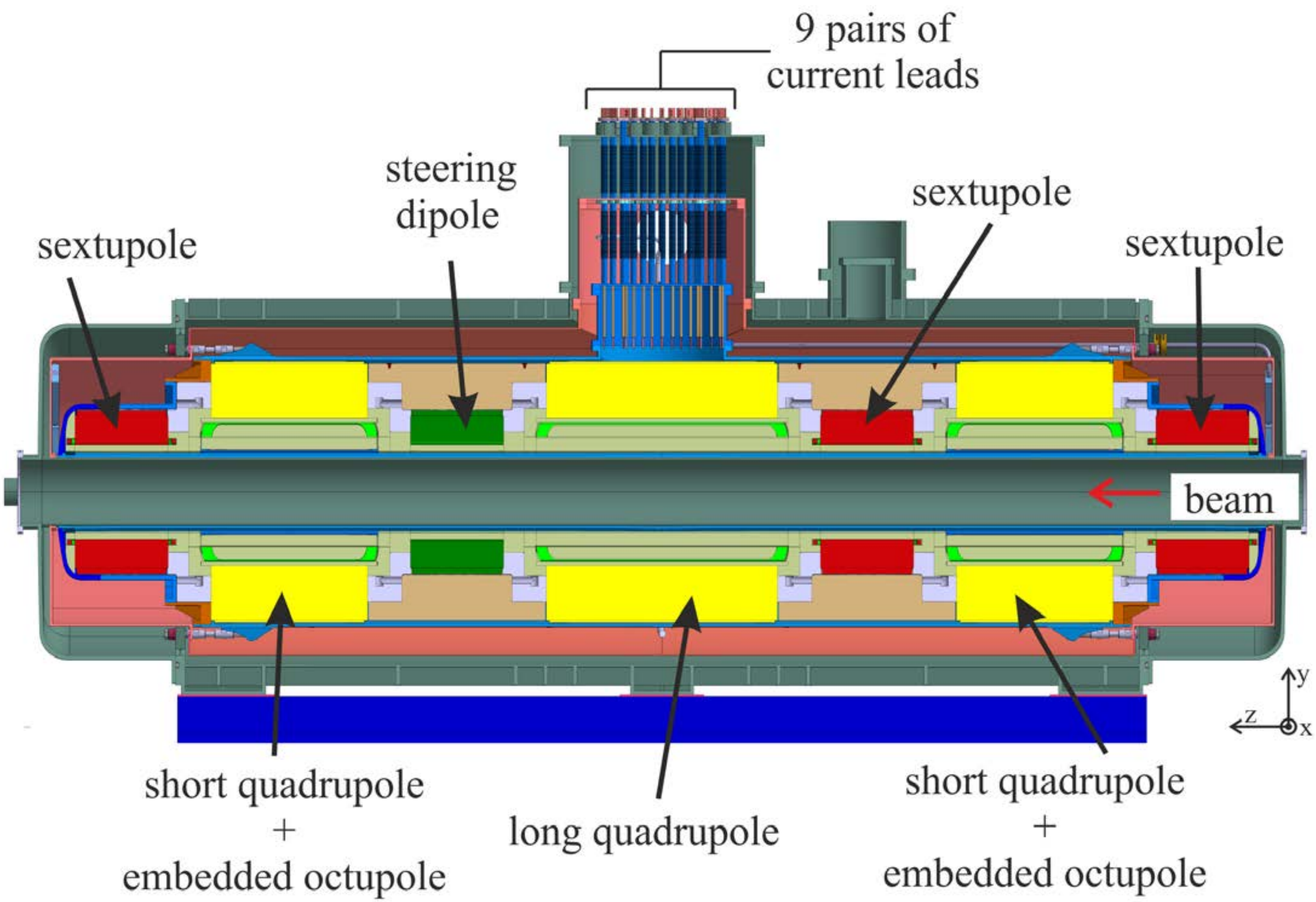

current lead
tower
yoke
current
leads
cryostat
coil

(a) (b)


current leads
cryostat
support structure

Super-FRS Multiplets

up to 9 magnets in a common He bath...

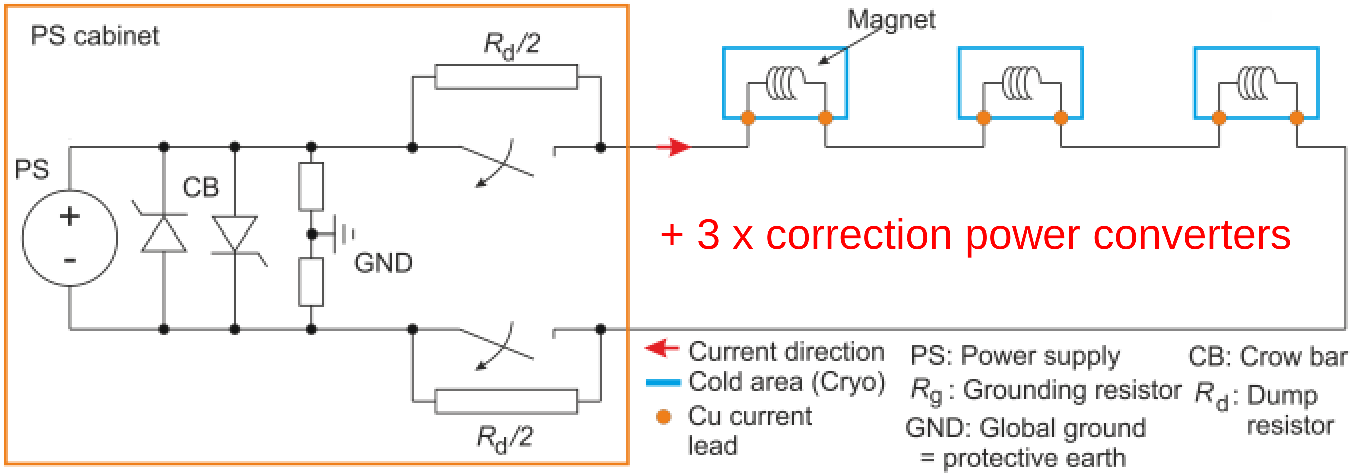


Super-FRS Magnets Parameters

		Multiplet magnets					Dipoles		
		Long Quadrupole	Short Quadrupole	Sextupole	Steering magnet	Octupole	9.75 (D3)	11 (D2)	Branch (D3Y)
Max. inductance L	H	43.2	30.41	1.06	0.0665	0.097	23	26	24
Max. operation current Iop	A	300	300	291	280	163	<250	<250	280
Max. test current (110%)	A	330	330	320	308	179	275	275	308
Rising time for operation T	sec.	120	120	120	120	120	120	120	120
Max. inductive voltage =LIop/T	V	108.0	76.0	2.6	0.2	0.1	47.9	54.2	56.0
Stored energy at Iop	kJ	952	670	37	2.6	1.3	572	666	490

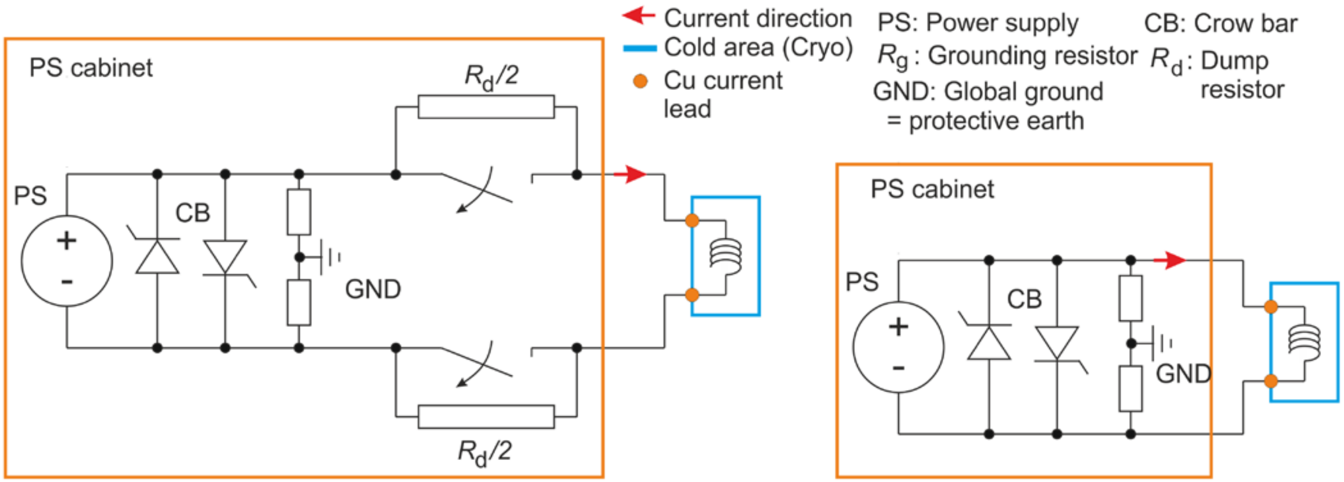
Super-FRS Magnets – Powering Circuit

Dipoles



Quads

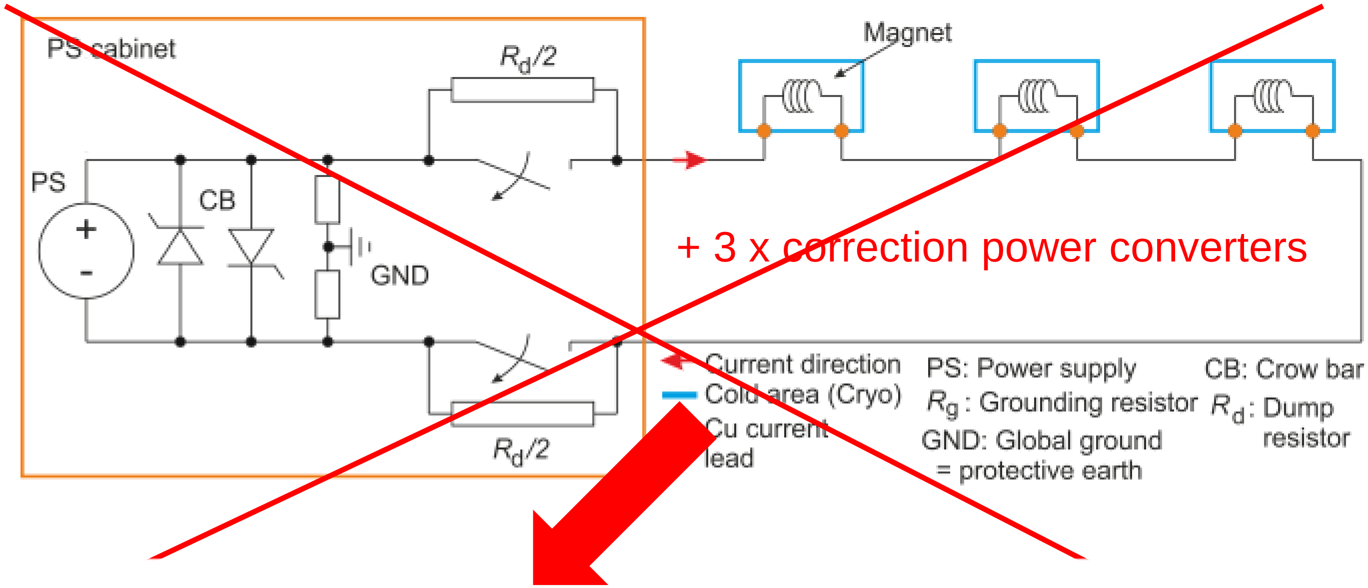
Correctors



(a) (b)

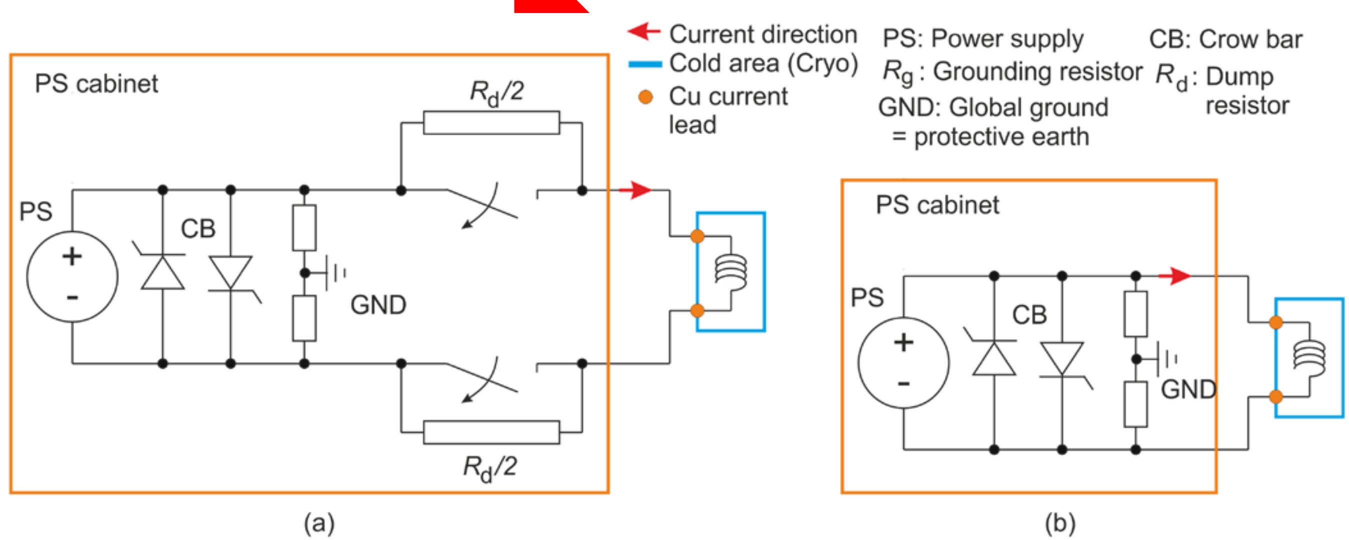
Super-FRS Magnets – Powering Circuit

Dipoles



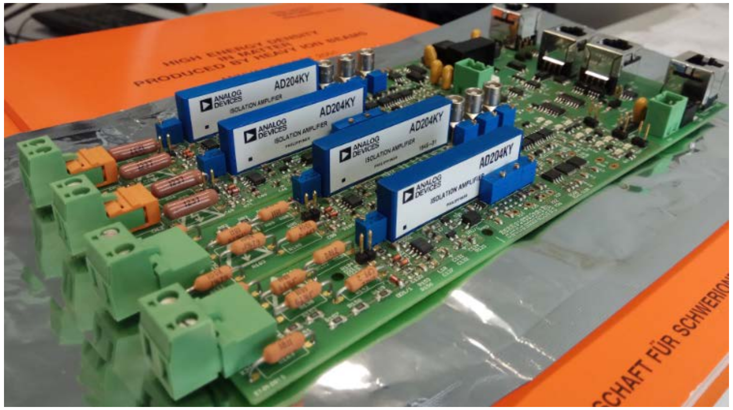
Quads

Correctors



Super-FRS Quench Detection

- All magnets powered individually
- Location of the quench detectors in the power converter cabinets make perfectly sense
- Cabinet infrastructure, interlock card, MFU, SCU available



- Opportunity to merge the development with SIS100

SIS100

World's Superconducting Particle Accelerators

Accelerator	Circumference (km)	B_{dipole} (T)	$B\varrho$ (T·m)	$\frac{dB_{\mathrm{dipole}}}{dt}$ (T/s)	Years of operation
Tevatron	6.300	4.4	$3.3 \cdot 10^3$	0.29	1987-2011
HERA	6.336	4.682	-	0.007	1992-2007
Nuclotron	0.252	1.98	45	2	1993-
RHIC	3.834	3.45	839.5	0.07	2000-
LHC	27	8.36	$23 \cdot 10^3$	0.008	2009-
SIS100	1.0836	1.9	100	4	2022-
SIS300	1.0836	4.5	300	1	-

SIS100 vs. LHC

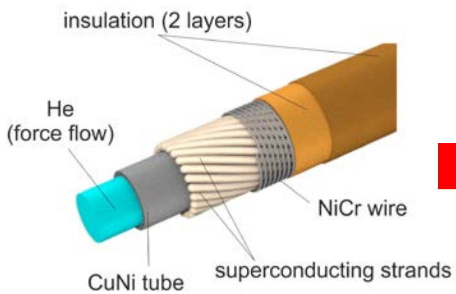
Parameters of superconducting dipole circuit of LHC and SIS100

Machine	LHC	SIS100
Number of magnets	154/circuit	108
Number of power converters	1/circuit	2
Nominal current (kA)	11.85	13.1
Nominal ramp rate (A/s)	10	28000
Total inductance of the circuit (mH)	$154 \times 2 \times 51 =$ $= 15.7 \times 10^3$	$108 \times 0.55 =$ $= 59.4$
Inductive voltage at cycling (V) per twin dipole / overall in the circuit	$1/ \approx 160$	$15.4/ \approx 1660$
Energy extraction system	$2 \times R_\mathrm{d}$ per circuit	$12 \times R_\mathrm{d}$
Cold by–pass	cold diode per twin dipole	none
Quench back heaters	on each coil	none

SIS100 is a fast cycling machine with extremely high ramp rate!

Protection system of SIS100 considers only extraction resistors

SIS100: low AC loss superconducting cable (Nuclotron type), NbTi/CuMn

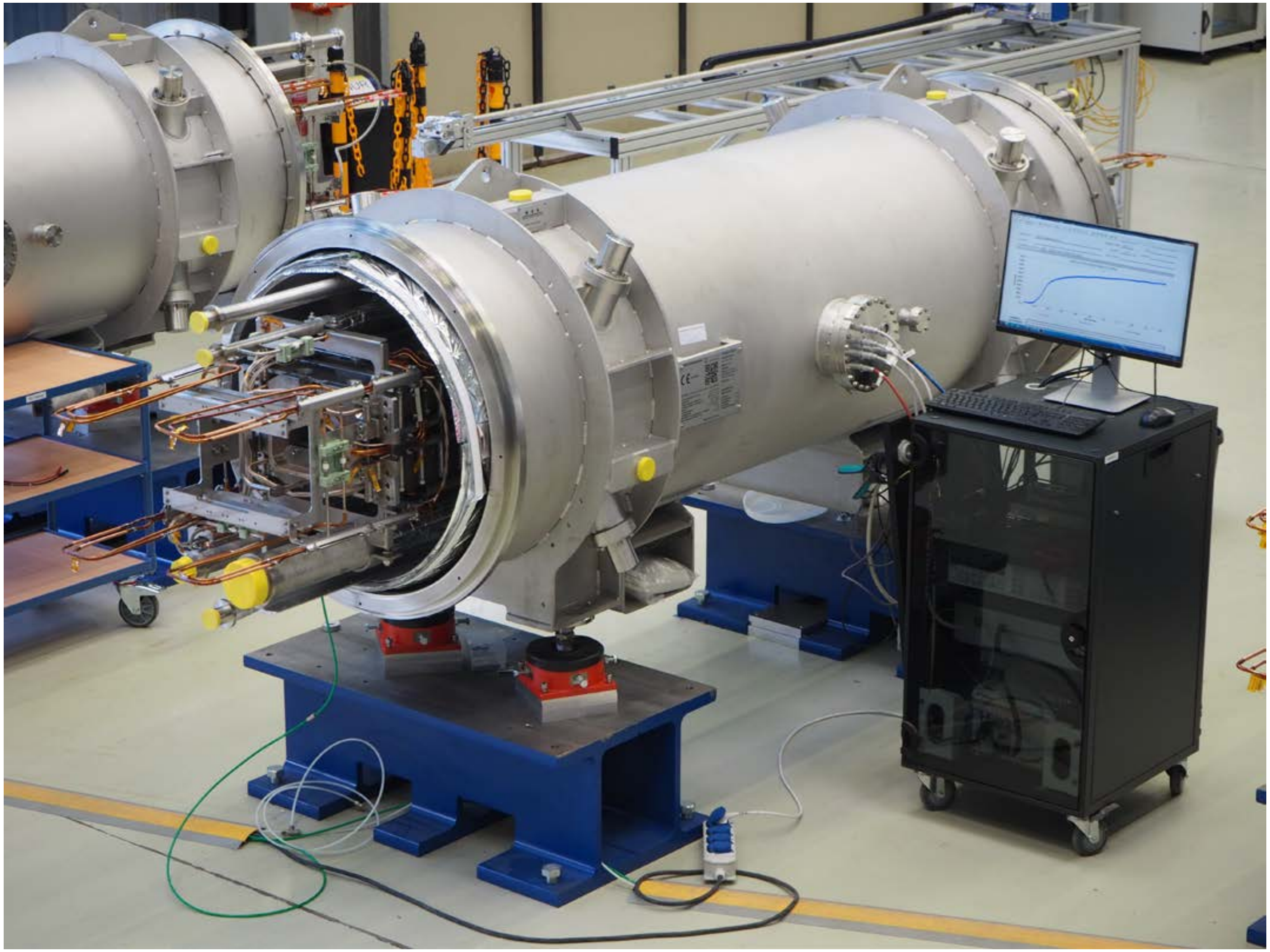


Quench back effect is not expected! If a single magnet quenches, other magnet will not quench due to high d*i*/d*t* at current dumping (very low probability).

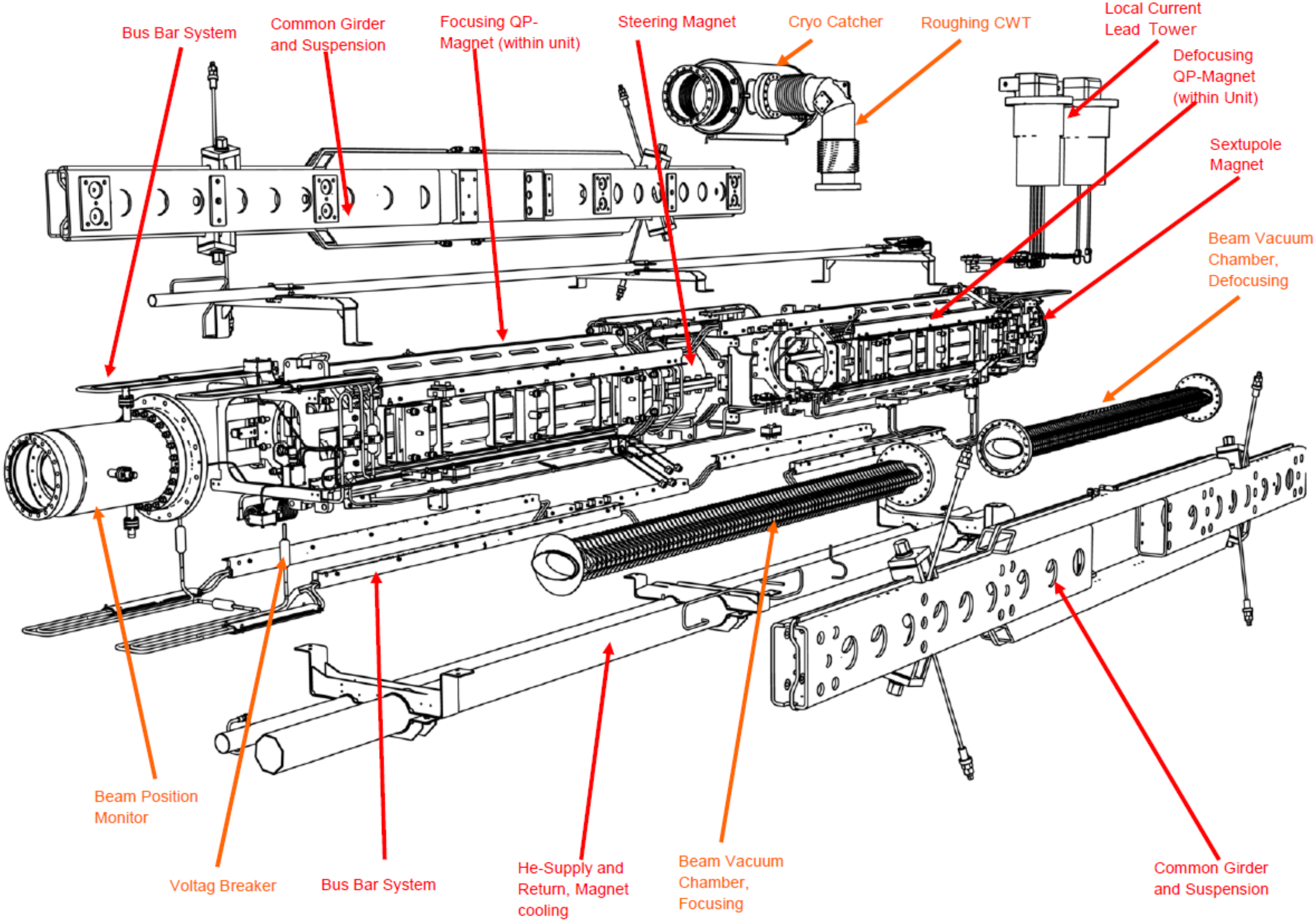
SIS100 Magnets Parameters

Magnet	Nominal current (A)	Inductance (mH)	Inductive voltage (V)	Quantity
Main dipole	13100	0.55	15.4	108
Main quad.	10512	0.41	7.5	83 (QD) 36 (F1) 47 (F2)
Chrom. sext.	250	43	62	42
Steering magnet	245 (SH) 241 (SV)	21	25	83 magnets 166 coils
Multipole corrector	250 (MQ) 250 (MS) 250 (MO)	1.1 (MQ) 5.6 (MS) 7.4 (MO)	1.8 (MQ) 5.8 (MS) 7.7 (MO)	12 magnets 36 coils
In/ex quad.	507	139	147	4

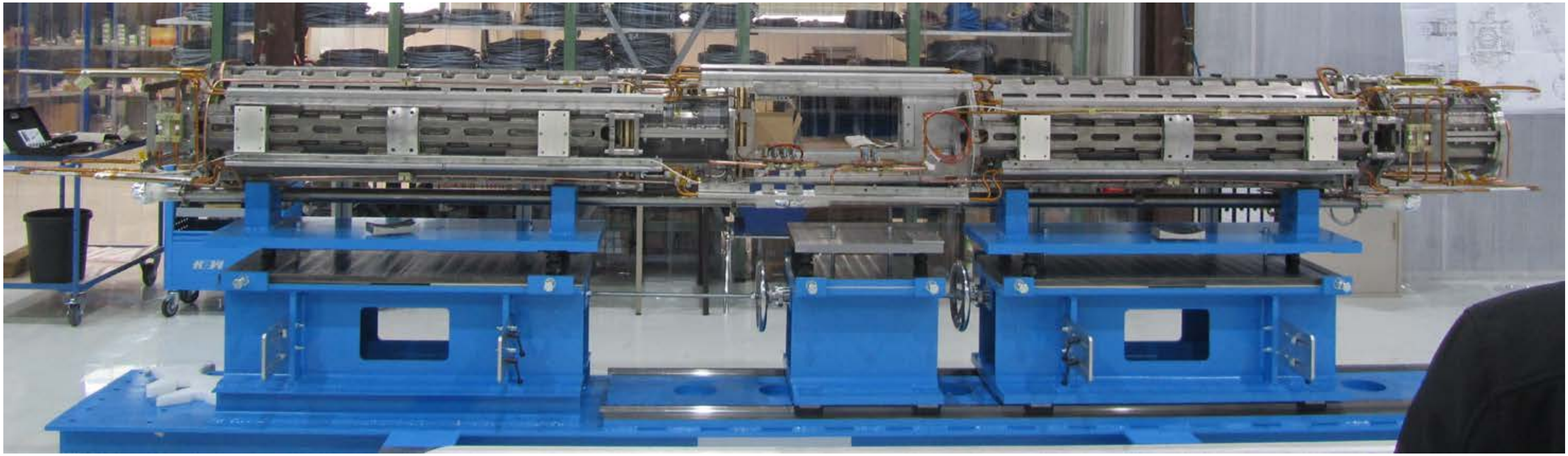
SIS100 Dipoles

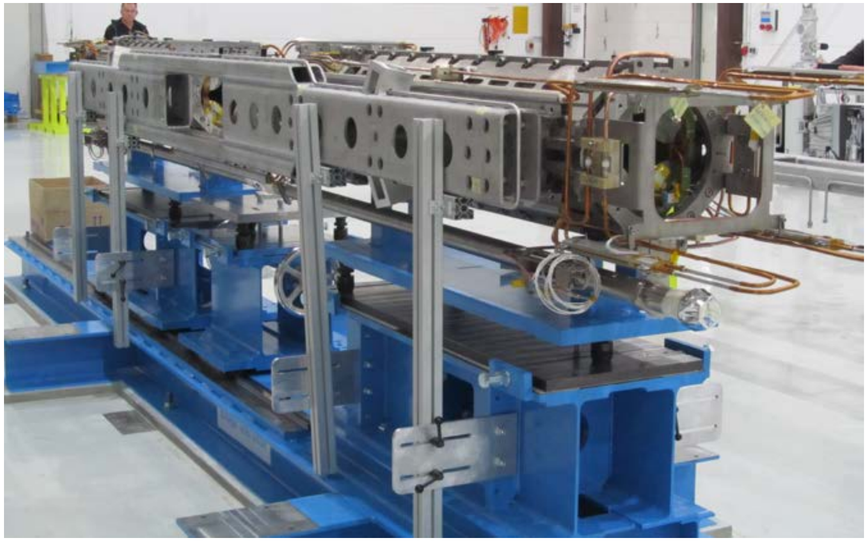


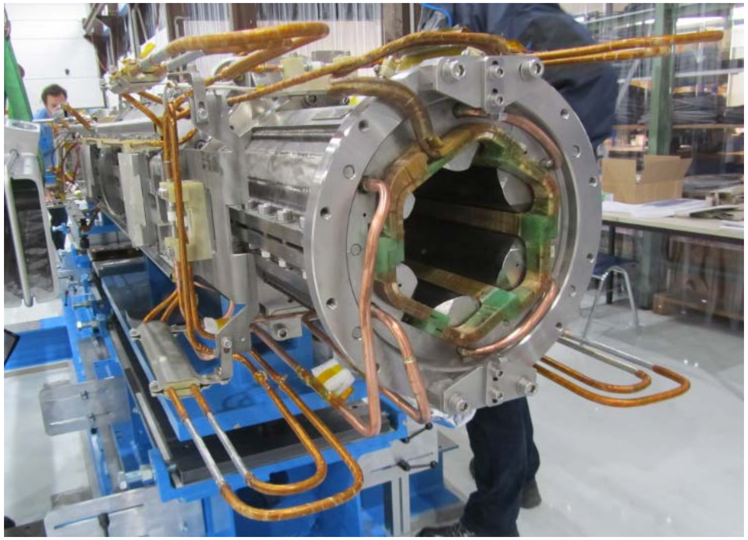
SIS100 Quadrupole Doublet Modules



SIS100 Quadrupole Units

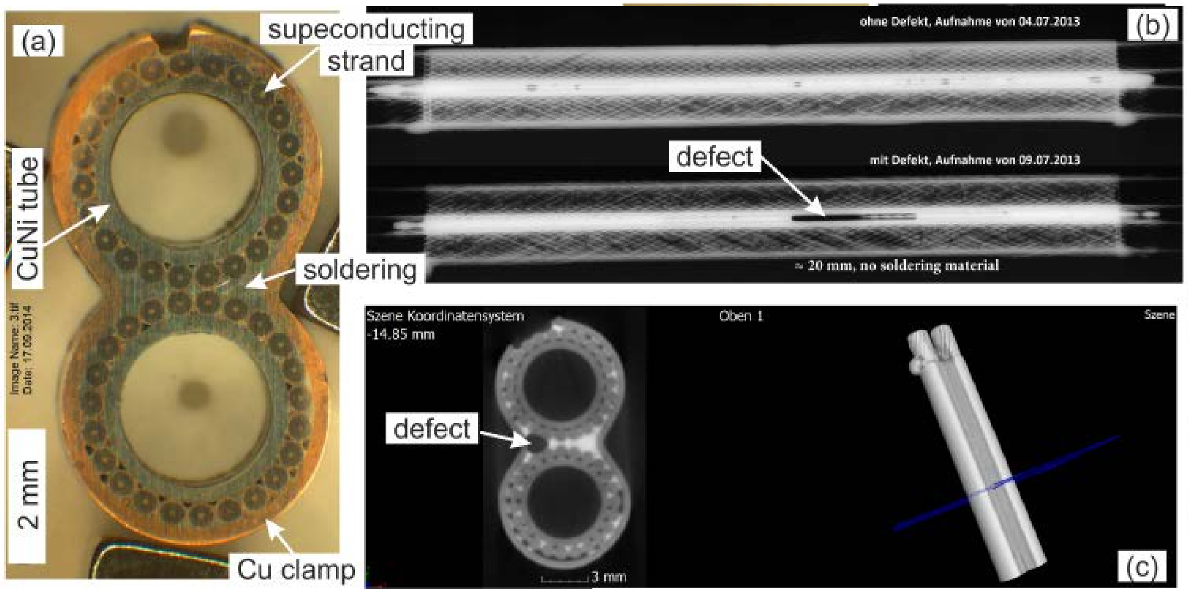


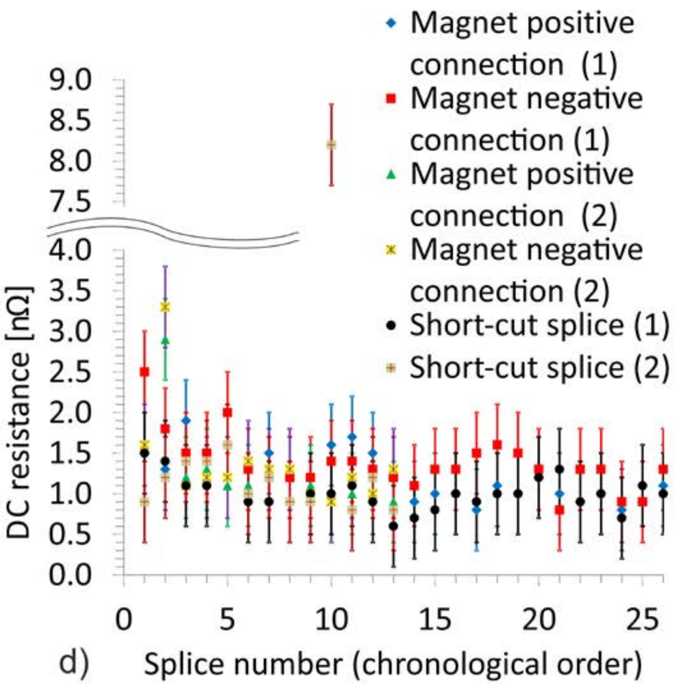




SIS100 Quadrupole Units

SIS100 Splices



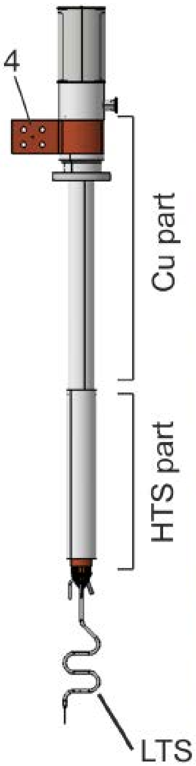


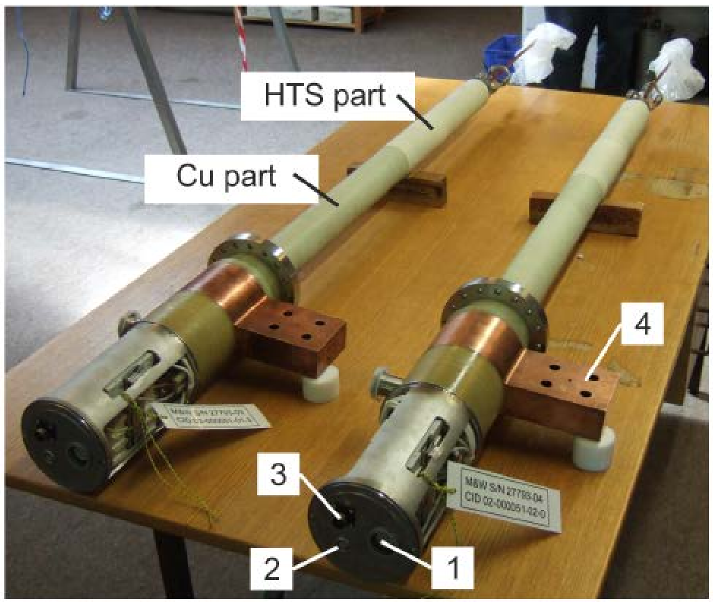
- excellent reproducibility since 2013
- easy and fast connection method
- relatively low ac losses
- no correlation between *R* (300 K) and *R* (4 K)

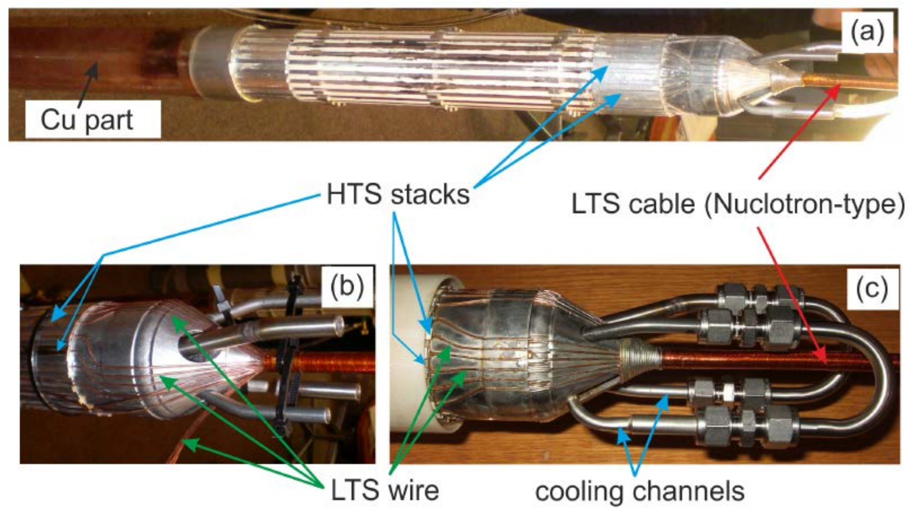
Main Current Leads

14 kA DC HTS current leads

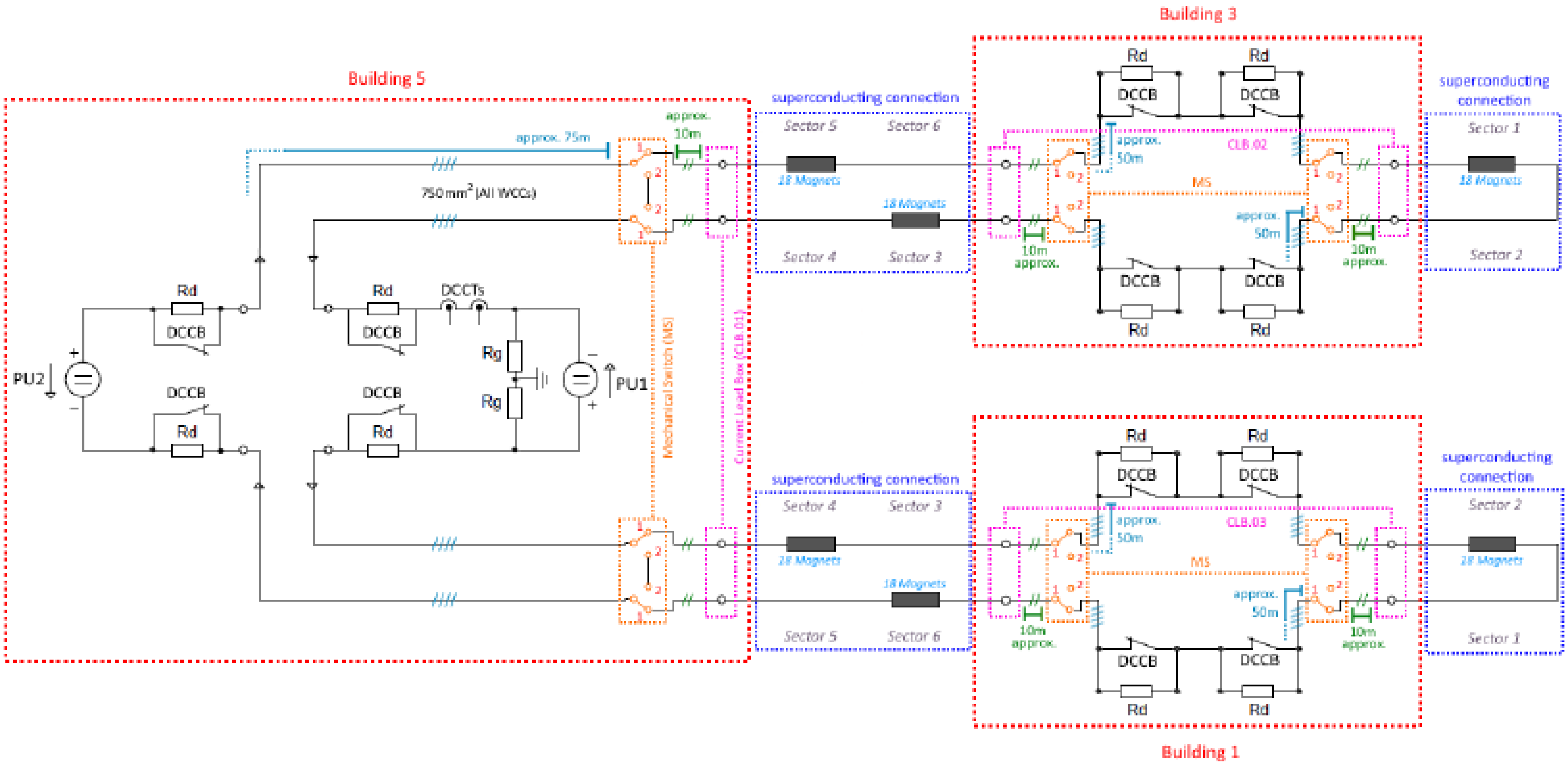
- Cu part – vapour cooled
- HTS part – conduction cooled





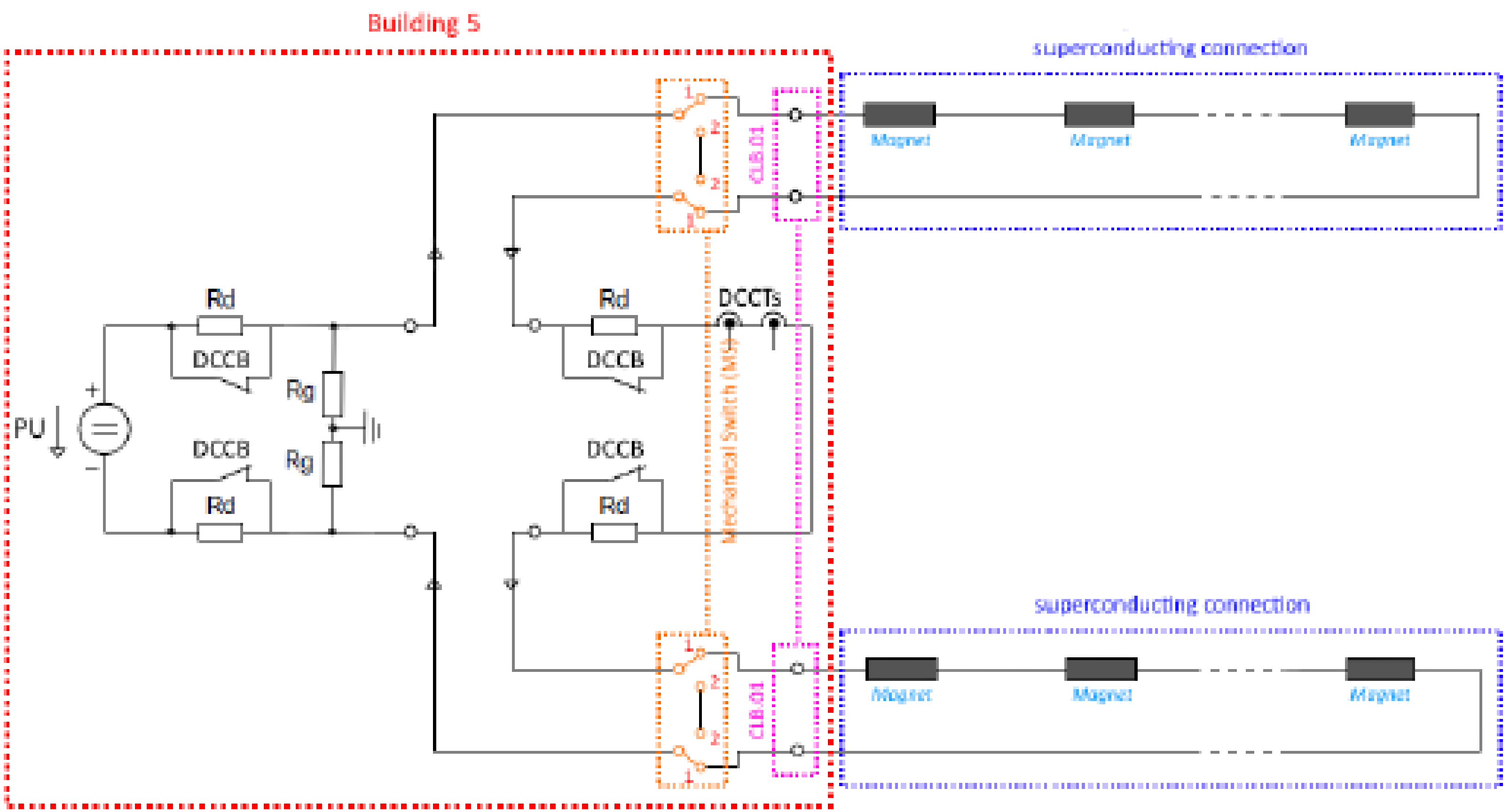


SIS100 Dipole Circuit



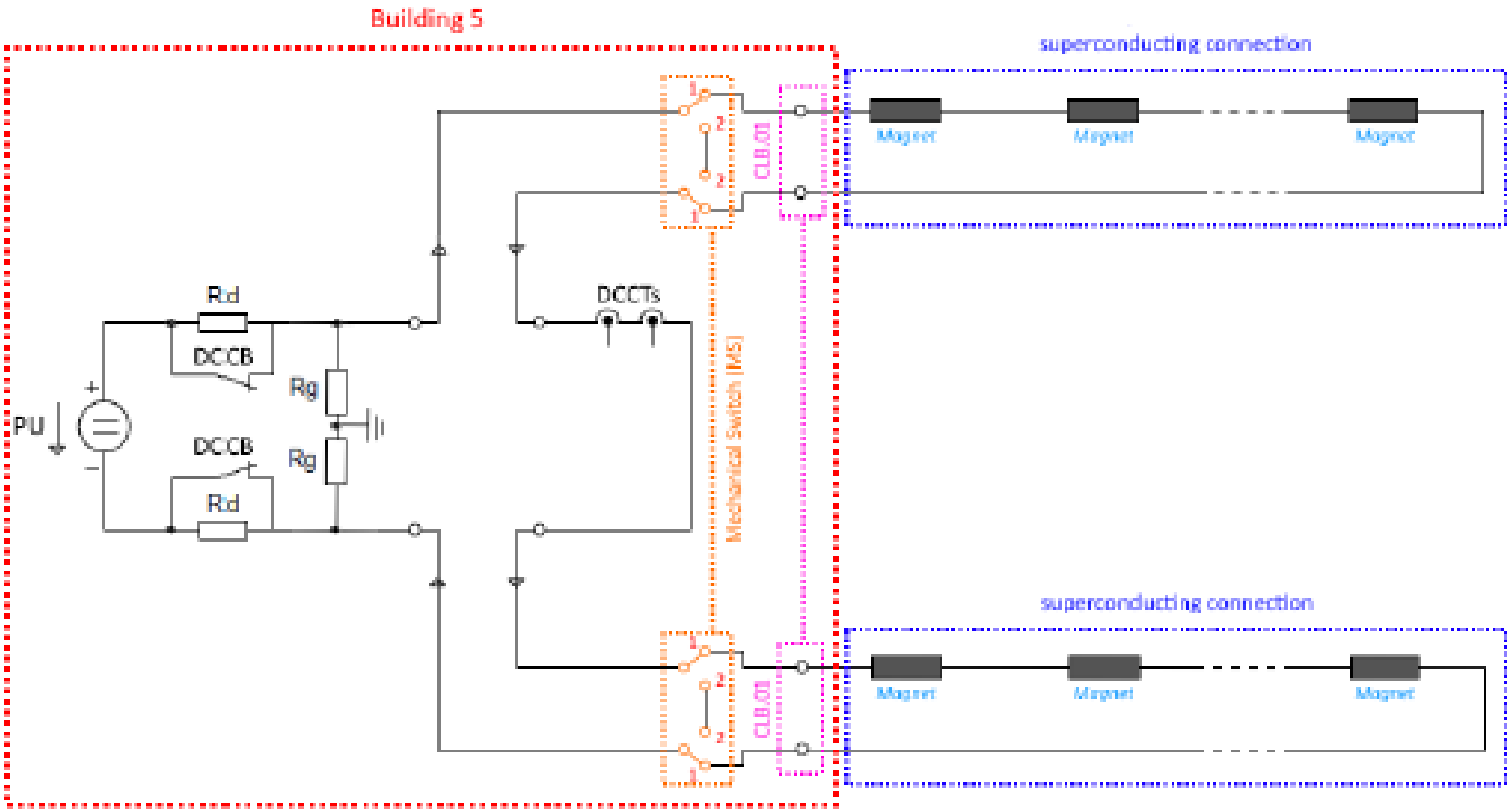
courtesy V. Plyusnin

SIS100 Main Quadrupole QD



courtesy V. Plyusnin

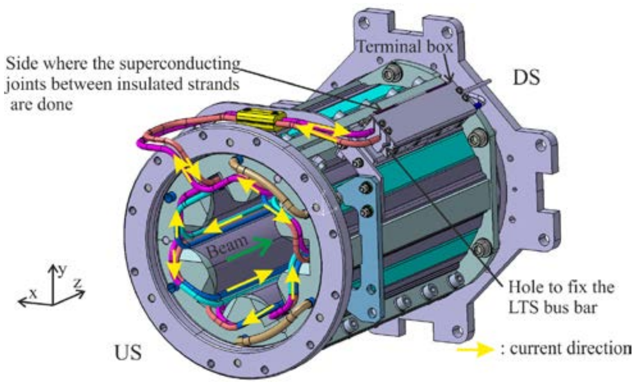
SIS100 Main Quadrupole F1/F2



courtesy V. Plyusnin

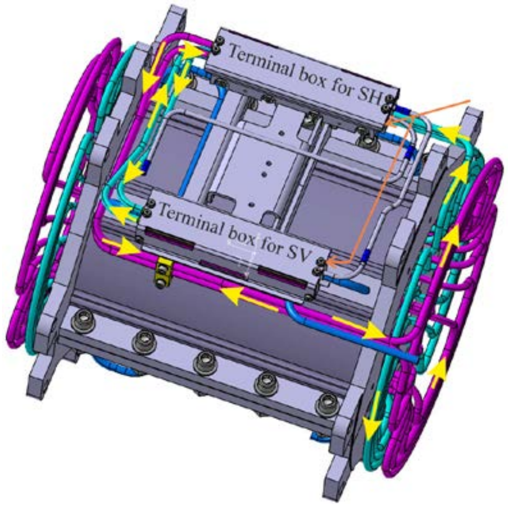
SIS100 Corrector Magnets

Chromaticity sextupole



single coil

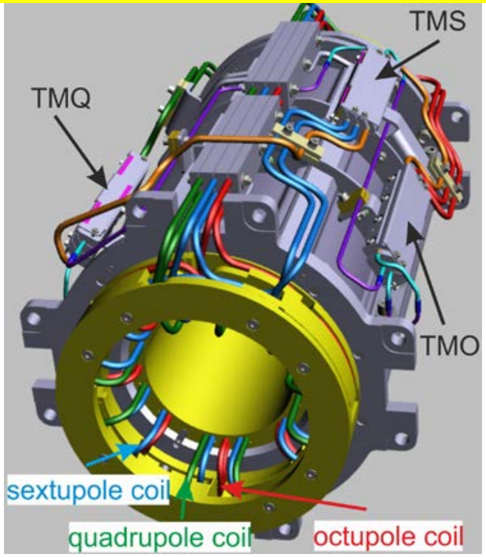
Steering magnet



2 coils:

- horizontal
- vertical

Multipole corrector

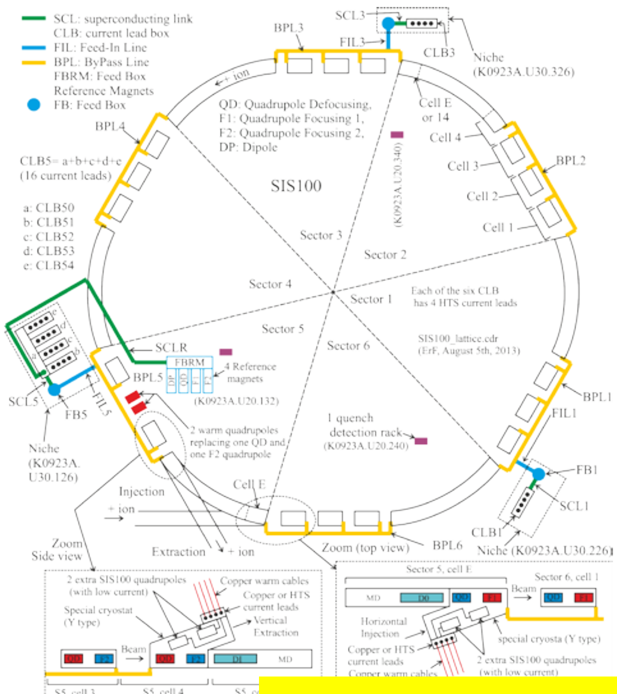


3 coils:

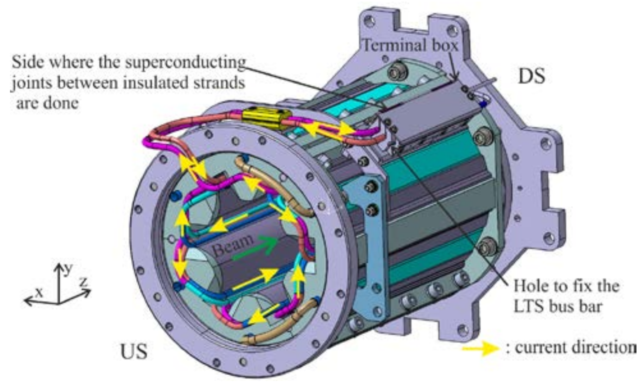
- quad.
- sext.
- oct.

SIS100 Chromaticity Sextupole (7 circuits)

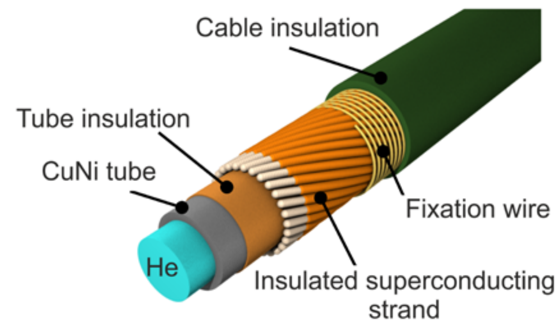
SIS100 ring



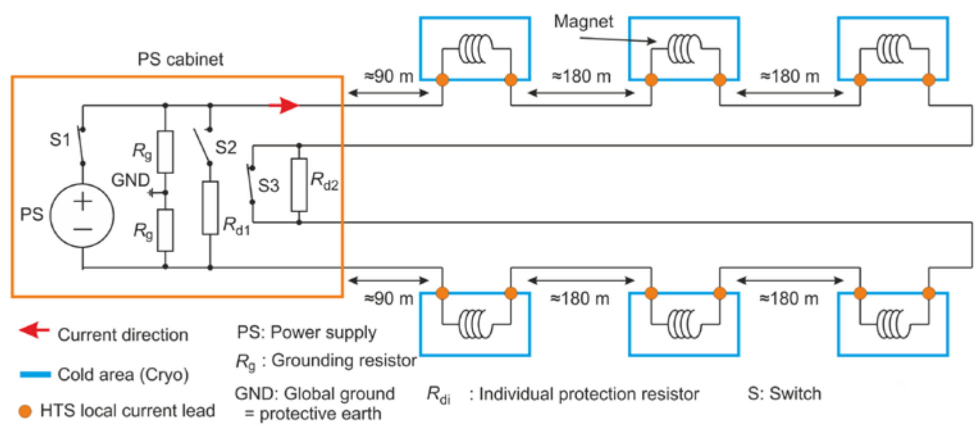
Chromaticity sextupole (42)



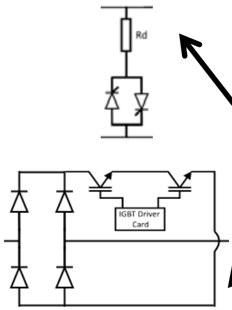
Corrector cable (Nuclotron-type)



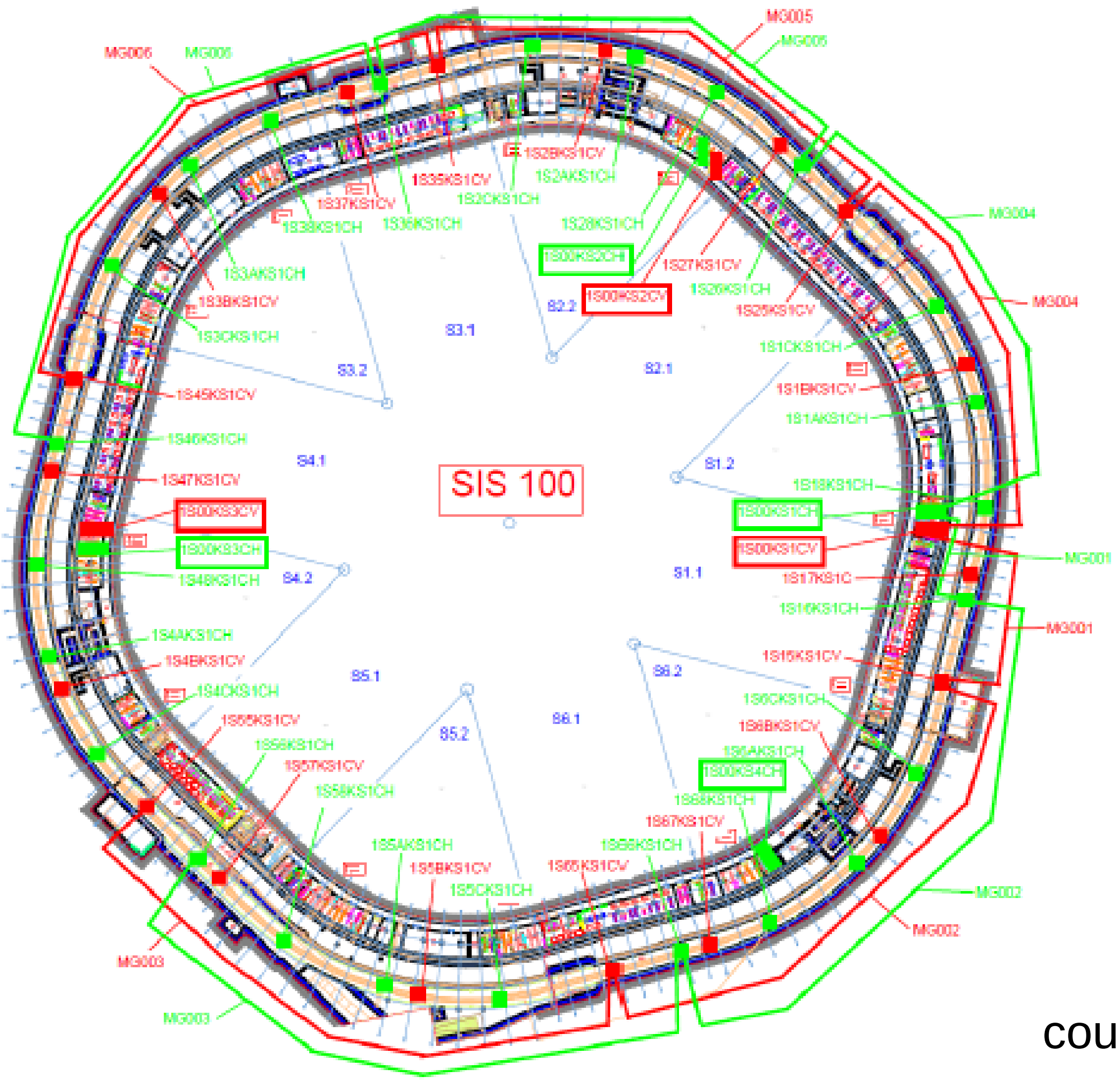
Magnet parameters:
I_n = 252 A, L=43 mH, $L\,di/dt$ = 62 V



Circuit parameters:
R_d= 2 x 3.846 (±10%) Ω
Fast semiconductor switches are required!
S2 – thyristor switch (bipolar)
S1, S3 - DC voltage breakers (bipolar), GND in the middle.

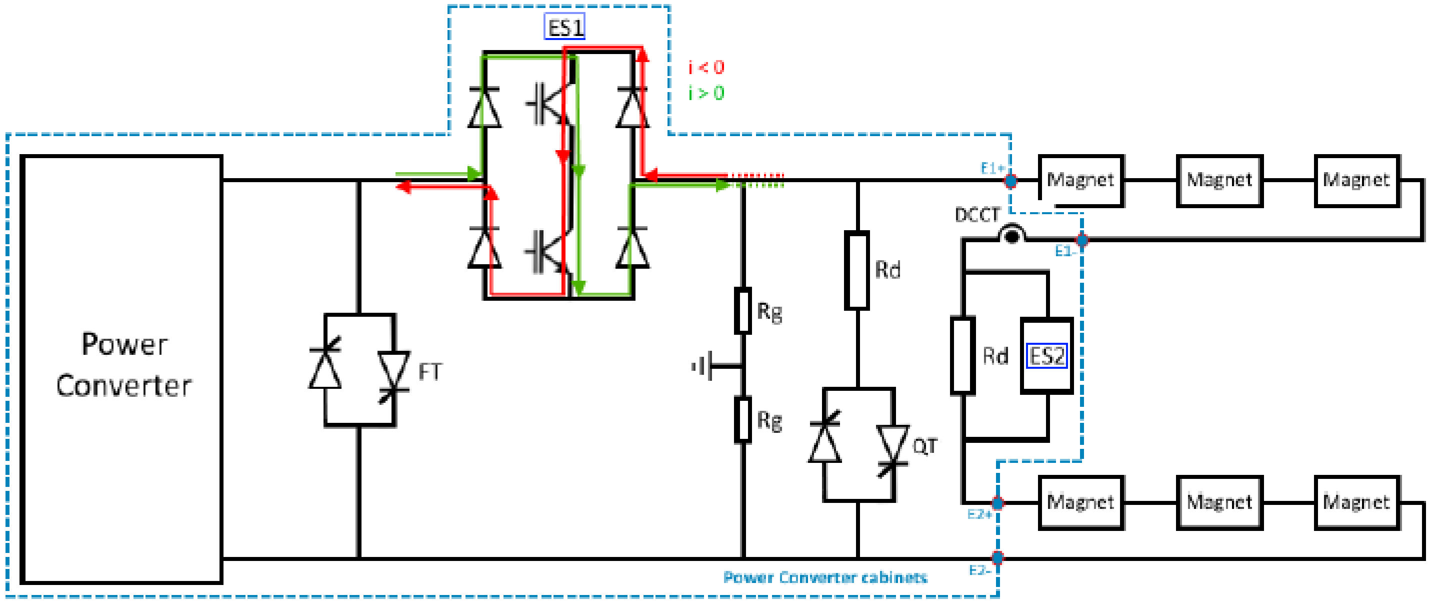


SIS100 Chromaticity Sextupoles Circuits



courtesy V. Plyusnin

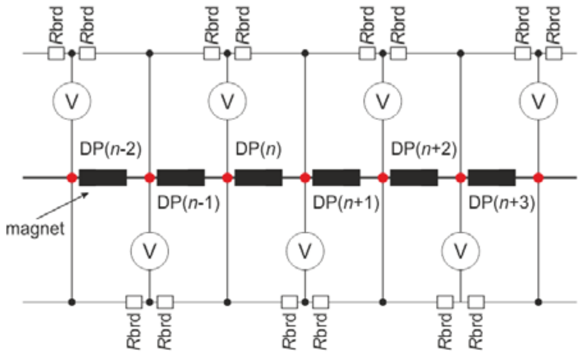
SIS100 Chromaticity Sextupole Circuit

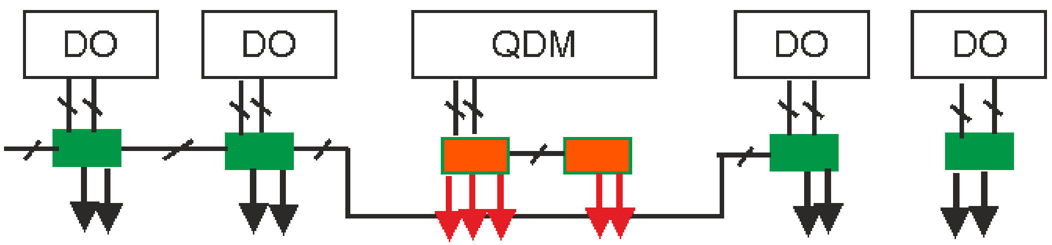


courtesy V. Plyusnin

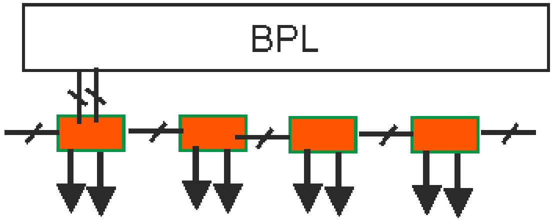
SIS100 Quench Detection Structure

Main circuits

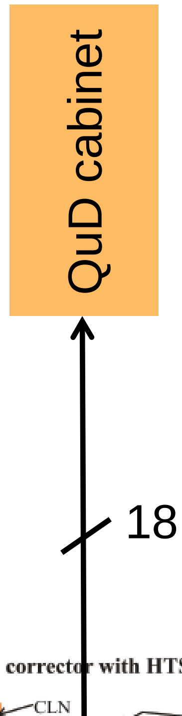




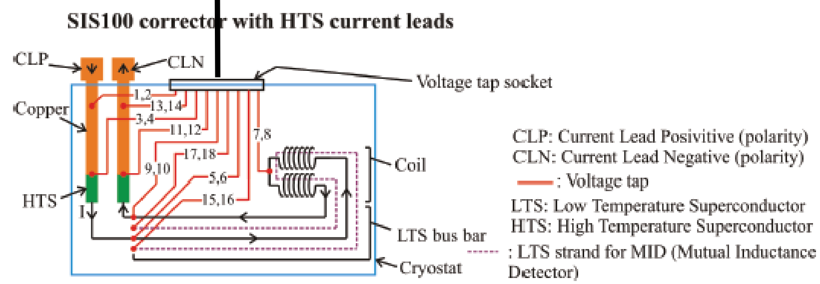
complicated HV cabling



Correctors

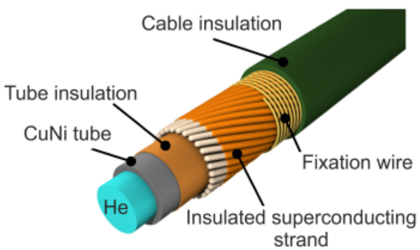


Direct connection to the QuD cabinet



SIS100 Corrector Magnets

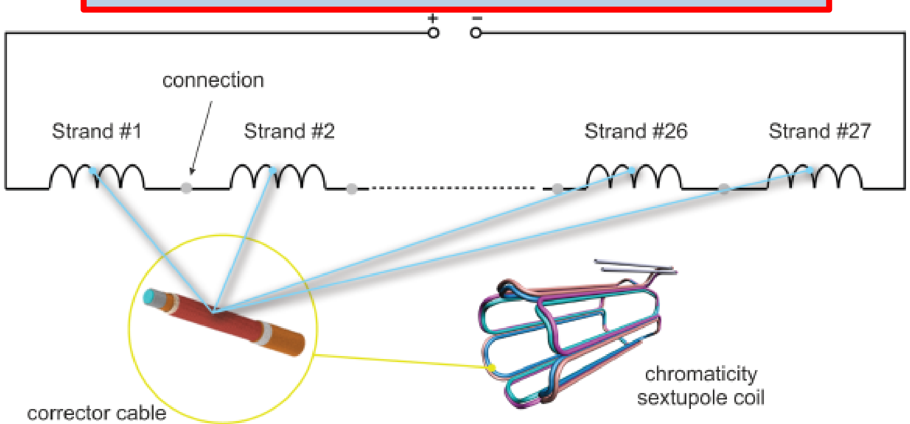
Insulated strand Nuclotron-type cable



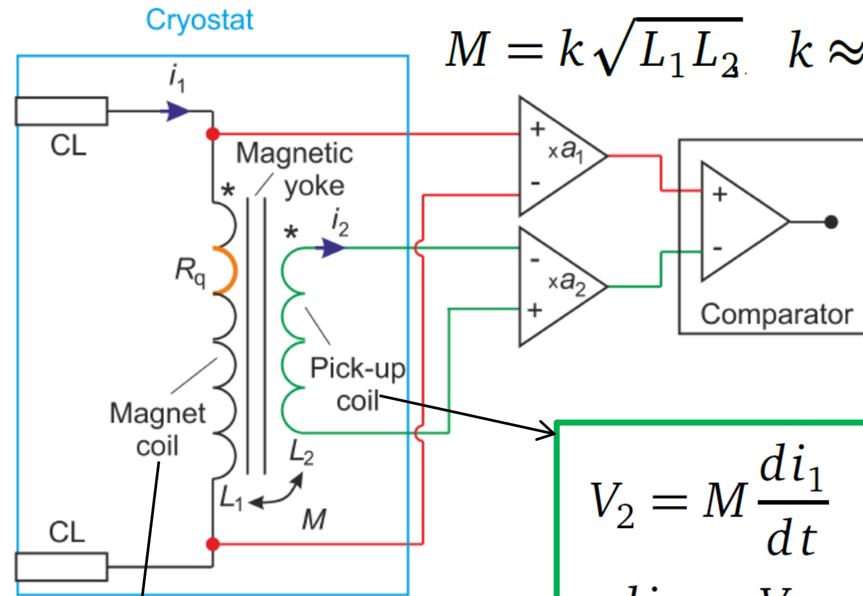
High risk of symmetrical quench, e.g. beam induced. Balance BRD is completely insensitive to such an event.

A typical solution for the problem considers either an asymmetrical middle V-tap of BRD or/and secondary BRD in multi-coil circuits.

Series connection of strands



Quench Detection with a Coupled Pick-up Coil



$$M = k\sqrt{L_1 L_2} \quad k \approx 1$$

$$V_2 = M\frac{di_1}{dt}$$

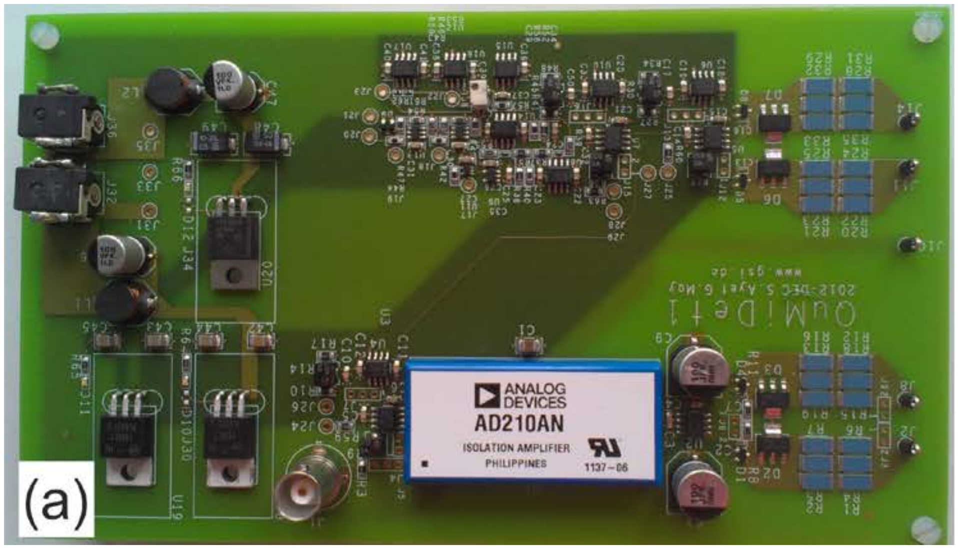
$$\frac{di_1}{dt} = \frac{V_2}{M}$$

$$V_1 = L_1\frac{di_1}{dt} + V_q$$

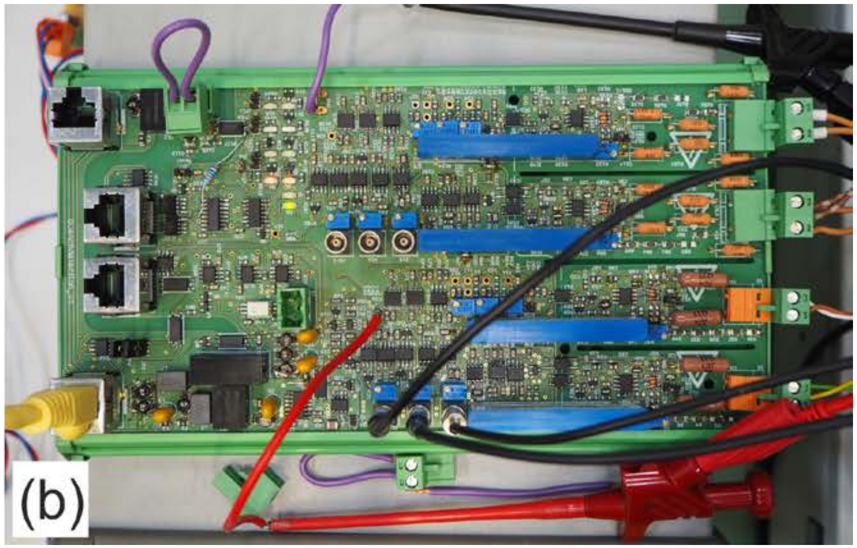
$$V_q = V_1 - L_1\frac{di_1}{dt}$$

$$V_q = V_1 - \frac{L_1}{M}V_2$$

MID Prototypes

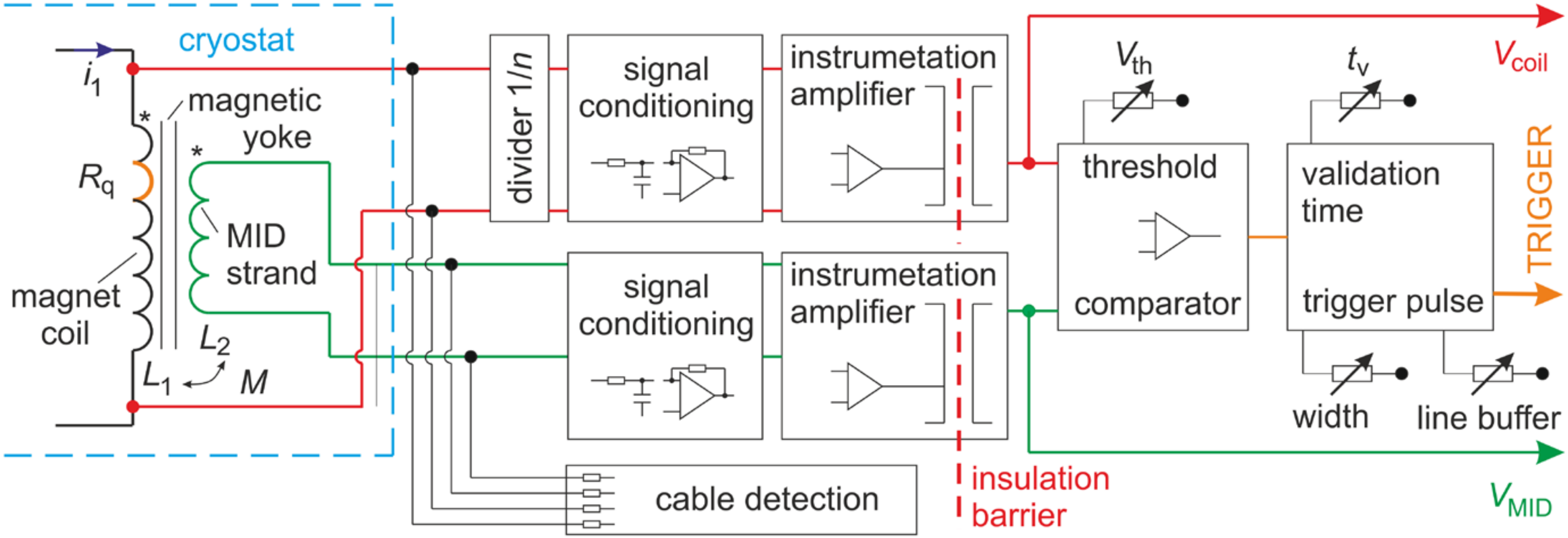


(2013)



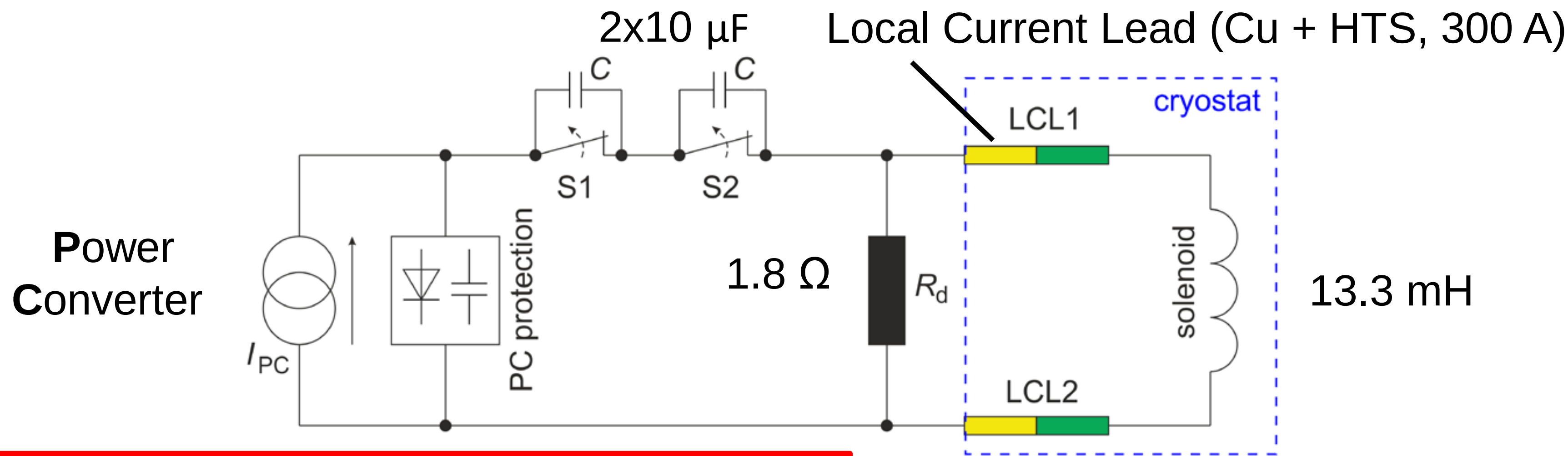
(2018)

MID Prototype



Main features:

- analogue robust design, fully differential channels
- easy hardware adaptation for various strand numbers (SIS100: 27, 24, 20, 13)
- 2 kV HV insulation
- locally adjustable threshold and parameters of the validation circuit
- V_{coil}, V_{MID} and TRIGGER available for post mortem and data logging (bandwidth < 1 kHz → 300 Hz)
- cable detection with pull-up resistors



Quench Detection and Magnet Protection:

S1, S2 – redundant mechanical circuit breakers

C – snubber capacitor in order to cut-out the voltage peak on the switch

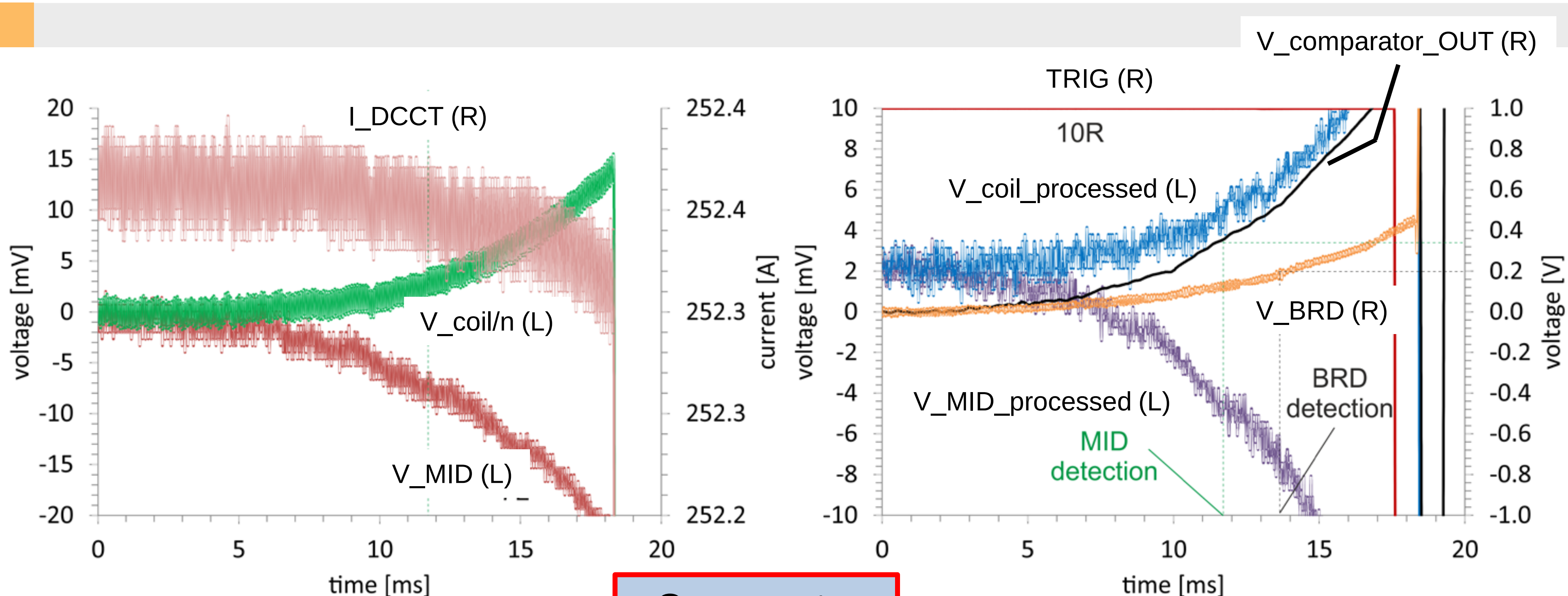
R_d – energy extraction resistor (always-ON)

Solenoid and LCL are monitored by the quench detection system of the test facility:

- small bridge – coil extremities and the middle V-tap, V_{th} = 200 mV
- large bridge – solenoid + 2 x HTS with the us of the middle V-tap, V_{th} = 220 mV
- 2x (Cu+HTS) – 2 single-ended channels, V_{th} = 80 mV

MID does not serve as a safety system!

- t_v = ~5 ms

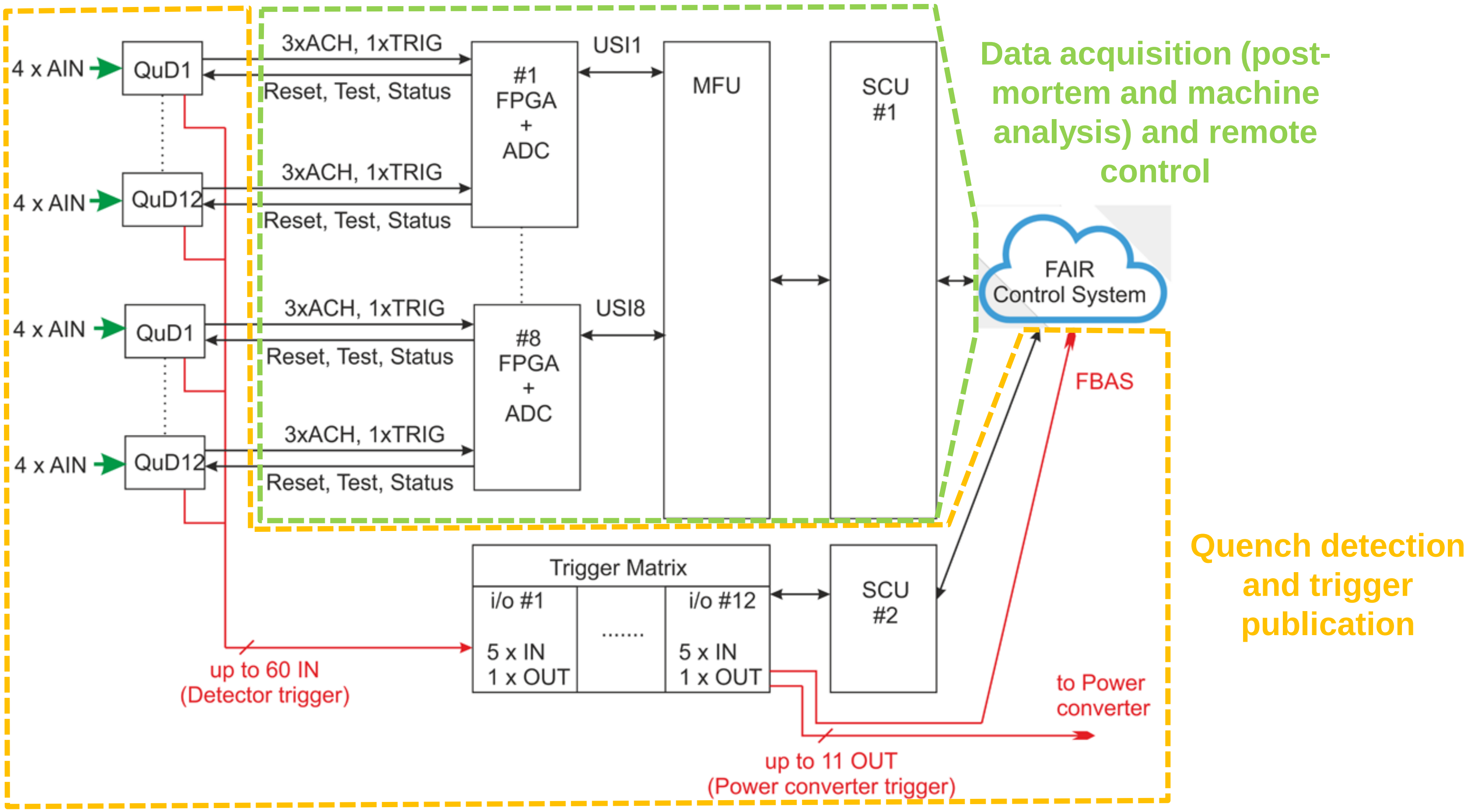


Comments:

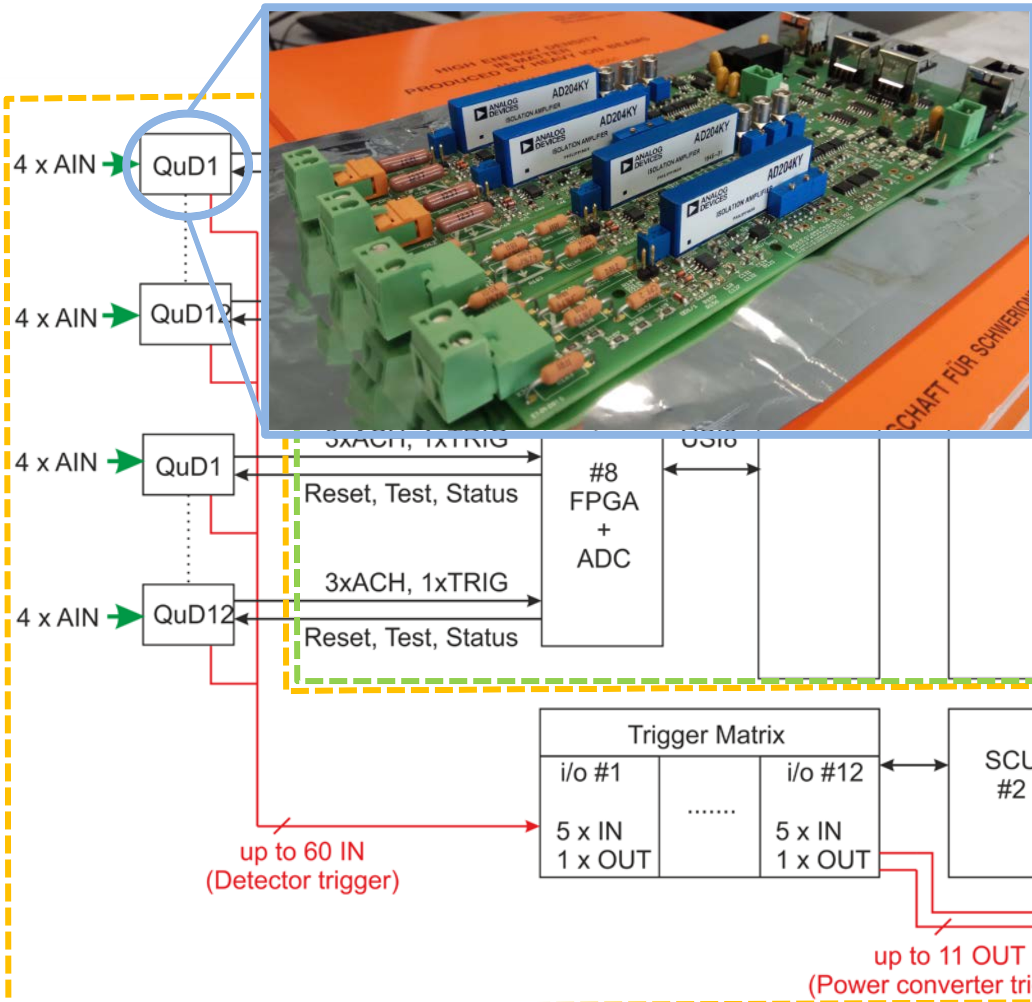
- visible current drop → PC's current regulator not as fast as initially anticipated
- drop in the current is immediately transferred to the MID strand → which actually speeds up the quench detection; CAUTION: polarity in MID is of extreme importance!
- filtering and signal conditioning blocks function as expected
- in the example, V_{thMID} was set to 340 mV, tv ≈ 5 ms, lower threshold is possible
- the signal at the comparator output is clean and clearly indicates quench

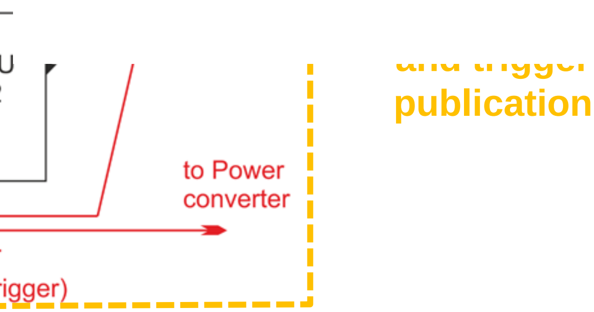
FAIR Quench Detection System

SIS100 – In-house development



SIS100 – In-house development





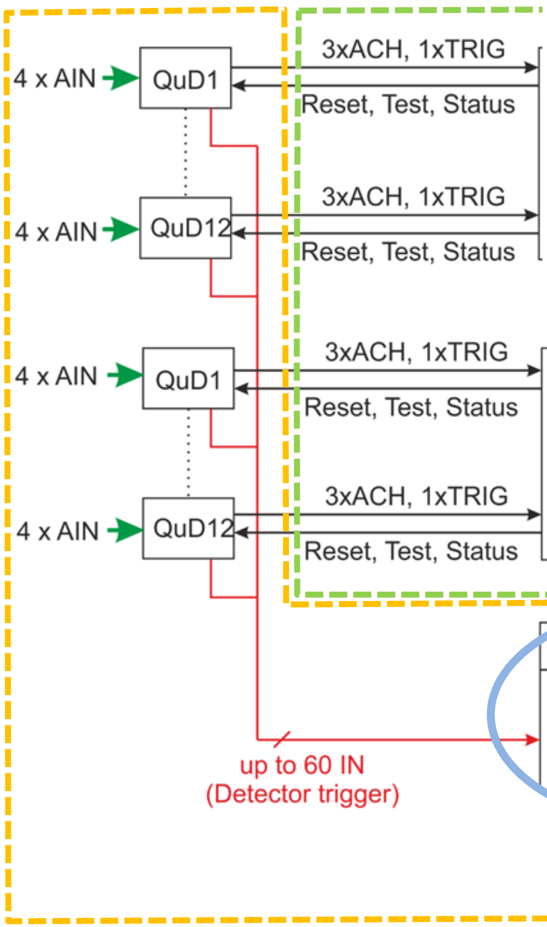
Quench Detector (QuD)

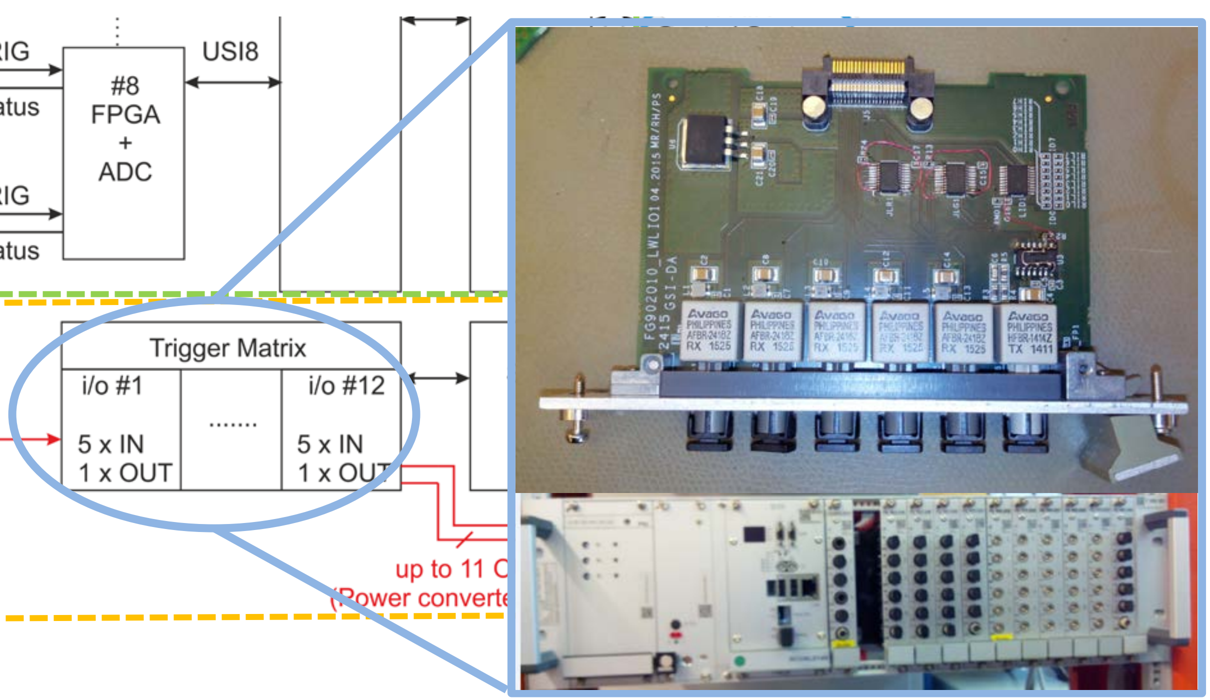
- Analog board with 4 differential inputs, 4 analog outputs and 2 optical trigger outputs.
- Three types of board (Main magnet board, corrector + LCL board, MCL board).
- (+) Prototype existing – parallel development with Super-FRS.
- (−) No remote configuration of the quench detection parameters (threshold, integration time, etc.).
- (−) Insulation amplifiers could be obsolete in the near future.

SIS100 – In-house development

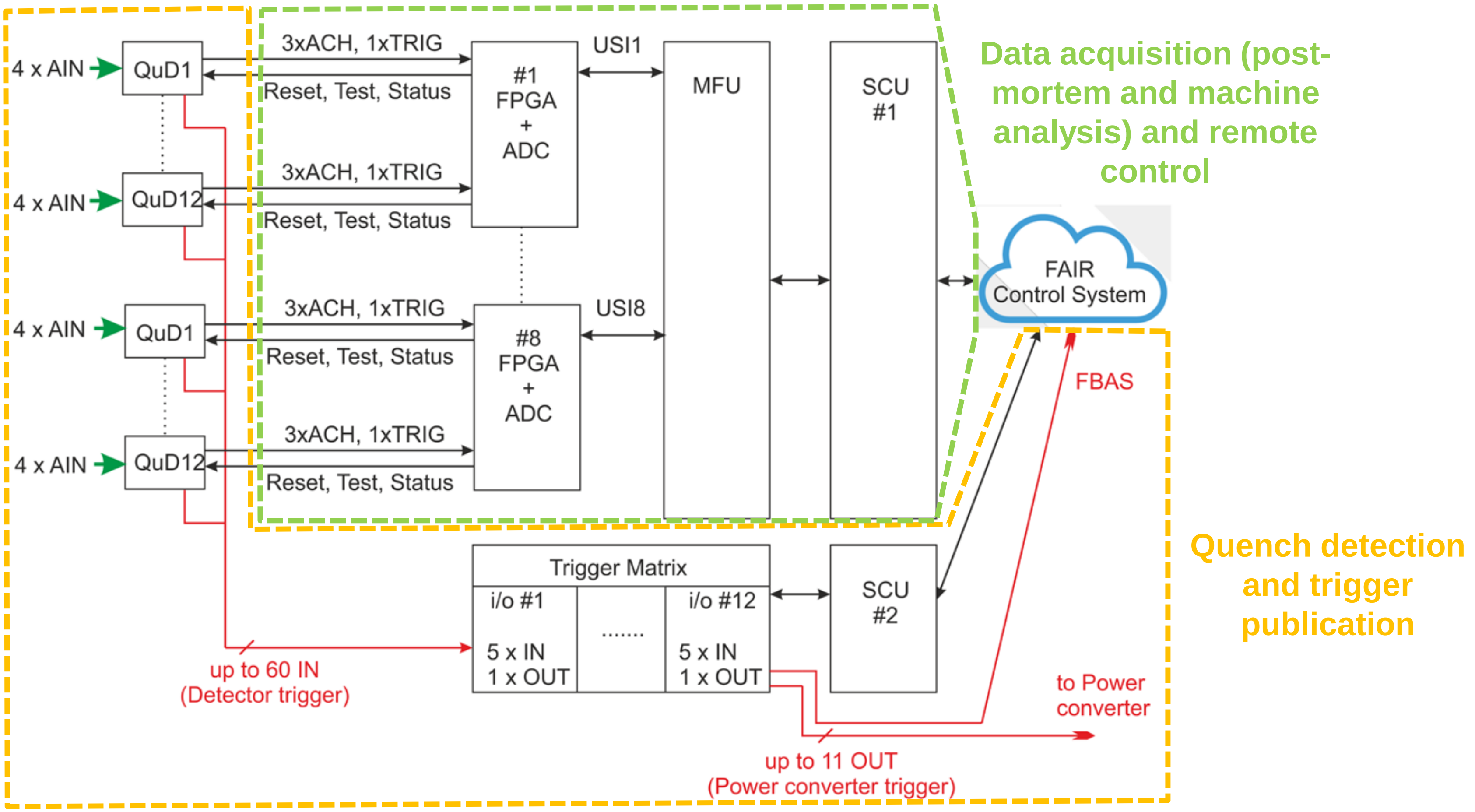
Trigger Matrix (Trigger concentrator)

- Up to 12 i/o-cards in one crate; each card has 6 i/o´s.
- FPGA design.
- ➕ Existing component developed by CSCO.
- ⛔ Not designed for safety critical system.
- ⛔ Hardware and Software adaptation needed.

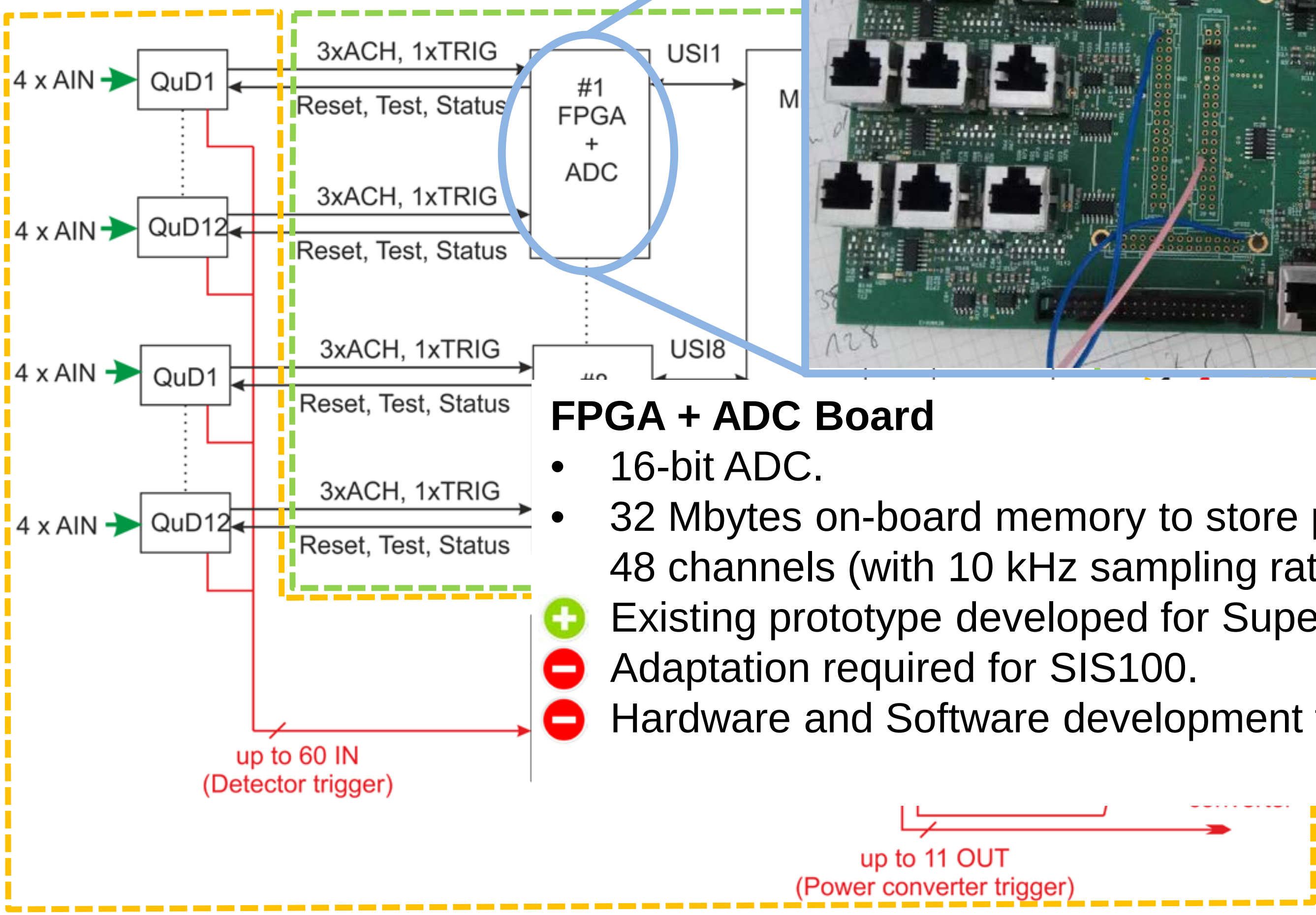


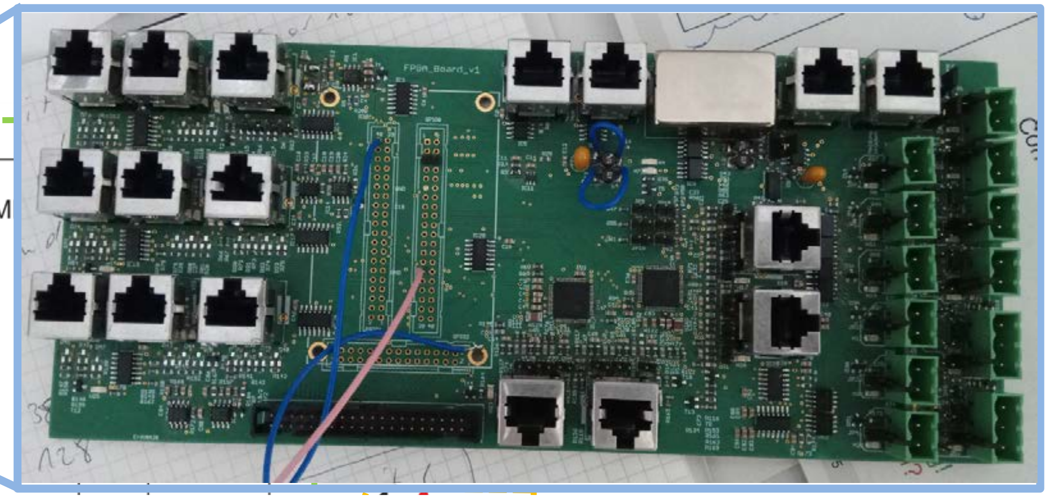


SIS100 – In-house development



SIS100 – In-house development





FPGA + ADC Board

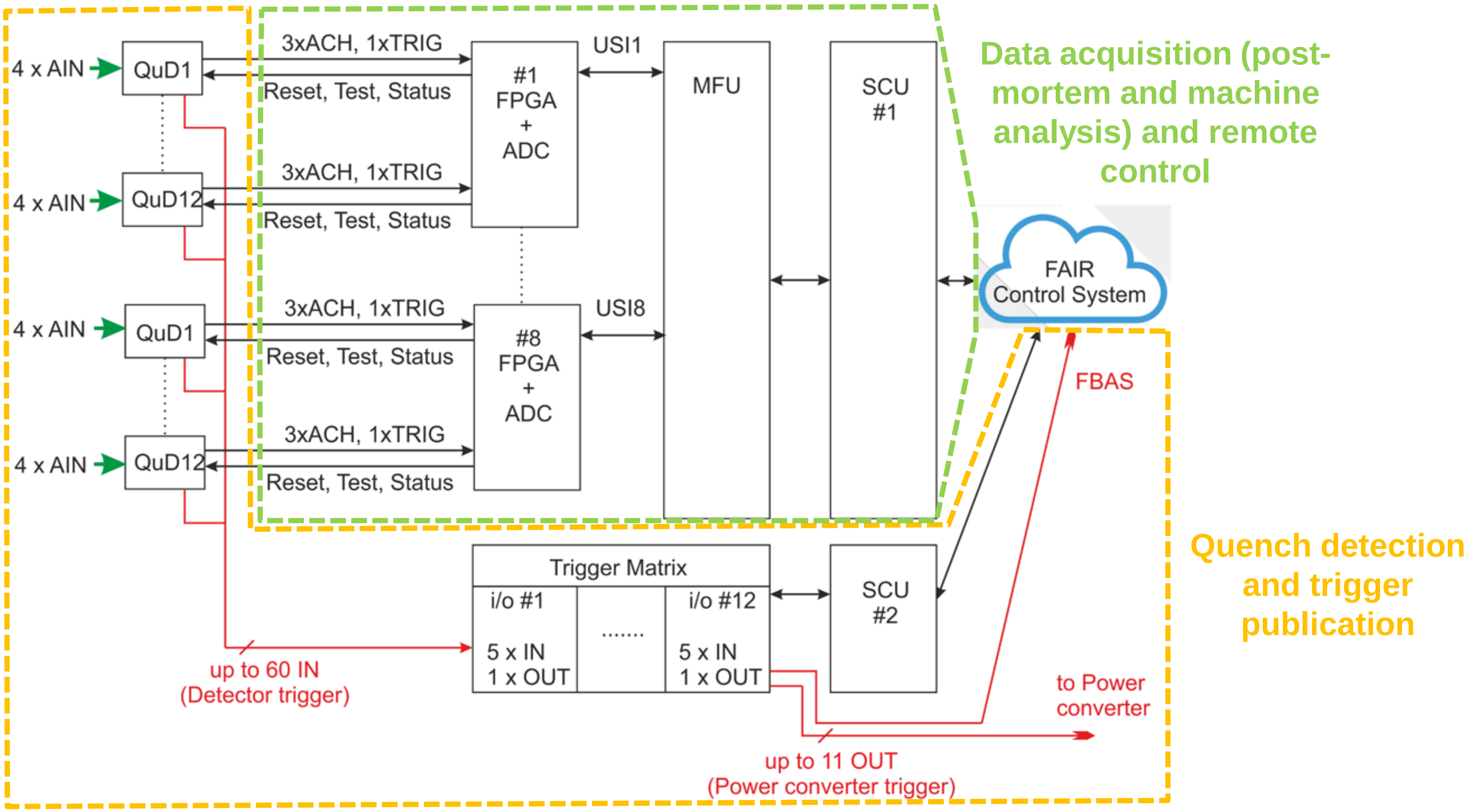
- 16-bit ADC.
- 32 Mbytes on-board memory to store post-mortem data of the 48 channels (with 10 kHz sampling rate for +/-16 s).

(+) Existing prototype developed for Super-FRS.

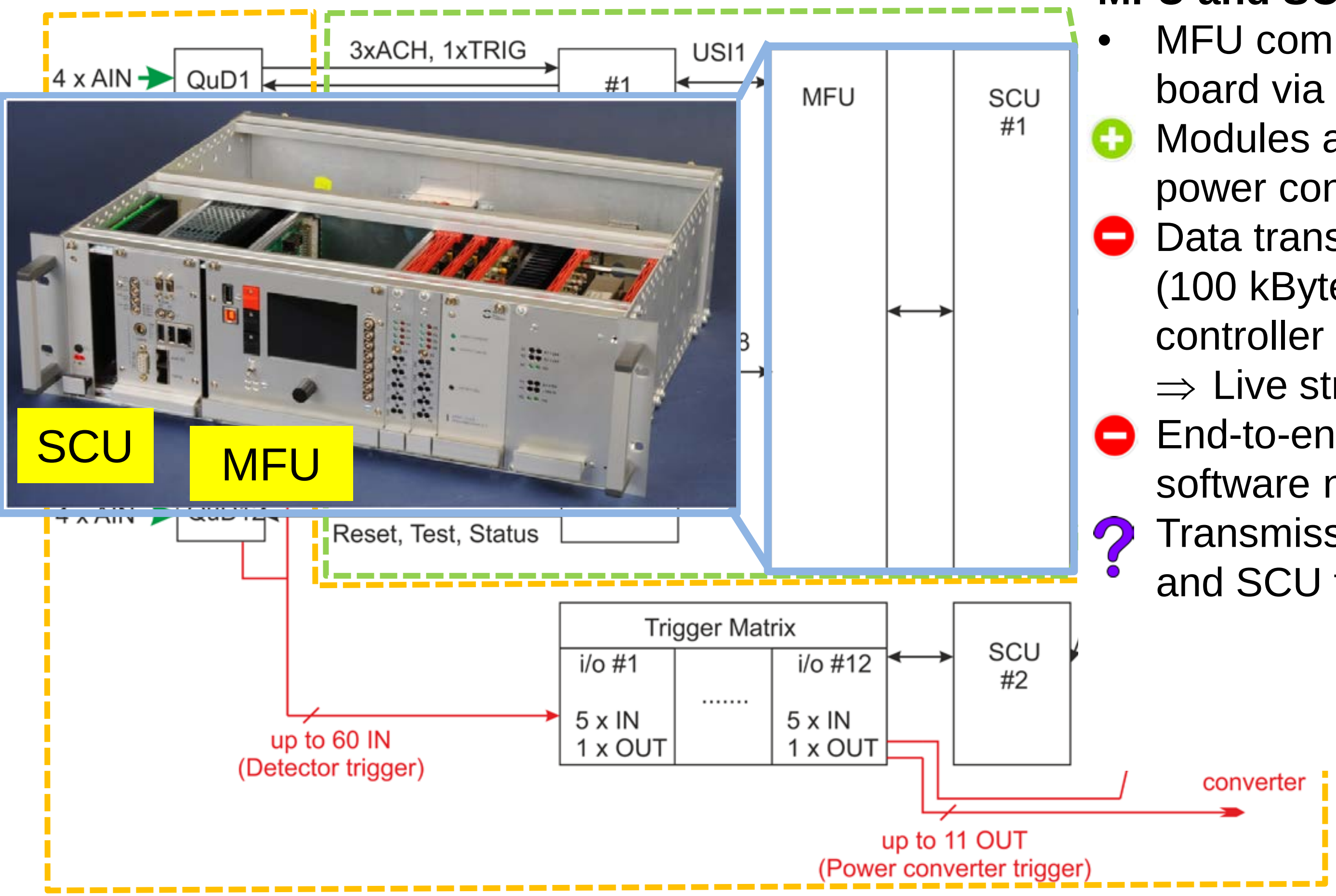
(–) Adaptation required for SIS100.

(–) Hardware and Software development to be done.

SIS100 – In-house development



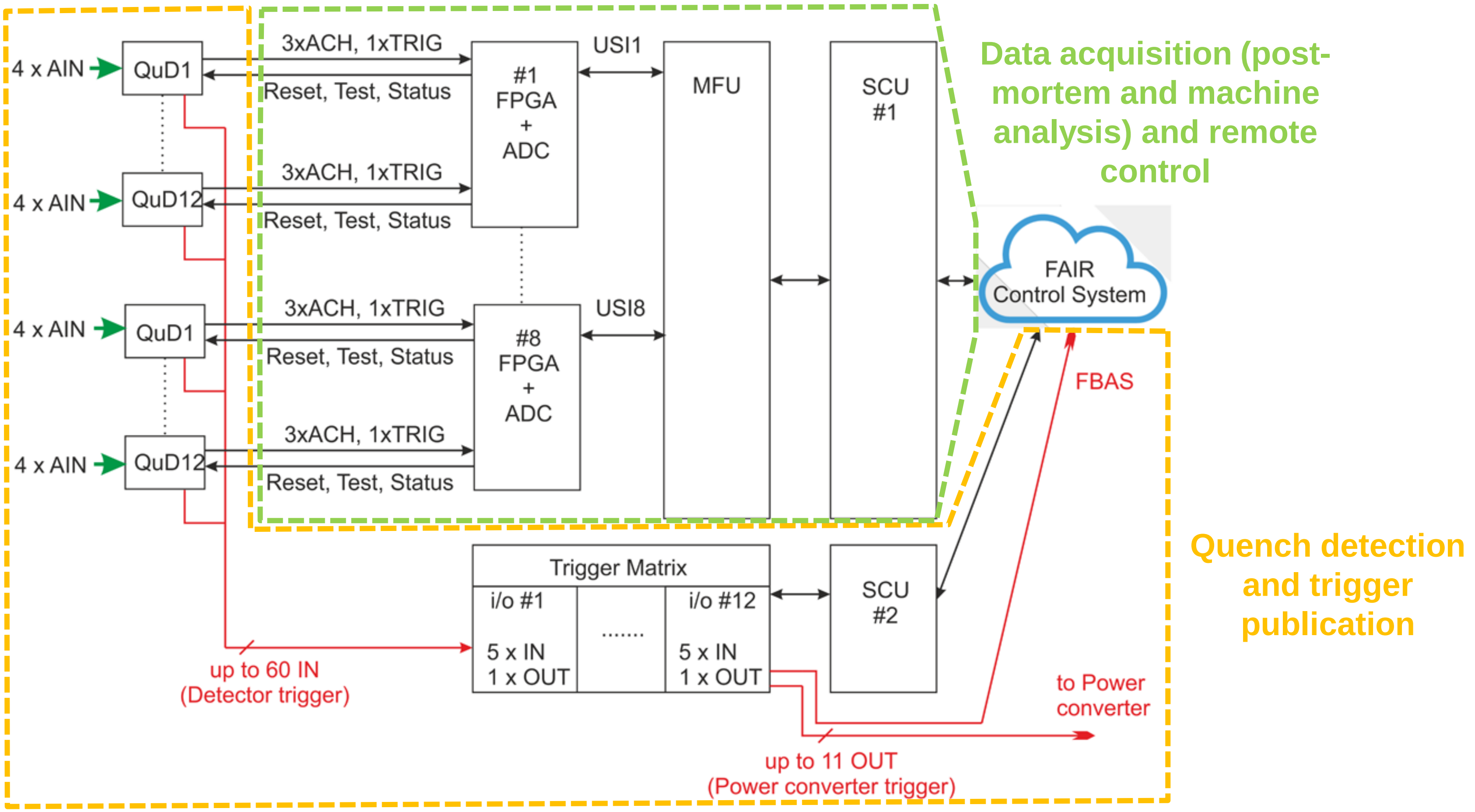
SIS100 – In-house development



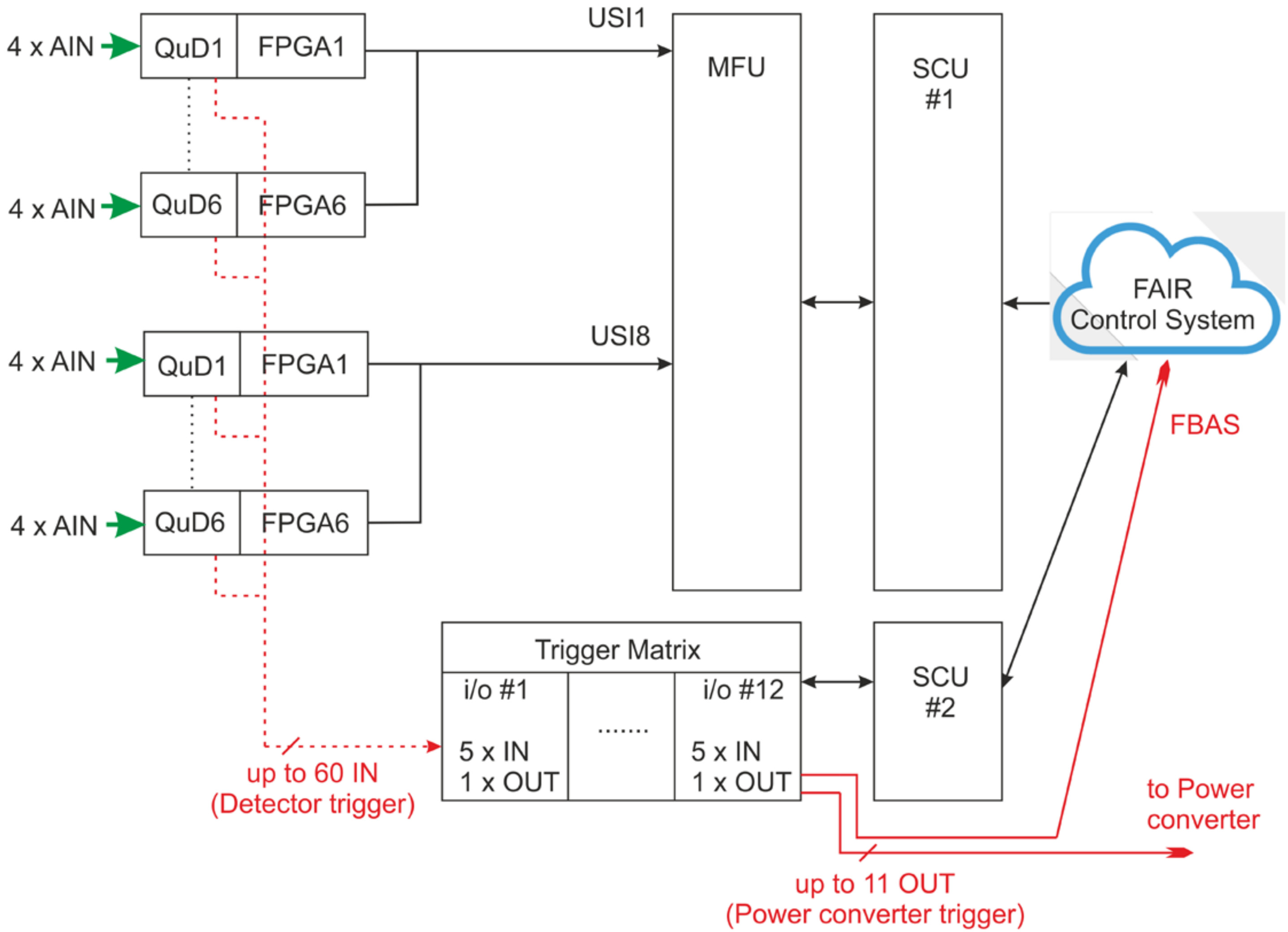
MFU and SCU

- MFU communication to FPGA board via USI.
- (+) Modules already in use in each power converters.
- (−) Data transmission rate limited (100 kBytes/s) by the MFU controller speed.
  ⇒ Live streaming not possible.
- (−) End-to-end communication software need to be developed.
- (?) Transmission rate between MFU and SCU to be clarified.

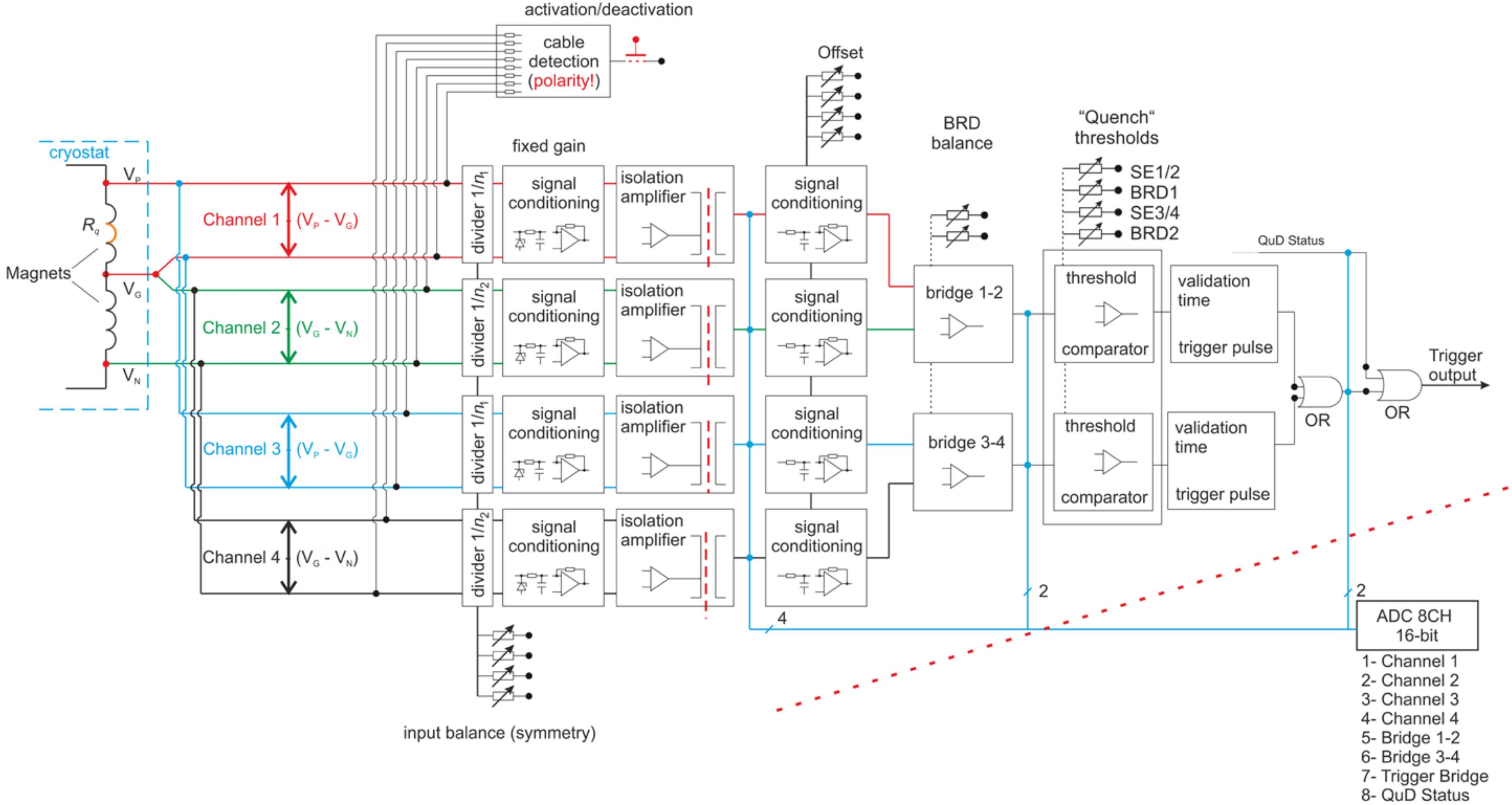
SIS100 – In-house development



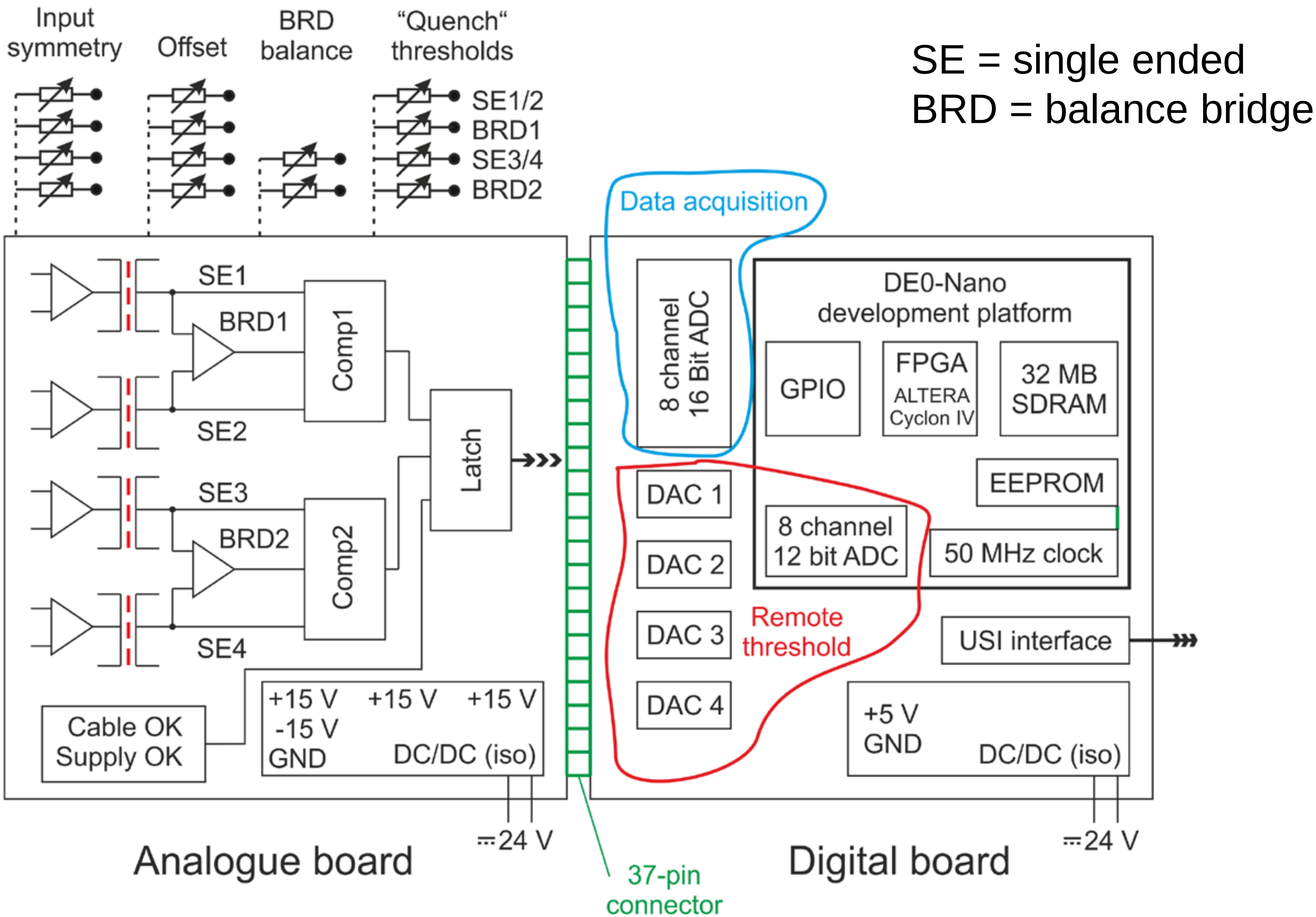
SIS100 Quench Detection System (Evolution)



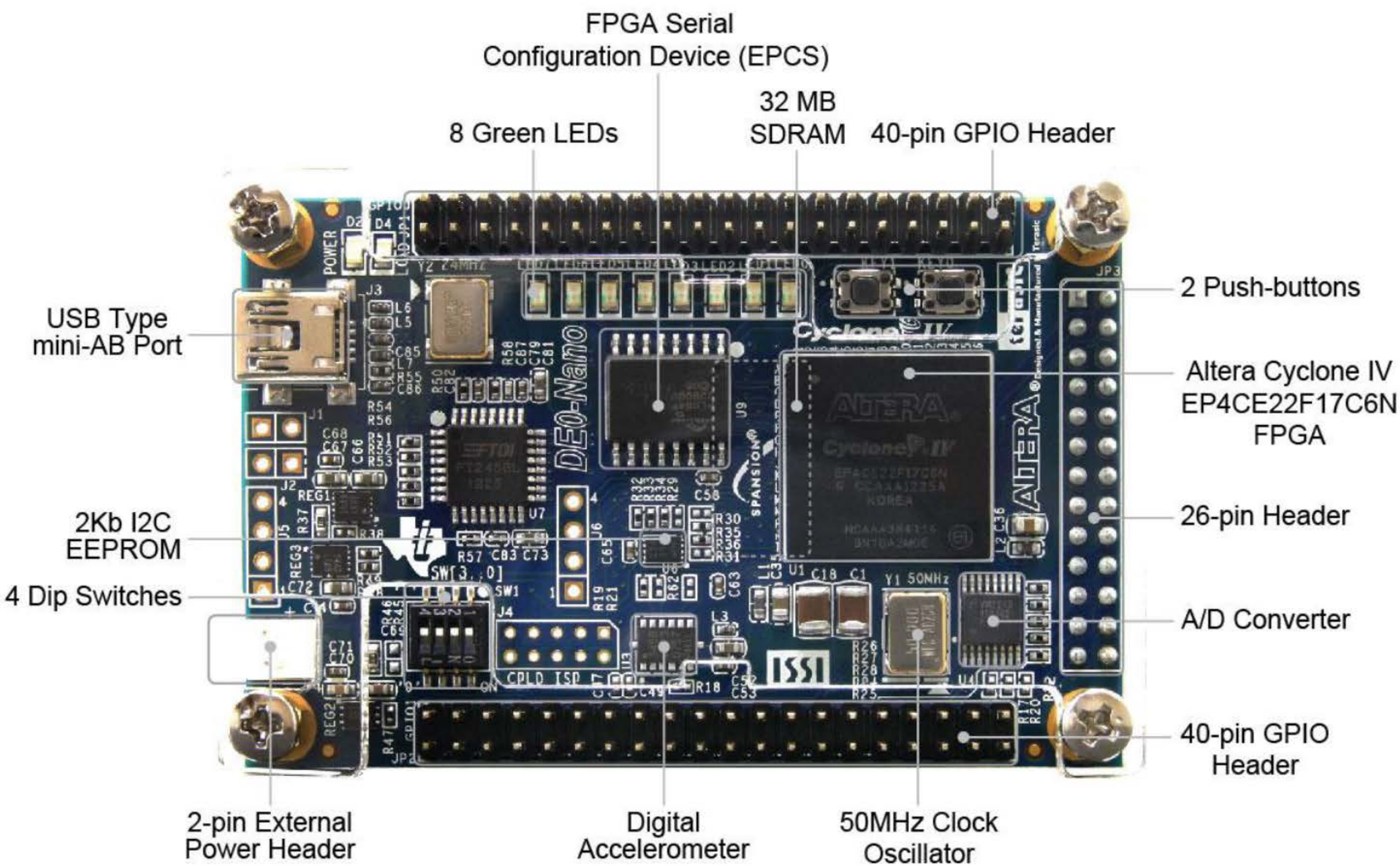
QuD Analogue Board



FAIR Quench Detection Electronics (Evolution)



DE0-Nano Development Platform



Digital Board

Functionality:

- Acquisition of the circuit voltages and transfer to the MFU
- Control of the QuD thresholds
- Remote control of the QuD
  - Reset of the QuD.
  - Reset of the QuD Trigger latch
  - Test each channel of the QuD (Quench test)
  - Read-out of the QuD type
  - Read-out of the QuD status

QuD Digital Board ↔ MFU

- Control and Readout of the QuD via FPGA : Reset, reset trigger latch, quench test, readout for QuD type, readout of QuD status.
- Transfer active quench trigger to the MFU in order to timestamp the quench event with accelerator timing.
- Data transfer from the FPGA to the MFU after a quench trigger and for very low frequency data logging and on-demand data recording.
- Launch on-demand recording with user selected parameters (number of signals to record, sampling rate, time span).
- Reset FPGA board
- Activation of the threshold control feature (to be seen if needed).
- Readout of the status of threshold control (active or not active).
- Setting and readout of the threshold values.
- Firmware upload: update of the FPGA firmware must be possible remotely from the FAIR control system.

QuD Analogue Boards

	QuD Type			
Analog Inputs #	**QuD for SIS100 Main Magnet circuits**	**QuD for SIS100 Corrector Magnets and Local Current Leads**	**QuD for SIS100 Main Current Leads**	**QuD for S-FRS Magnets and Local Current Leads**
1	V_P-V_G	V_{magnet}	V_{CU_MCL+}	$V_{magnet\_half\_1}$
2	V_G-V_N	V_{MID}	V_{CU_MCL-}	$V_{magnet\_half\_2}$
3	V_{bridge}	V_{bridge}	V_{HTS_MCL+}	V_{bridge}
4	V_P-V_G – from QuD redundant channel	V_{LCL+}	V_{HTS_MCL-}	V_{LCL+}
5	V_G-V_N – from QuD redundant channel	V_{LCL-}	Quench Trigger	V_{LCL-}
6	V_{bridge} – from QuD redundant channel	Quench Trigger		Quench Trigger
7	Quench Trigger			
8				

QuD i/o

Analog outputs to the QuD – Thresholds

Analog Outputs #	Description
1	Voltage Threshold QuD Channel 1
2	Voltage Threshold QuD Channel 2
3	Voltage Threshold QuD Channel 3
4	Voltage Threshold QuD Channel 4

Digital inputs from QuD

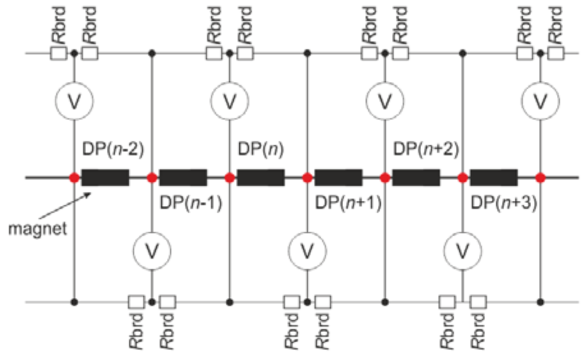
Digital Input #	Description
1	Quench trigger
2	QuD status
3	QuD type bit 1
4	QuD type bit 2
5	QuD type bit 3
6	QuD type bit 4
7	spare
8	spare

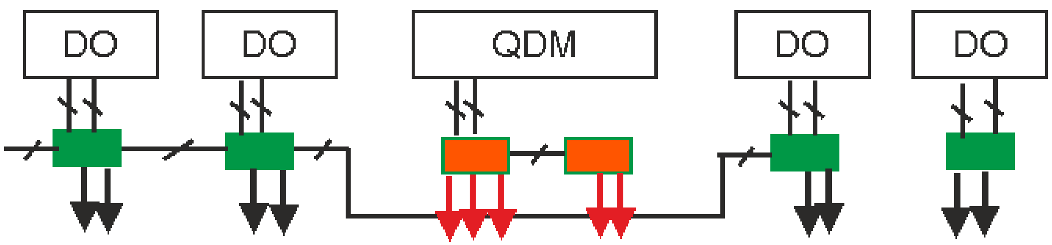
Digital outputs to QuD

Digital Output #	Description
1	Board reset
2	Trigger latch reset
3	Quench test QuD channel 1
4	Quench test QuD channel 2
5	Quench test QuD channel 3
6	Quench test QuD channel 4
7	Trigger for Threshold error & FPGA power failure
8	spare

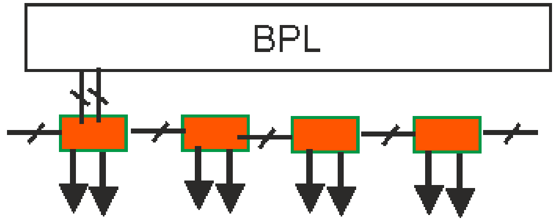
SIS100 Quench Detection System

Main circuits

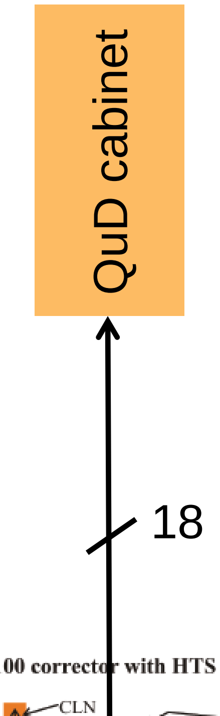




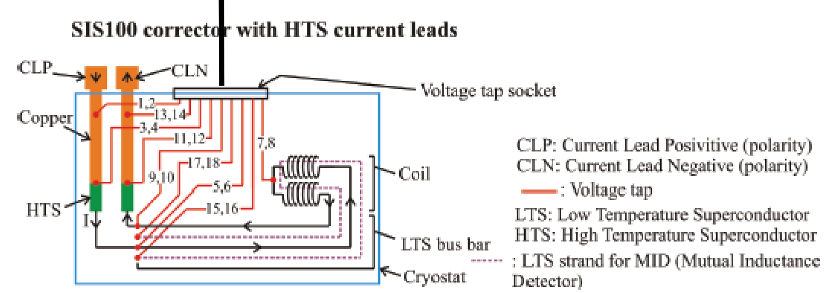
complicated HV cabling



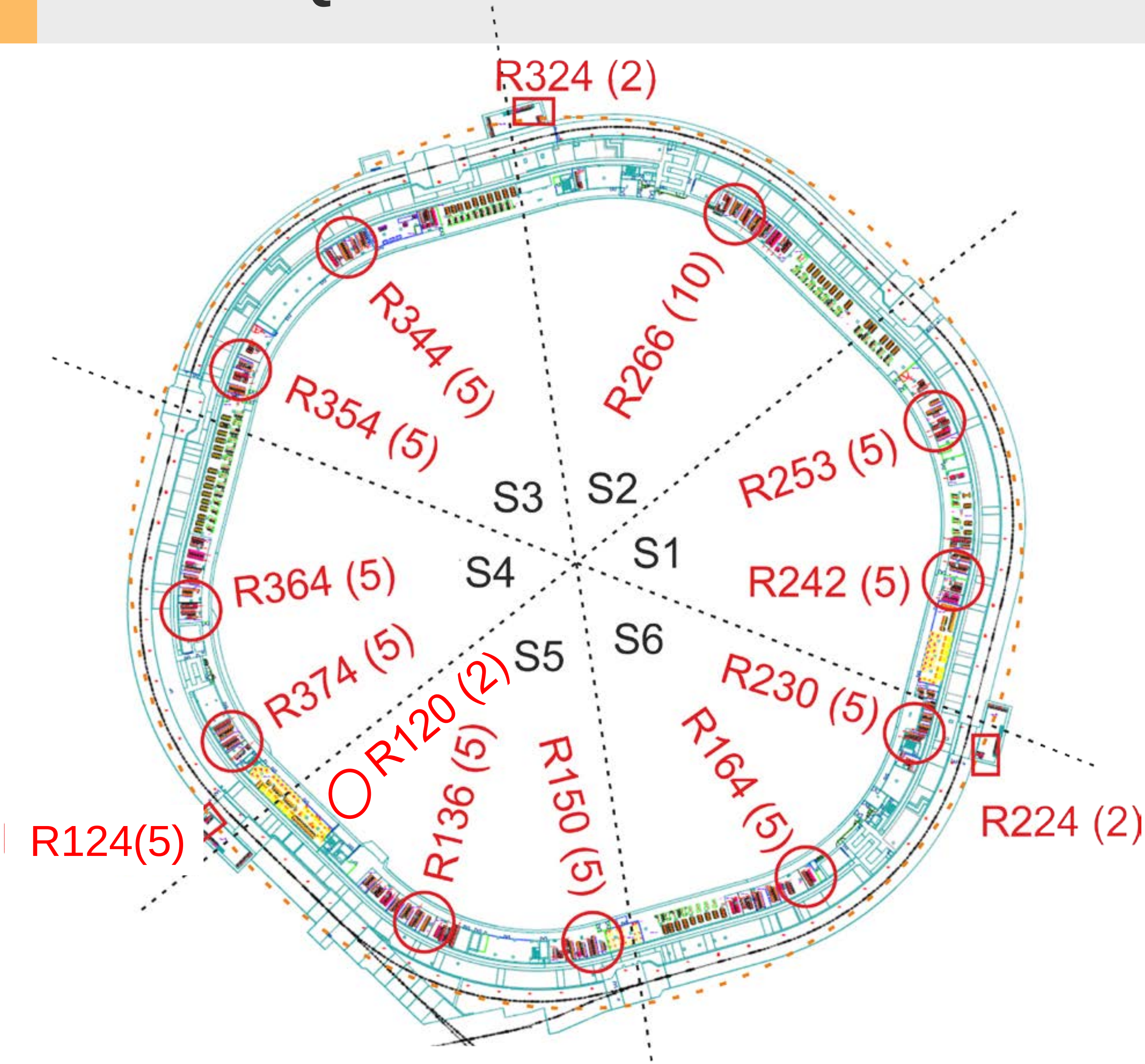
Correctors



Direct connection to the QuD cabinet



SIS100 Quench Cabinets Distribution

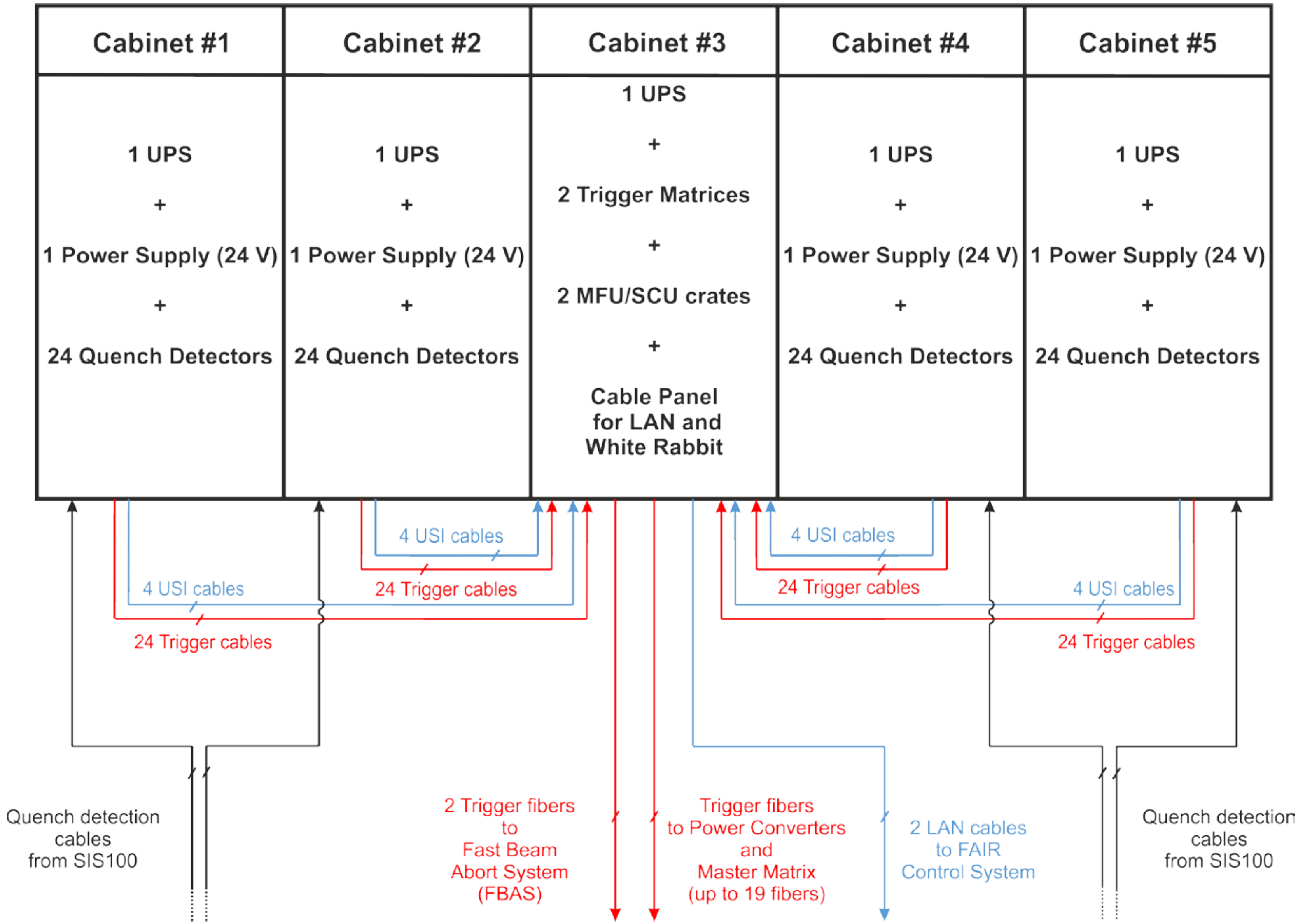


- 7 cabinets in (11+4) rooms
- cables up to 150 m
- cabling along the beam

- ~442 quench conditioning boxes at the support structure:
  - 1-2/ DP
  - 2/ QDM
  - 4/ BPL,
  - FB, CLB, EB...

- cabling concept is rather complicated
- several types of QCB layout

SIS100 Quench Detection System – Cabinet System



Thank you for your attention!

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