LHC: The Long Way (20 years) from the Initial Quench Detection System to UQDS (and beyond ...)

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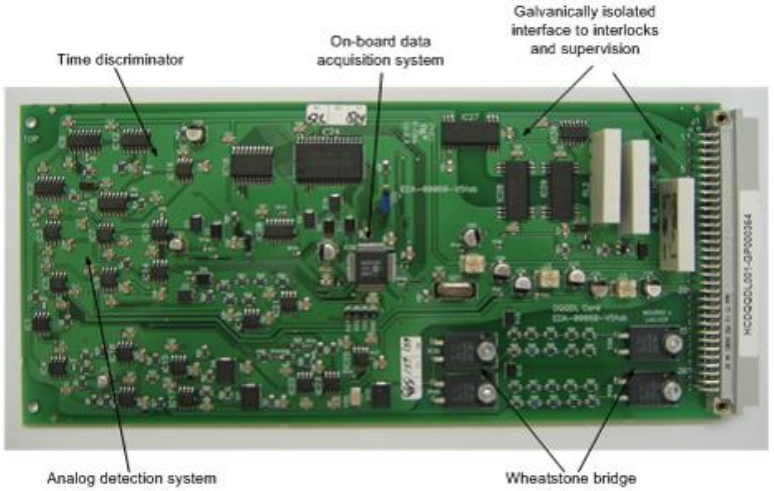
Introduction

- From the design start at the end of 20th century to the upcoming HL-LHC era, the LHC Quench Detection System (QDS) evolved significantly
  - The developments were mainly driven by changing requirements for quench detection and diagnostics e.g. timely detection of aperture symmetric quenches, protection and diagnostics of the bus-bar splices of the LHC main circuits, enhanced quench heater supervision …
- The LHC QDS has been relying from the beginning on digital signal processing to overcome limitations of classic analog solutions
  - 600 A corrector magnet circuits, HTS current leads …
- The LHC QDS has to cope with very specific technical constraints such as system size, very restricted access, ionizing radiation …

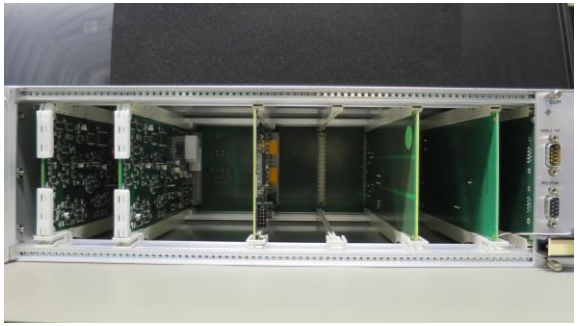
The starting point …

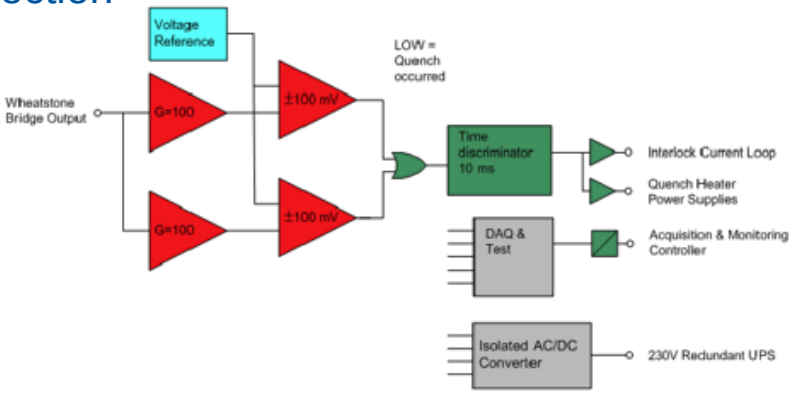
- Classical bridge type quench detection s
  and quads
  - Those type of devices are still in use on many
  - This is, what still many people (even experts) h
- Installed in STRING II (= fully functional
  prototype device for LHC
- STRING II outcome: device cannot be u
  - Too expensive, too noisy, not adjustment free, input stage not robust enough …



The LHC classical bridge detector - features

- Classical bridge design based on instrumentation amplifiers and comparators
  - Fixed quench detection settings (±100 mV, 10 ms)
- Detection circuit is referenced to the midpoint of the magnet; galvanic isolation by digital isolators, AD/DC converters and relays (interlock)
- On board micro-controller fore DAQ and test mode operation
  - Bridge signal can be used to qualify the internal magnet splices → several discoveries requiring magnet exchange …
- Radiation tolerant
- Very robust and highly dependable
  - 4032 units in LHC for main magnet protection
  - Partial replacement during LS2





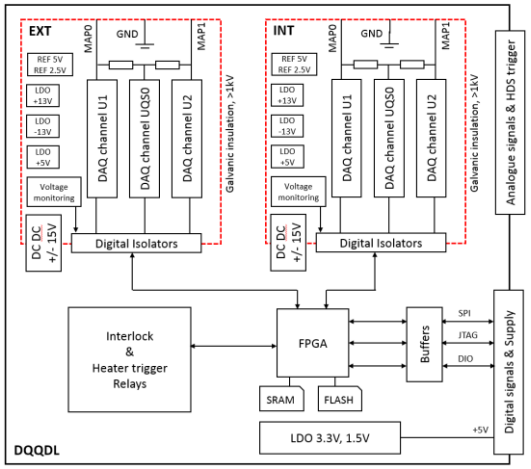
The LHC classical bridge detector – the scary list of known unknowns and unknown unknowns …

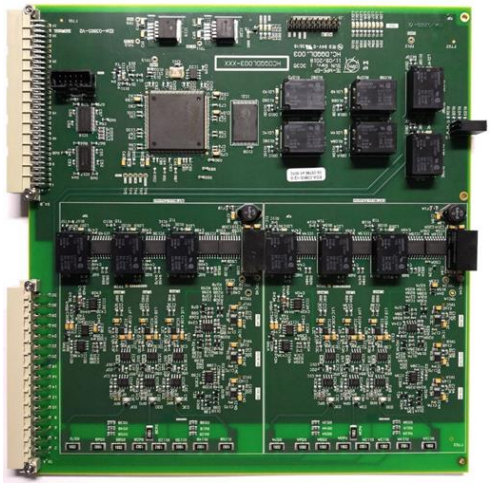
Class	Description	Solution / status
False positive	Bridge topology vulnerable to fast transients e.g. during fast abort sequences and powering failures	Fixed by changing activation sequence of energy extraction systems
	magnets in case of quench	training campaigns → pending
Reliability	(Too) late detection of aperture symmetric quenches	Installation of complimentary detection systems within nQPS upgrade.
Reliability	Partial loss of device powering may lead to blind detector without trigger	Upgrade to fully redundant power supplies including enhanced power supply supervision
Reliability	Accidental activation of test mode could render device blind	Firmware upgrade triggering software interlock
Availability	Local SPI bus could stall	Firmware & hardware upgrade
Availability	Latched PM DAQ trigger due R2E effect	Firmware upgrade (effect now used as a radiation monitor!)

- Those issues were either “discovered” in LHC or identified by system experts
- Luckily we had only near misses …

Beyond the classical bridge detector …

- New quench detector fro MQ protection replacing classical circuit board
  - LS2 upgrade driven by life cycle management; FPGA based (ProASIC 3E A3PE1500) mixed signal system
  - 2 in 1 design implementing two different detection algorithms
  - Optimized for MQ detection, enhanced DAQ systems
  - Advanced remote maintenance and device configuration





Design concepts – make or buy?

- The decision whether to use custom made electronics or buy commercial off the shelf systems is not straightforward
- The major (and very serious) drawback of using custom made electronics is the required expert level staff, also for the long term support
- Very few commercial suppliers offering suitable (and non exotic) solutions

ak points are typically the galvanic isolation, analog input stage protection, nectors and sometimes the quality/rating of the selected components

useful lifetime of a commercial product might be rather limited (<10 years)

ne commercial suppliers offer advanced and user friendly development ronments also for FPGA

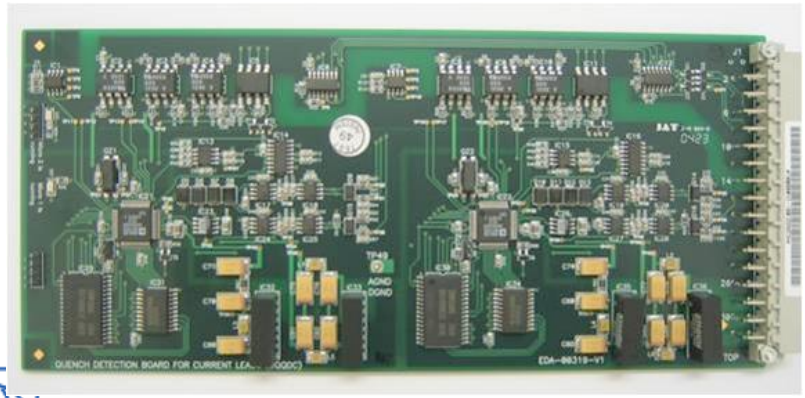
mpting approach but the verification of those tools for safety critical applications might be allenging

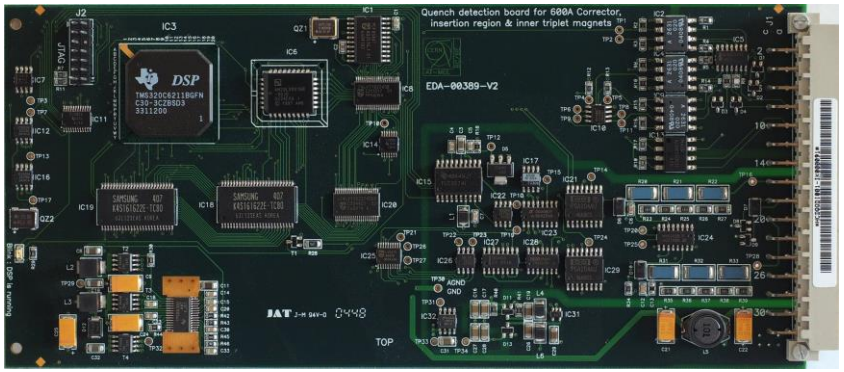
the art electronics is software defined → other than for mainstream h volume applications one cannot avoid the custom part

le kind of expert support level will be also required for commercial systems

Design concepts - digital (=mixed signal) quench detection systems

First applications of digital quench detection systems in LHC	
HTS current lead protection	600 A corrector circuit protection
• 1 mV, 3 mV 100 ms • 2 x 1198 devices in LHC • Highly dependable circuit board • The bus-bar splice protection system (2 x 2068) introduced in 2008 is a clone of this board.	• 100 mV 20ms • Detection scheme avoids voltage taps on individual magnets (essential for the spool piece correctors) but is very challenging to implement.
• ADUC834™ micro-converter with 24 Bit Σ-Δ ADC	• TMS320C6211™ DSP + 14 Bit SAR ADC





Design concepts – digital quench detection systems – the 600 A case

- Perfect and elegant solution for all low inductance corrector circuits especially the spool pieces
- A less good solution for many other corrector circuits requiring enormous efforts by QPS, power converters and LHC operation to get those circuits commissioned at all
  - As direct consequence, all HL-LHC superconducting circuits are equipped with a gazillion of instrumentation voltage taps
- Once one manages to ramp the circuit, the algorithm itself is one of the most reliable for quench detection (e.g. with built-in symmetric quench detection … used recently for the 11 T prototype tests in SM18)
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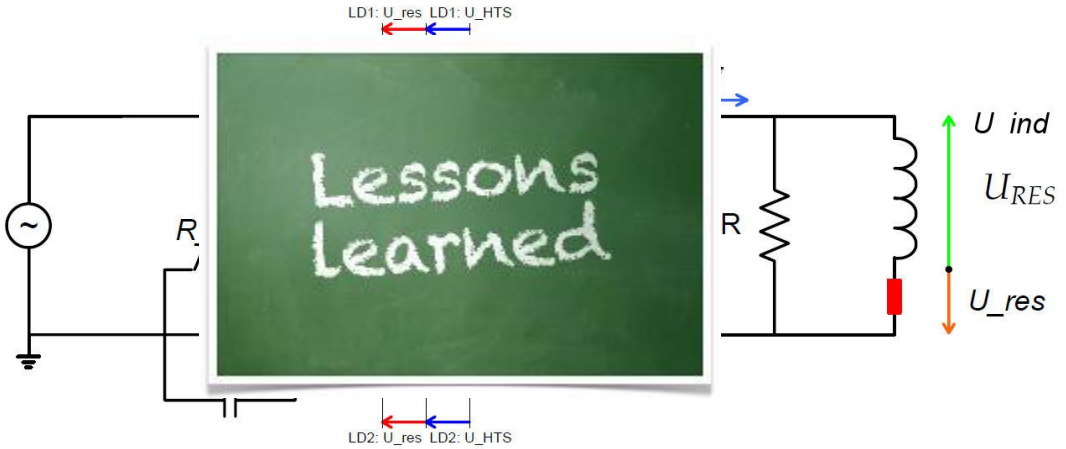
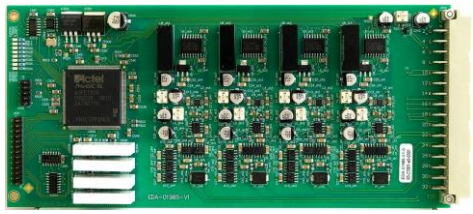


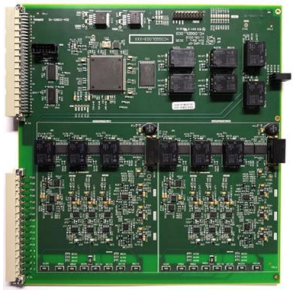
$$U_{RES} = U_{DIFF} + L(I) \cdot \left(\frac{\partial I}{\partial t} + \frac{\partial U_{DIFF}}{\partial t} \cdot \frac{1}{R_{PAR}} \right)$$

Design concepts - digital (=mixed signal) quench detection systems

- The emerging flash based FPGA with reasonable radiation tolerance (in contrary to the DSP) and affordable pricing triggered the development of FPGA based QDS and DAQ for LHC





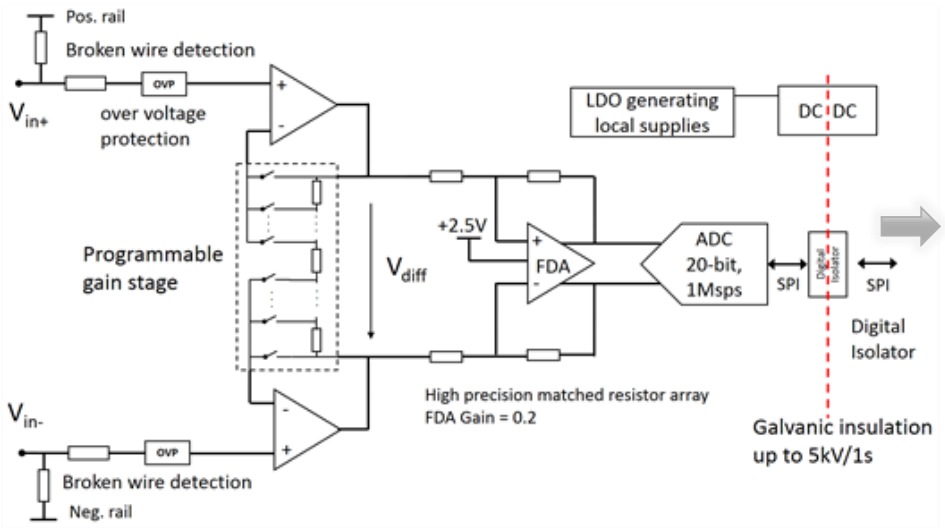
- The growing zoo of FPGA based circuit boards eventually triggered the development of the **U**niversal **Q**uench **D**etection **S**ystem

Design concepts – recent developments

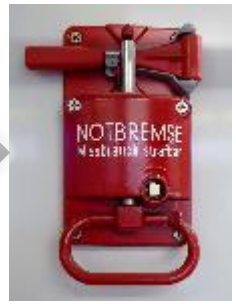
- 21st century electronics allows the development of high performance versatile quench detection systems including integrated high resolution fast DAQ systems
- Key elements are:
  - Fast high resolution SAR ADC (e.g. 20 Bit 1 Msps)
  - FPGA for signal processing, implementation of the quench detection logic, controls interface
    - Fully parallel processing capability, implementation of finite state machines (FSM) as an important element for mission critical applications
    - Without the constraint radiation tolerance it is strongly recommend to base the development on widely used FPGA types
  - Digital isolators and DC-DC converters providing galvanic isolation

Design concepts – the analog front-end

- The analog front-end provides several import functions
  - Analog signal conversion (of course …)
  - Signal conditioning prior to ADC conversion (anti-aliasing filter, programmable gain amplifier …)
  - Broken instrumentation wire detection
  - Overvoltage protection → worst case to be considered …
  - Galvanic isolation



Digital logic



Interlock

Design concepts – all the rest

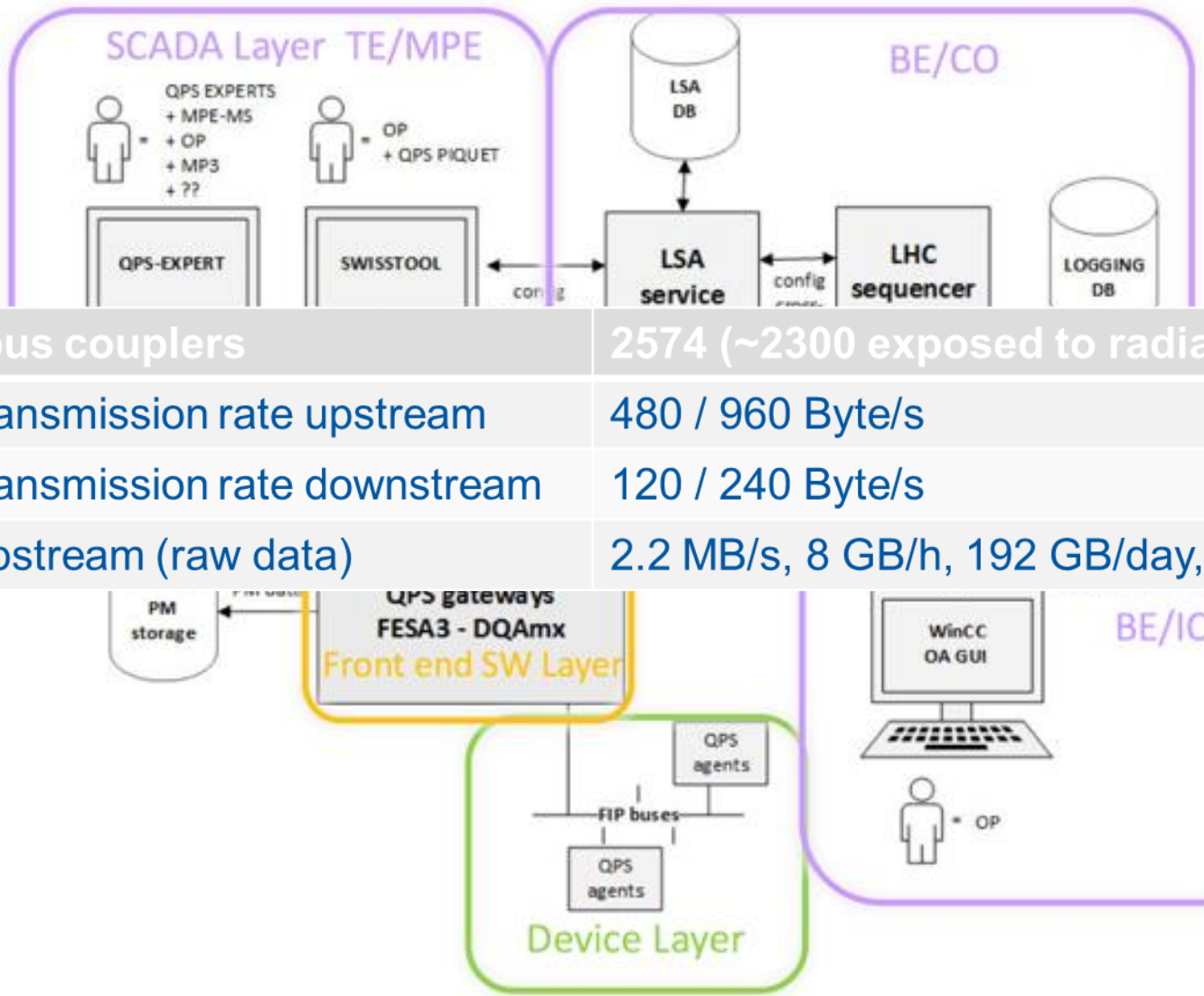
- Galvanic isolation:
  - Always in the digital signal path, preferably directly after the ADC
  - ⚠ Electrical tests have a tendency to exceed the specified insulation voltage ratings significantly. This concerns in particular the duration of the tests. Maximum voltage ratings given by part manufacturers usually refer to surge voltages.
- Power supplies:
  - Powering should be always fully redundant. Detection systems, which use active triggers, must be fed from two independent UPS (“U” may not necessarily mean uninterruptable …)
  - The redundancy is only effective in combination with a dedicated power supply supervision
  - The combination of isolated DC-DC converters with LDO regulators gives satisfying results with respect to noise and stability
- Interlocks:
  - LHC uses a combination of hardwired interlocks (for fast power aborts and activation of protection devices) and software interlocks (verification of system readiness, loss of redundancy …).
  - Current loops are still first choice and should be differential.

CERN

Data transmission & controls

- All LHC QDS use either SPI™ or I²C™ as local data bus
  - Having some serious inherent flaws the I²C™ bus it is no longer used in new designs
- The local data transmission volume for QDS does not justify the use of more advanced and fancy concepts like MicroTCA™
- In addition to the local data bus some hardwired lines are used (PM trigger, test mode and power cycle enable …)
- The field-bus coupler interface provides the link between the local communication bus and the field-bus or any other data transmission link
  - The field-bus network is used as well for absolute timing synchronization
- In the LHC the most serious limitation is the required radiation tolerance; without this restriction there is a very wide choice of possible solutions
  - HL-LHC will use PowerLink™ as an Ethernet based field-bus

Data transmission & controls



Field-bus couplers	2574 (~2300 exposed to radiation)
Data transmission rate upstream	480 / 960 Byte/s
Data transmission rate downstream	120 / 240 Byte/s
Total upstream (raw data)	2.2 MB/s, 8 GB/h, 192 GB/day, 70 TB/year

Quench detection versus controls

- A properly designed QDS should have only two macroscopic states, either it is running or its interlocks are activated

Task	Conditions	Who
Reset	No beam, zero current, valid controls access token (RBAC)	Expert, operator, sequencer (unlatching of interlocks may require additional permissions)
Power cycle	No beam, zero current, valid controls access token (RBAC)	Expert
Device configuration update	No beam, zero or stand-by current, valid controls access token (RBAC)	Guru (maximum safe settings are hard coded)
Interlock test device level	No beam, zero current, valid controls access token (RBAC)	Expert
Interlock test circuit level	No beam, zero current, valid controls access token (RBAC)	Guru (parallel execution not permitted)

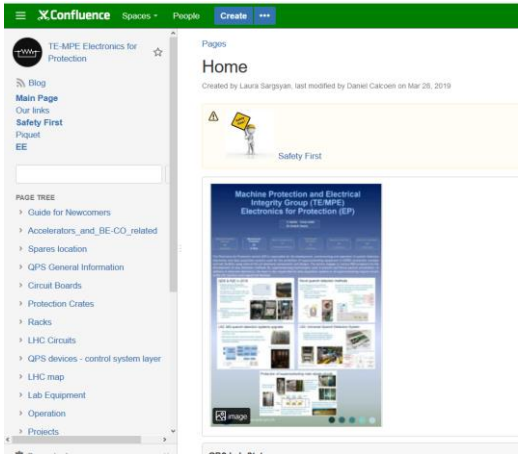
Design verification & system testing

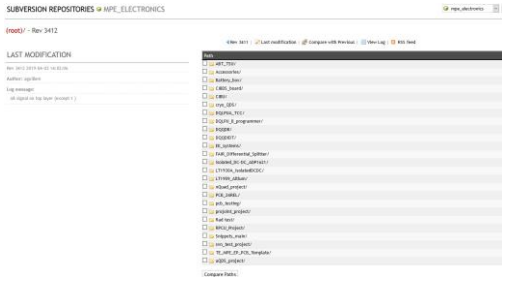
The very thorough test procedures are complimented by other methods such as reliability calculations (e.g. for the validation of the required system redundancy and the frequency of recurrent tests), quench and circuit simulations, personal safety assessment by respective experts, various design reviews and a proper project management.

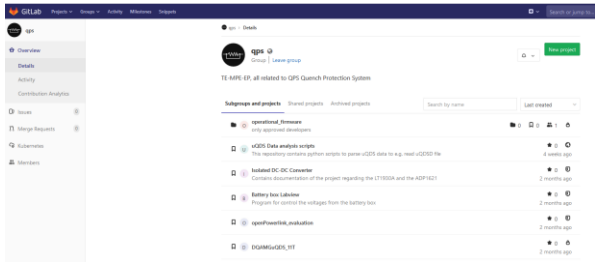
Type testing	Verify that device complies with functional specification	By team members not being the core developers
Functional testing	100% functional test prior to installation	Dedicated test team, in most cases fully automatic
Individual system test	After installation prior to powering, needs to be repeated on a regular basis	System specialist, in most cases fully automatic execution and report generation
Device self-check	Automatic verification of crucial settings	Automatic and linked to software interlock (QPS-OK)
Integrity checkers	Check permanently per-defined sets of signals and device parameters	Automatic but non-interlocking; creates warnings for experts
Automatic event analysis	Analysis of PM events e.g. a magnet quench	Automatic with report generation; re-start may require the permission by a human

Documentation

- Documentation is an very essential part of the complete design process asking for quite some effort:
  - Should document the design process and decisions taken
  - Provide all information required for manufacturing, test and commissioning, operation and maintenance
  - Include an exhaustive documentation of the device firmware and the respective API
  - Document and if needed archive the toolchains for device firmware development







Conclusions

- Since its initial deployment the LHC Quench Detection System (QDS) evolved significantly
- The enhanced diagnostic capabilities of the QDS are essential for the operation of the LHC superconducting circuits
- Recent developments profit largely from advances in electronics
- Further system evolution focuses on life cycle management, compatibility with increasing LHC energy and intensity, HL-LHC, fully automatic system operation and maintenance, high dependability …

QPS: what the user asked for

QPS: what the user actually needed

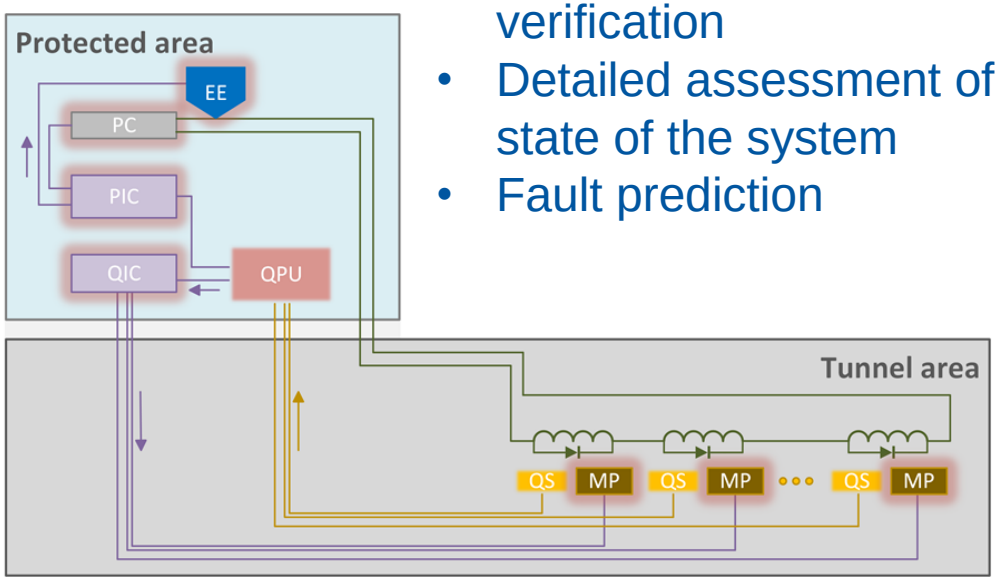
The crystal ball … QDS for the FCC era

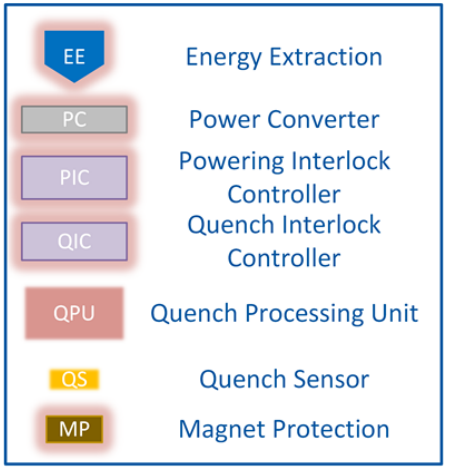
- With the actual baseline a substantial QDS will be required for the FCC-hh
- FCC-hh will operate from ~2045 to 2070, meaning that QDS electronics design would start earliest ~2035
  - Nevertheless, a preliminary design study has been presented at the FCC week 2018

Thanks

QPU == deep neural network

- Sophisticated system verification
- Detailed assessment of the state of the system
- Fault prediction





T. Podzorny

THANKS
FOR
LISTENING