UQDS
Design, status & operational experience

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Topics

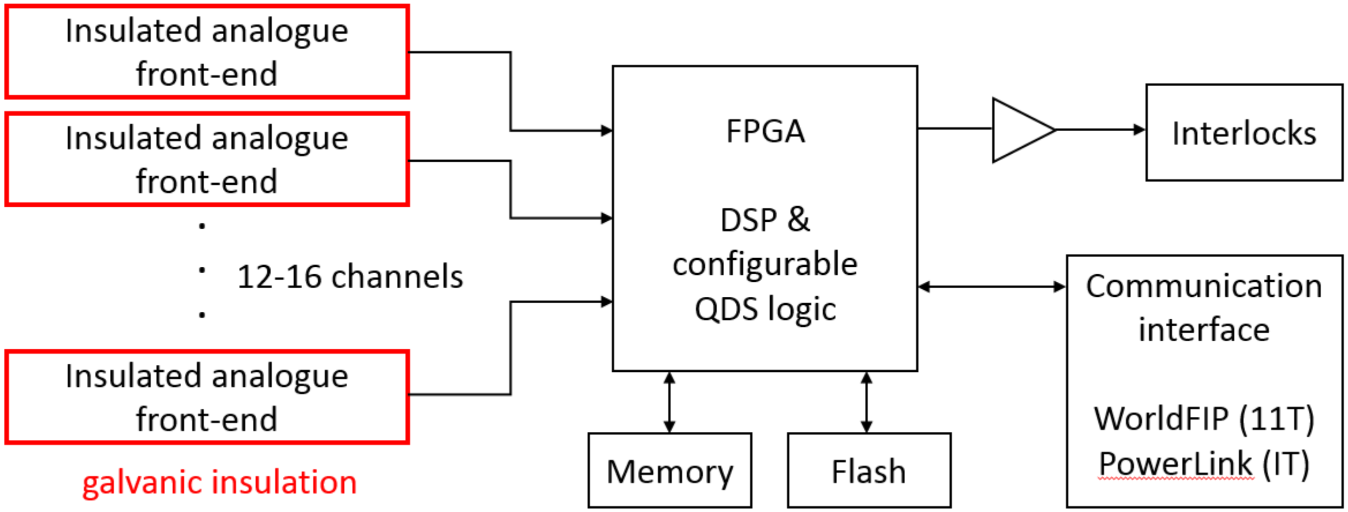
- UQDS concept
- UQDS design & performance
- Operational experience
- Conclusion

Motivation

- After LS1 (2015) multiple requests for protection of either HiLumi magnets and test-benches appeared
- Current QPS zoo of quench detectors was already quite large and divers
- “One size fits most” approach was taken
- Strong wish of the community for good DAQ capabilities

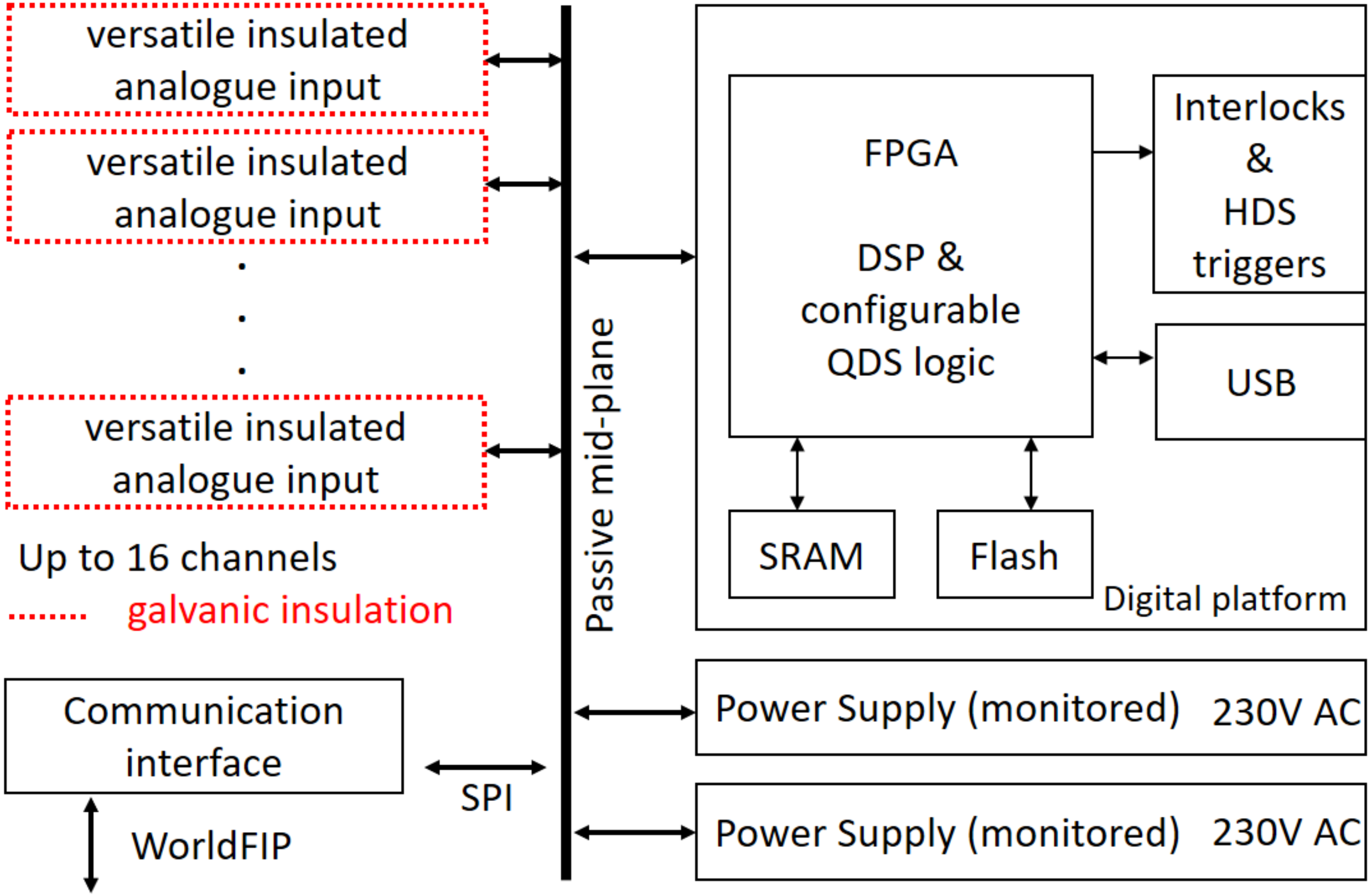
➔ Development of a flexible, generic system started

UQDS concept

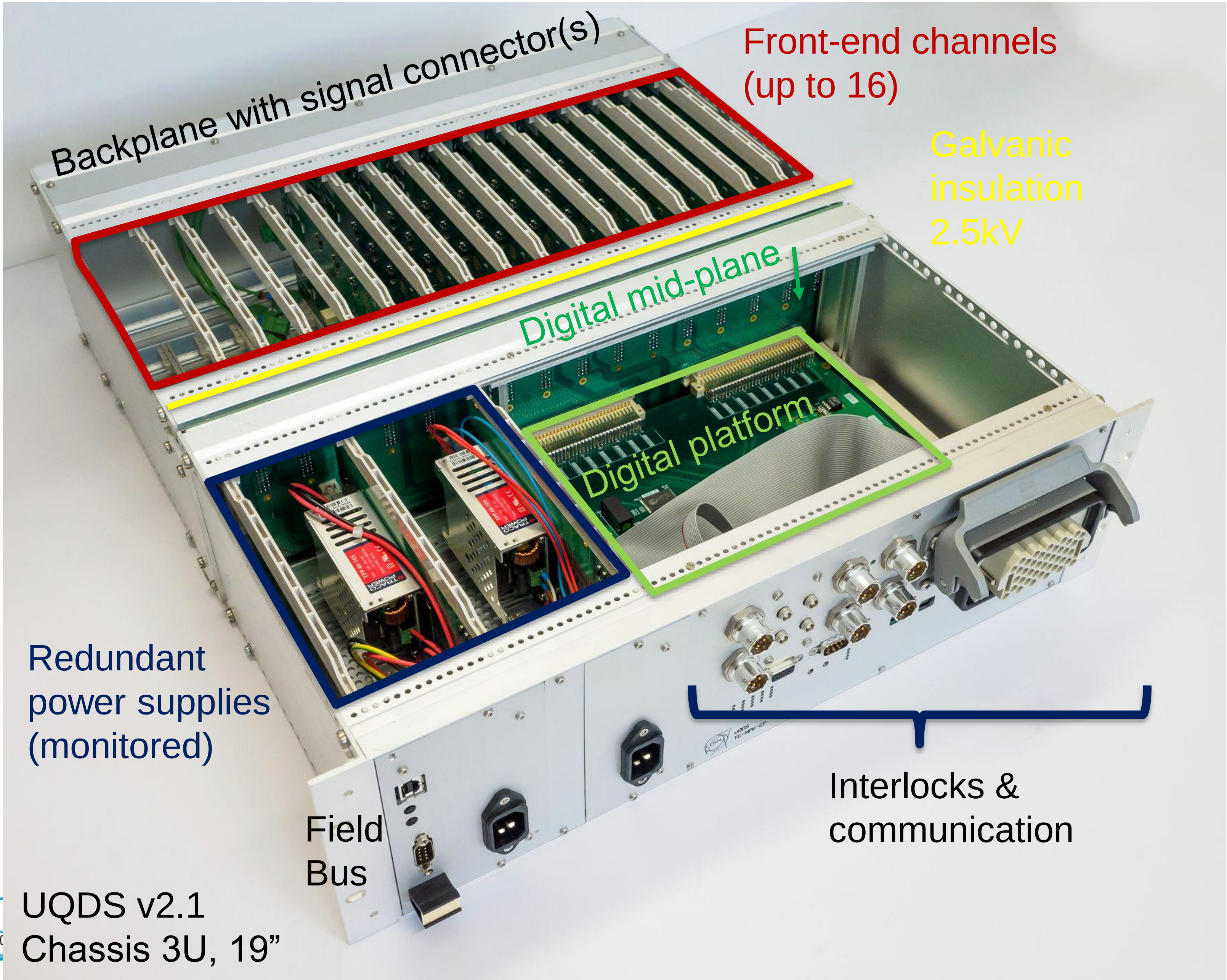


- Multiple front-end channels connected to one logic device performing the QDS tasks
- QDS function defined by FPGA firmware
- Front-ends flexible enough to cope with all required input signals
- Modular concept, one platform for various tasks

General design



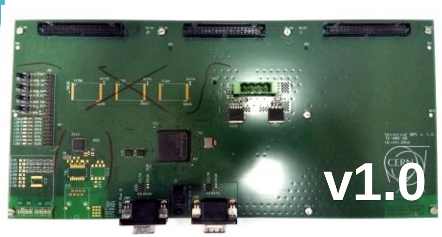
UQDS version 2.1, system overview

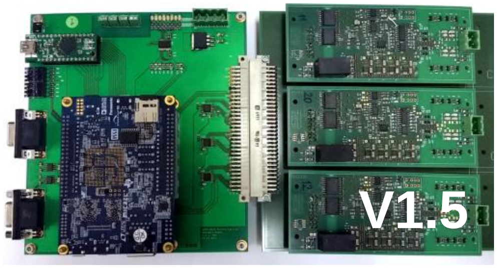


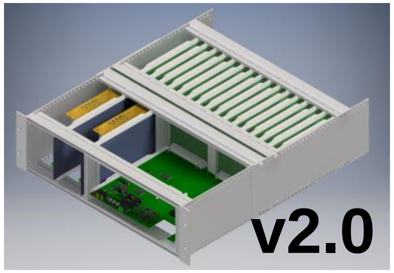
UQDS components

- **Digital platform** houses FPGA, interlocks and communication interface. Performs quench detection algorithms
- **Mid-plane** connects Front-end with Digital platform
- **Frontend** amplifies signal, digitizes and provides galvanic insulation
- **Power supplies** (redundant) including supervision
- **Auxiliary communications controller** to integrate system into controls infrastructure

Digital platform history







- First board with Microsemi IGLOO2 (M2GL060)
- Hosts up to 3 frontends
- Communication via RS485 (2.5Mbit)

➔ Proof of concept

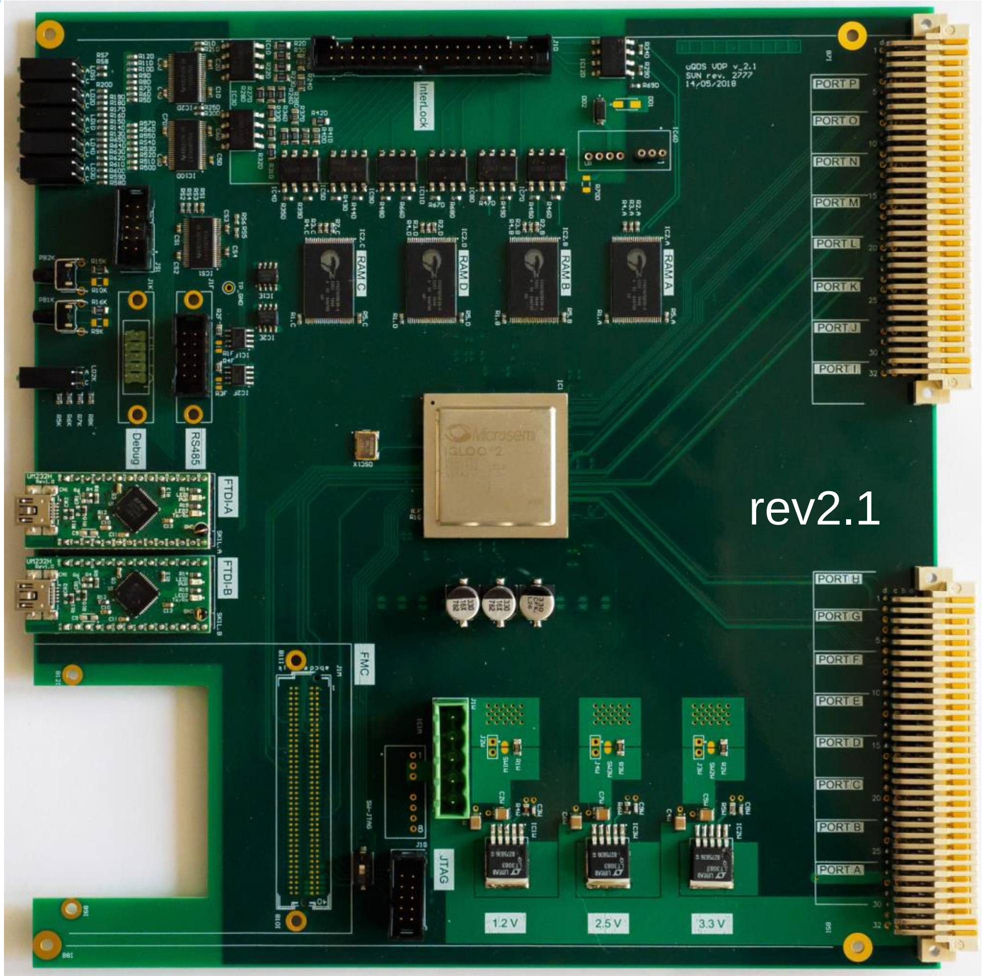
- INTEL dev board on carrier
- Supports channel carrier with 6 frontends
- Communication via USB 2.0 and RS485

➔ Intermediate solution for SM18 and LHC tests

- Based on IGLOO2 (M2GL150)
- Supports up to 16 front-ends via midplane
- Communication via RS485, USB 2.0, USB 3.0 or WorldFIP

➔ First prototype for 11T QDS

Digital Platform (VDP)



- Based on IGLOO2 (M2GL150)
- Supports 16 front-end channels via mid-plane
- FMC expansion slot
- 18 isolated trigger outputs
- 2/2 sync lines
- Rad-tol up to 100Gy (tested in CHARM)

➔ Baseline for 11T QDS

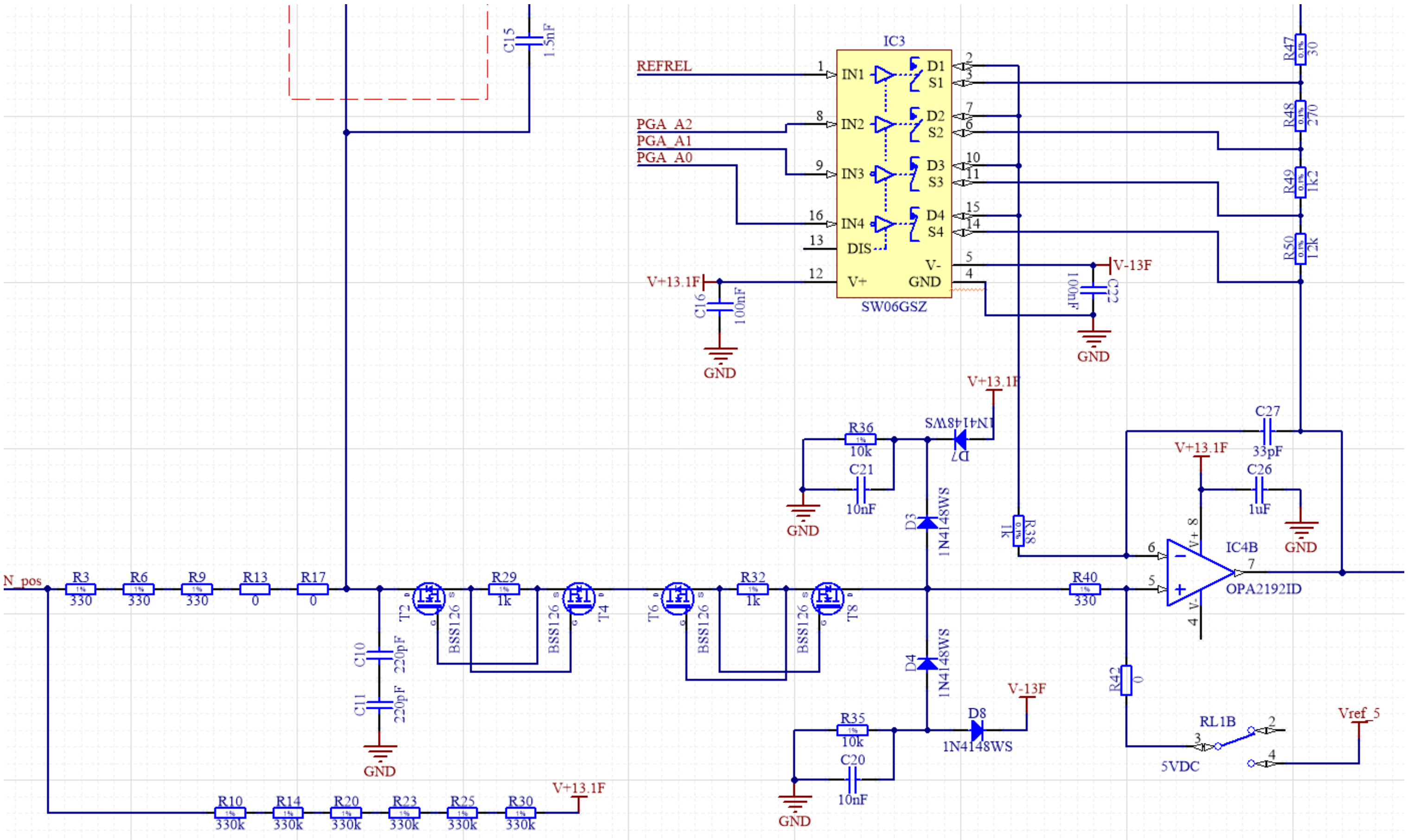
Digital platform: communication interfaces

- Slow control

Action	Line	1	2	3	4	5	6	7	8
Write register		Write (0x01)	Reg address	B0	B1	B2	B3	CRC	
Ex: Write register 0x23 with value 0xAB1200FF	MOSI/TX	0x01	0x23	0xAB	0x12	0x00	0xFF	0x64	
	MISO/RX	ignore	ignore	ignore	ignore	ignore	ignore	ignore	
Read register		Read (0x02)	Reg address	CRC (tx)	B0	B1	B2	B3	CRC (rx)
Ex: Read register 0x05 with value 0xAB1200FF	MOSI/TX	0x02	0x05	0x07	0x00	0x00	0x00	0x00	0x00
	MISO/RX	ignore	ignore	ignore	0xAB	0x12	0x00	0xFF	0x46

- Continuous readout
  - RS485, 2.5Mbit continuous data readout for remote and/or radiation areas
  - USB 2.0 (480Mbit) for test benches and lab usage (streaming of 16ch @ 200kHz possible)

Front-end channel design

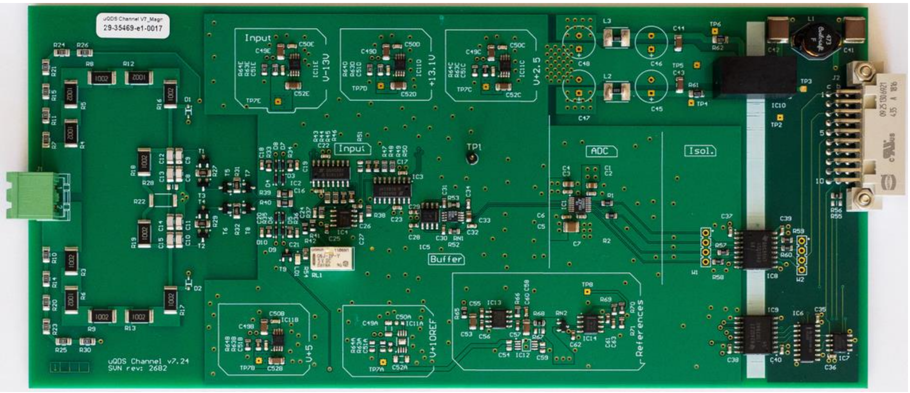


- Full Galvanic insulation, and robust inputs
- Wide input range without divider: +/-22.5V
- Broken Vtap detection (if no divider is used)

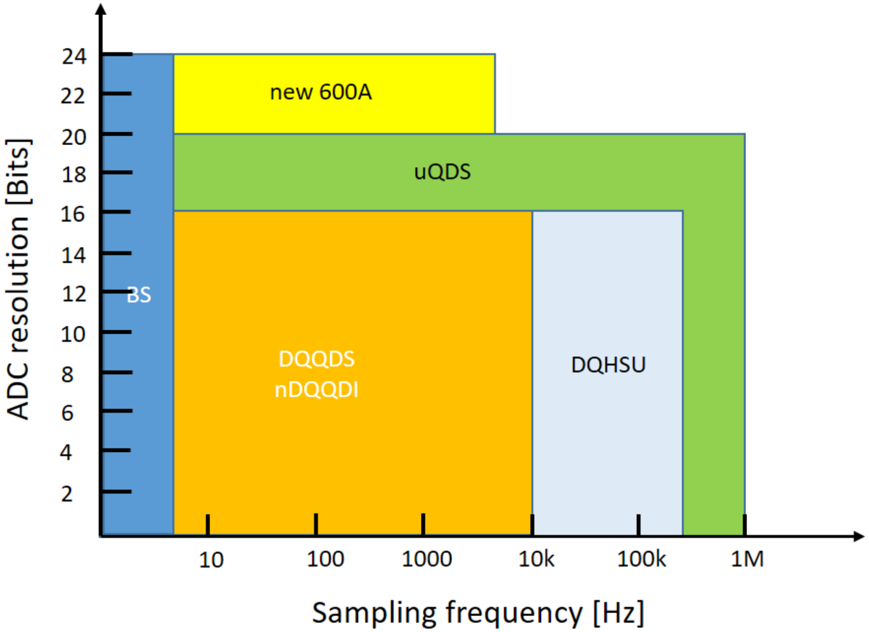
Front end specification

Parameter	Value
Resolution (20-bit ADC)	106nV/LSB .. 47uV/LSB
ADC speed	Up to 1Msp/s
Analogue bandwidth/ gain	125kHz @ G=1 90kHz @ G=9 50kHz @ G=45 7kHz @ G=450
Active input voltage range without divider	+/-50mV .. 22.5V
Input voltage range with divider for FAIR magnets	G=1/6: +/-135V
Max differential input voltage	1kV/1s
Galvanic insulation	2.5kV/20min, 5kV 1s

➔ Covers all our needs and adds healthy reserve for the future



Front-end rev7.24 (UQDS 2.x compatible)



Front-end channel status & performance

- UQDS 2.1 compatible version since spring this year
- 50 channels produced v7.24 (mainly for FAIR test-bench)
- Characterization of production shows good reproducibility of noise etc.
- High input range version with additional divider (up to +/-135V)
- Standard range version (+/-22.5V)

➔ Current version v7.24S serves as baseline for 11T UQDS boxes

Front-end channels performance

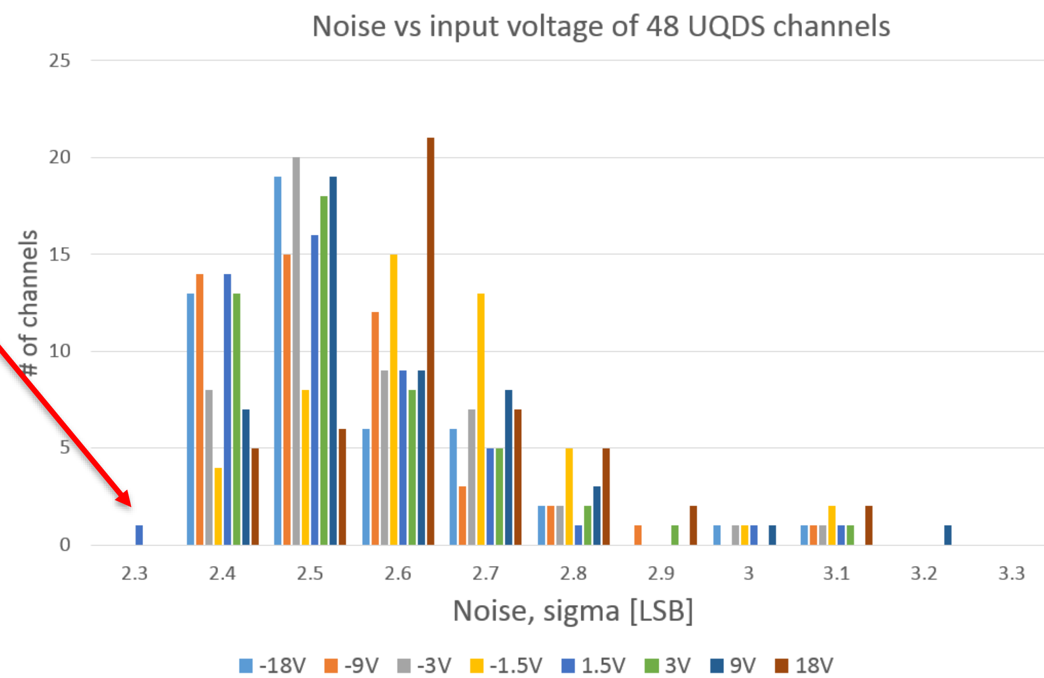
- Bandwidth

125kHz @ G=1, Vin = +/-22,5V
90kHz @ G=9 Vin = +/-2,5V
50kHz @ G=45 Vin = +/-500mV
7kHz @ G=450 Vin = +/-50mV

- Noise at different input voltages (G=1 or G=0.16)

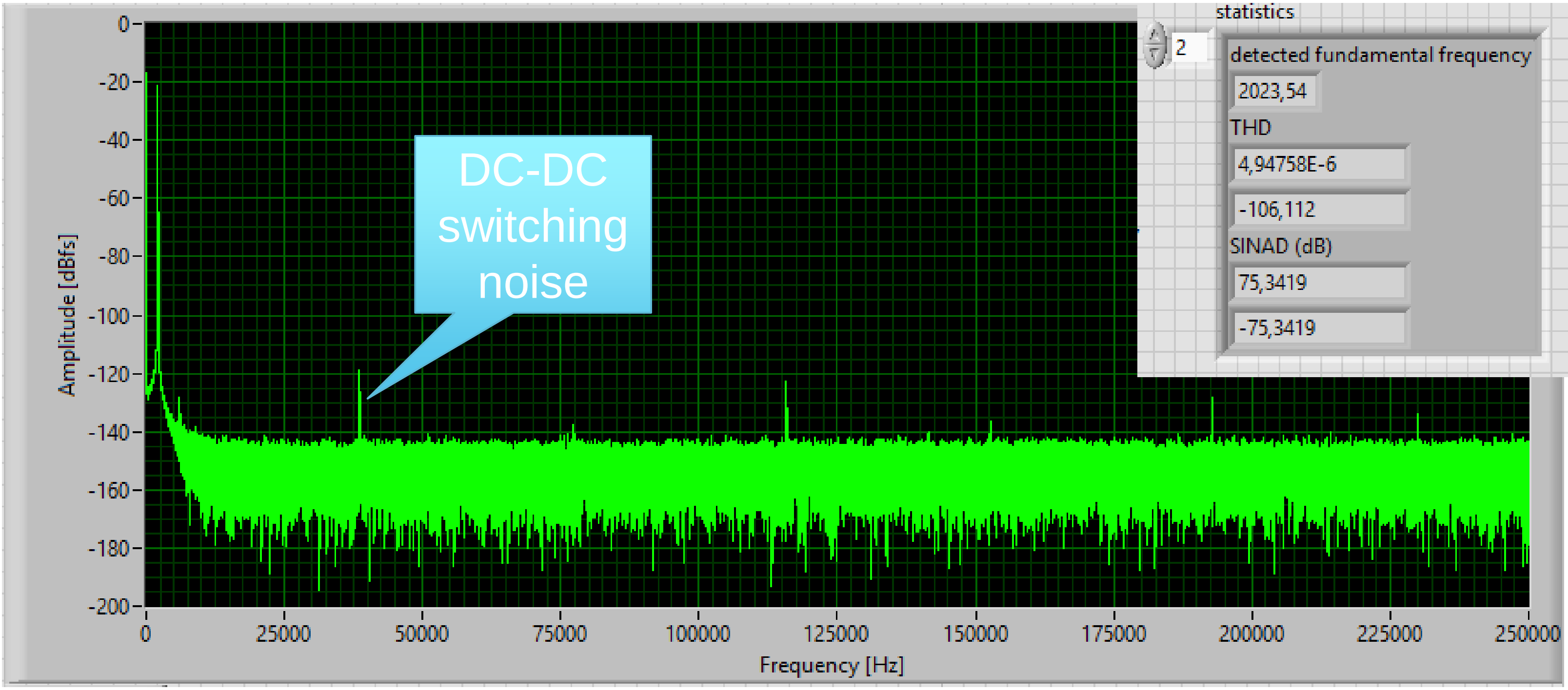
σ=2.3 LSB ADC lower limit
(data sheet performance)

1LSB = 47uV RTI @ g=1



Front-end channel performance

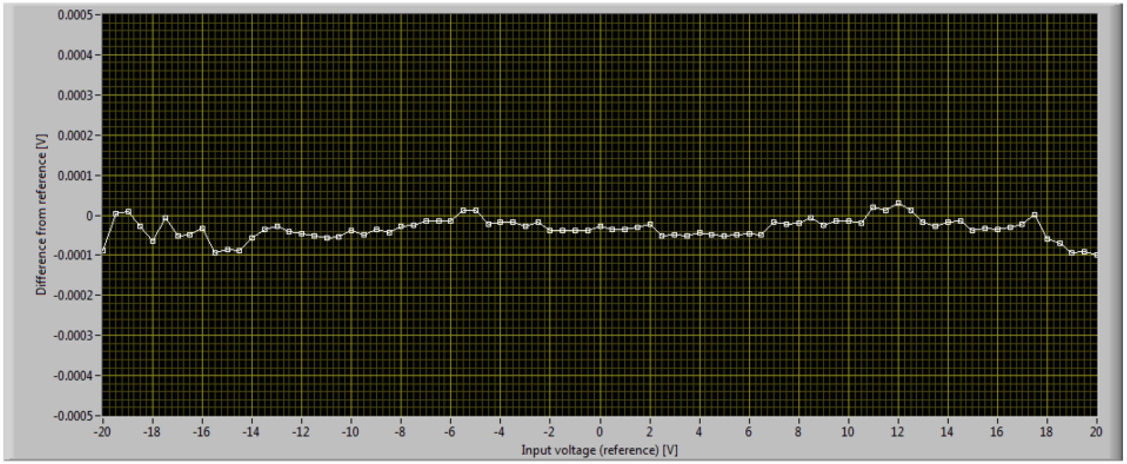
- Total harmonic distortion (THD)



➔ Excellent dynamics despite complex and robust front end

Front-end channels performance

G=1
linearity
< 5ppm RTI
(gain & offset calibrated)

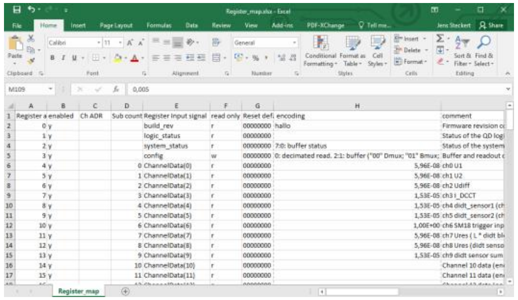


- All in all quite good performance (dynamic and static)
- So far we were never limited by the channel performance during operation (SM18 tests)

FPGA firmware

- Function of UQDS is fully defined by the FPGA firmware
- Various requests and configurations lead to several versions of the firmware
- Currently a unified firmware is under development which is largely generated by scripts
- This way the firmware creation process is simplified and usage of verified functional blocks simplifies verification
- Firmware is written in generic VHDL porting it to different FPGA is quite straight forward…

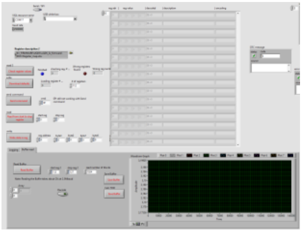
FPGA Firmware



Excel file with register map and function definition (which protection block)

Defines

Scripts



Fast readout screenshot

Operational software

Generate register file

.vhd

Select protection function

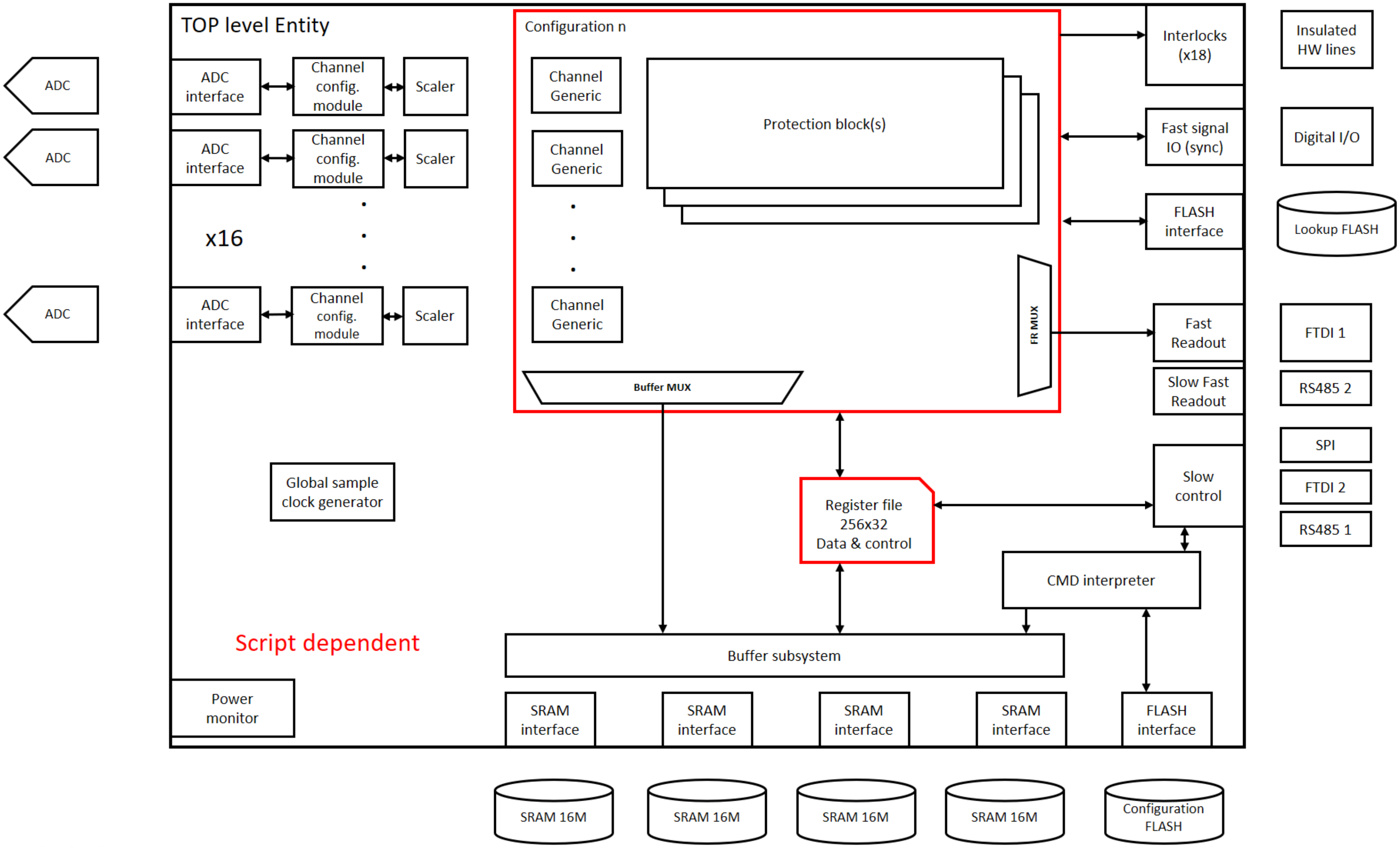
.vhd

Configure generics

FPGA toolchain

Firmware for protection

Firmware structure



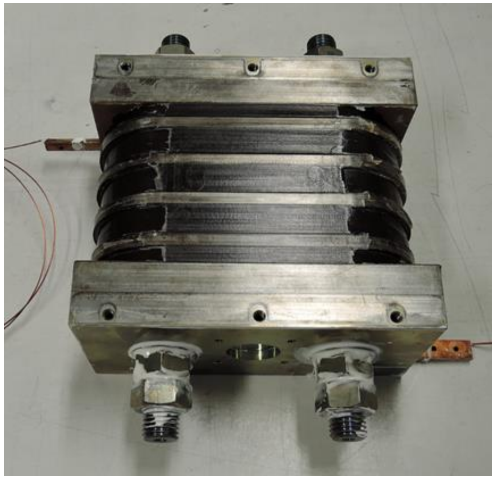
UQDS 2.x usage

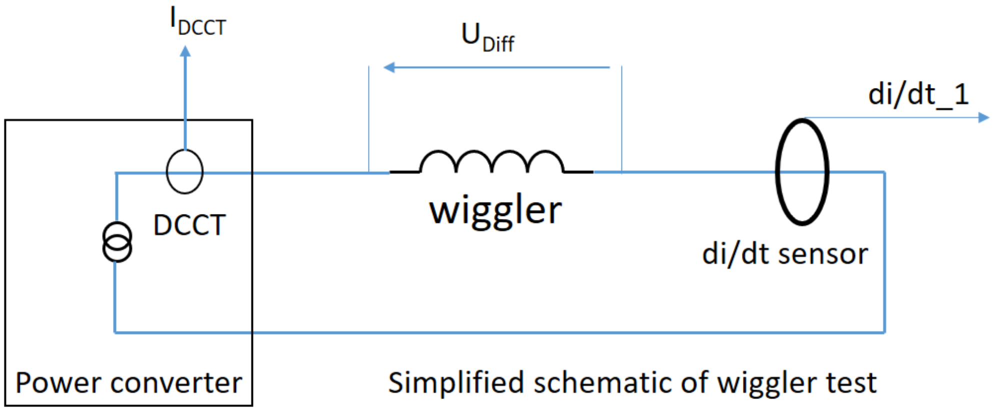
User	Usage	Date	#
MPE/SM18	DAQ for Nb3Sn magnet testing	2018	1-2
SM18	CLIC Nb3Sn wiggler test quench detection: first usage as protection device !	Sep 2018	2
SM18	HiLumi 11T Nb3Sn magnet single aperture prototype test: quench detection	Feb 2019	2
SM18	HiLumi MgB2 18kA Super conducting link test: quench detection	Mar 2019	2
FAIR test bench	Quench detection on FAIR magnets	2019 Apr	2 (18)
B163	FRESCA2 quench detection	2019	10
SM18	Cluster F quench detection	2019	Tbd.
LHC	11T quench detection	2020	6
SM18	IT string quench detection	2021	Tbd.

Operational experience

- So far three use cases as protection device
  - Nb3Sn wiggler magnet quench detection
  - 11T magnet quench detection
  - MgB2 18kA superconducting link & HTS current leads quench detection
- Next usage on CERN FAIR test-bench !

Operational experience: Wiggler

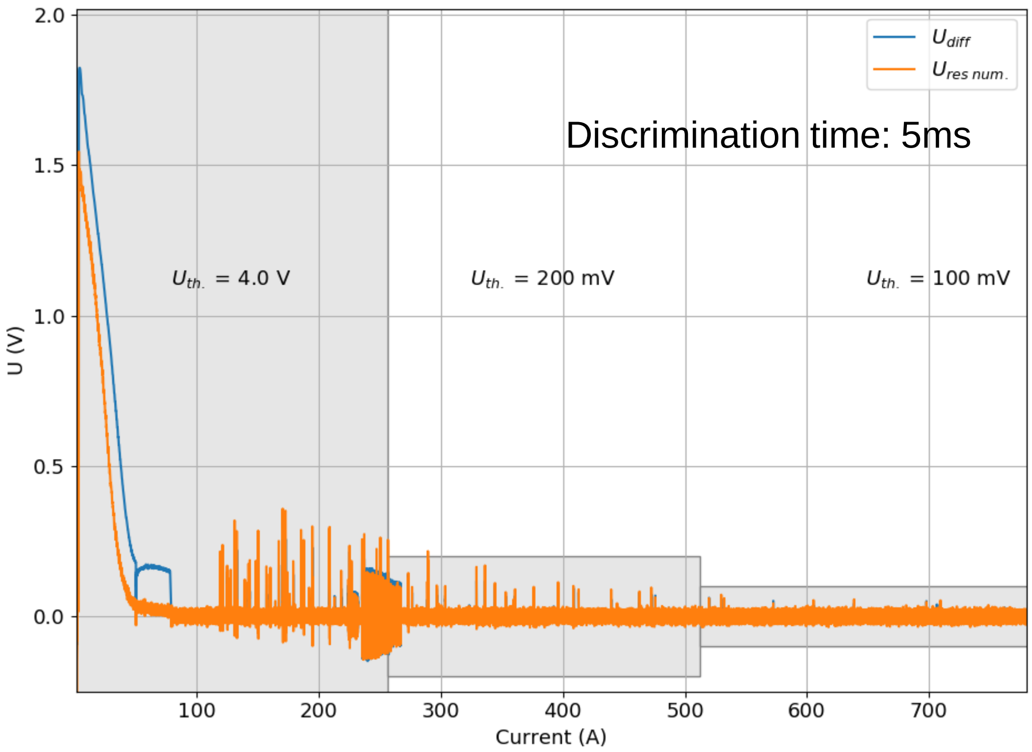




$$U_{res} = UDif_f + L\,\frac{di}{dt}$$

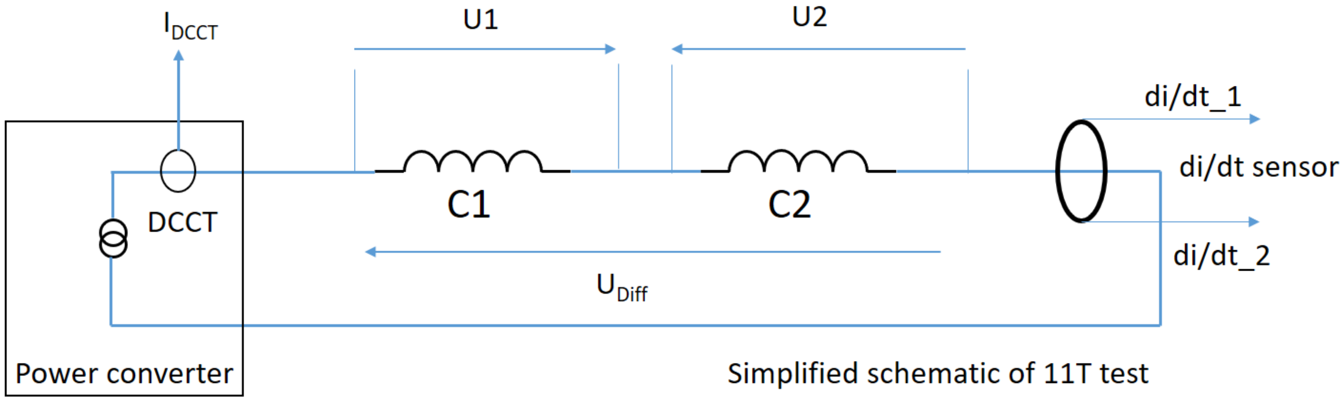
- Protection of a super conducting wiggler magnet made of Nb_3Sn with only 2 voltage taps
- Protection based on L*di/dt algorithm (numeric calculation and direct measurement of di/dt)

Operational experience: Wiggler



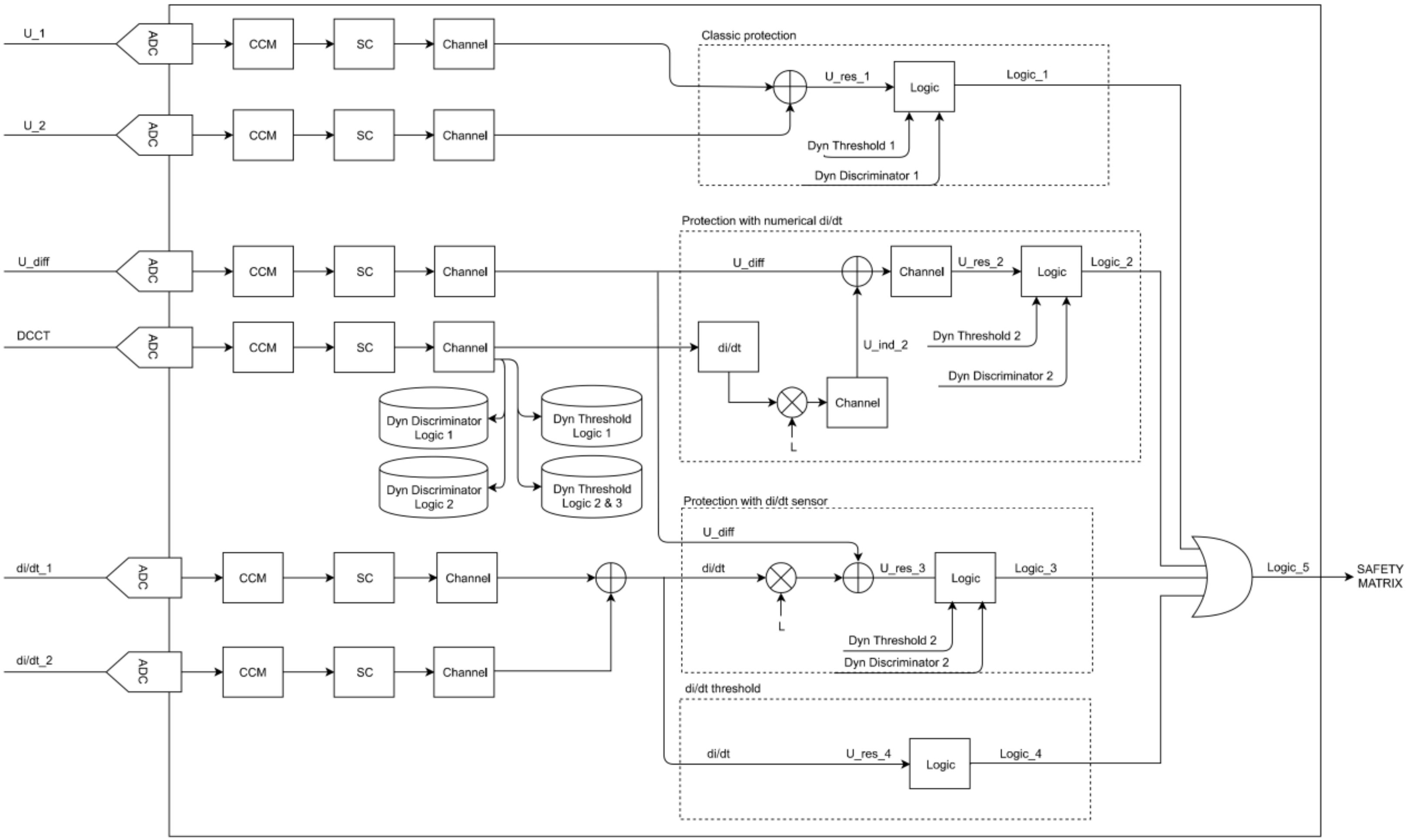
- Current dependent settings allowed to operate the circuit despite the presence of flux jumps and high di/dt during power converter start

Operational experience: 11T dipole prototype



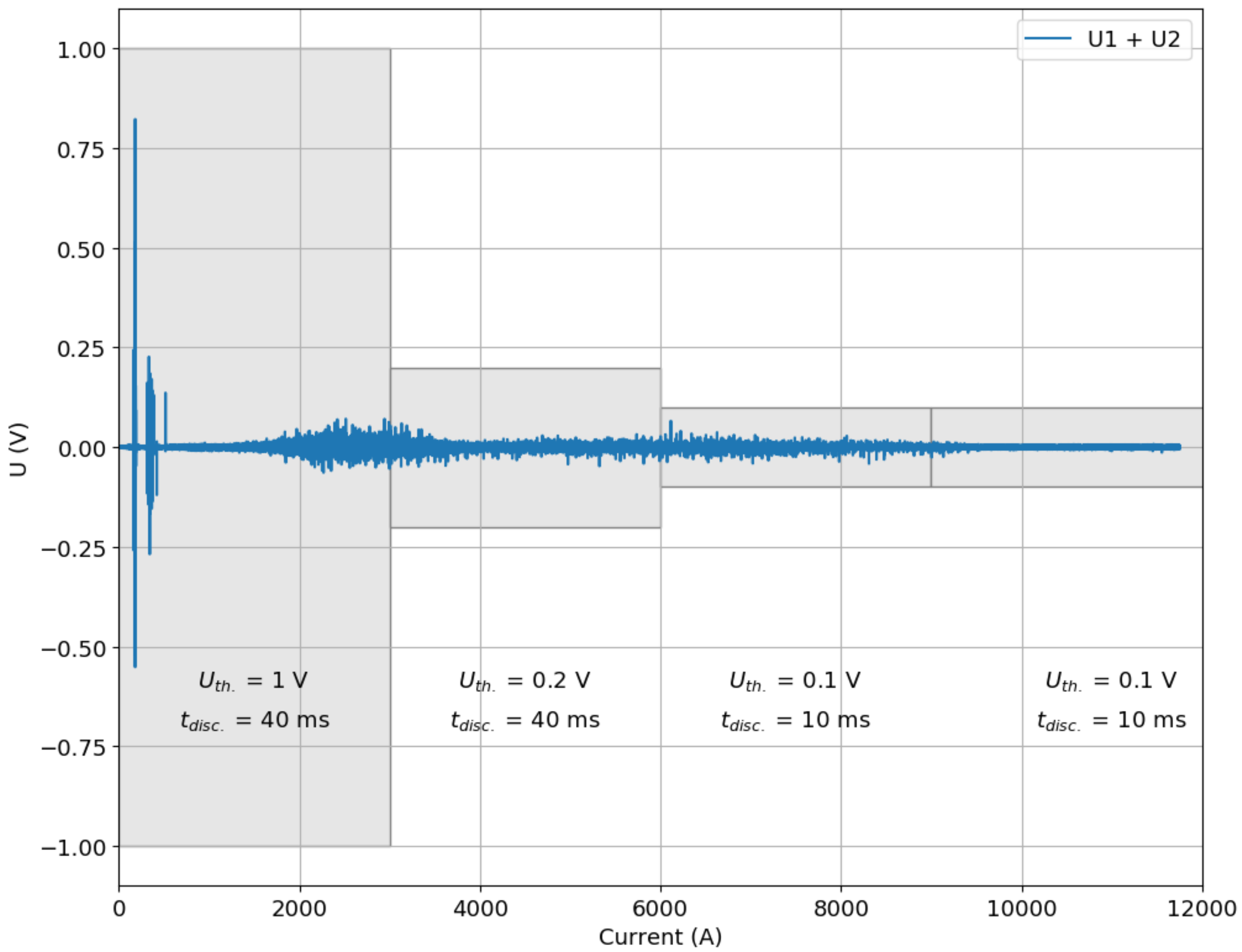
- Two coils of the prototype magnet in series forming one aperture → possibility of symmetric quenches
- In addition to comparison algorithm, a L*di/dt based algorithm (numeric and sensor) as well as a simple di/dt fixed threshold was used
- Due to flux jumps at lower currents, current dependent detection settings had been used

Operational experience: 11T dipole prototype



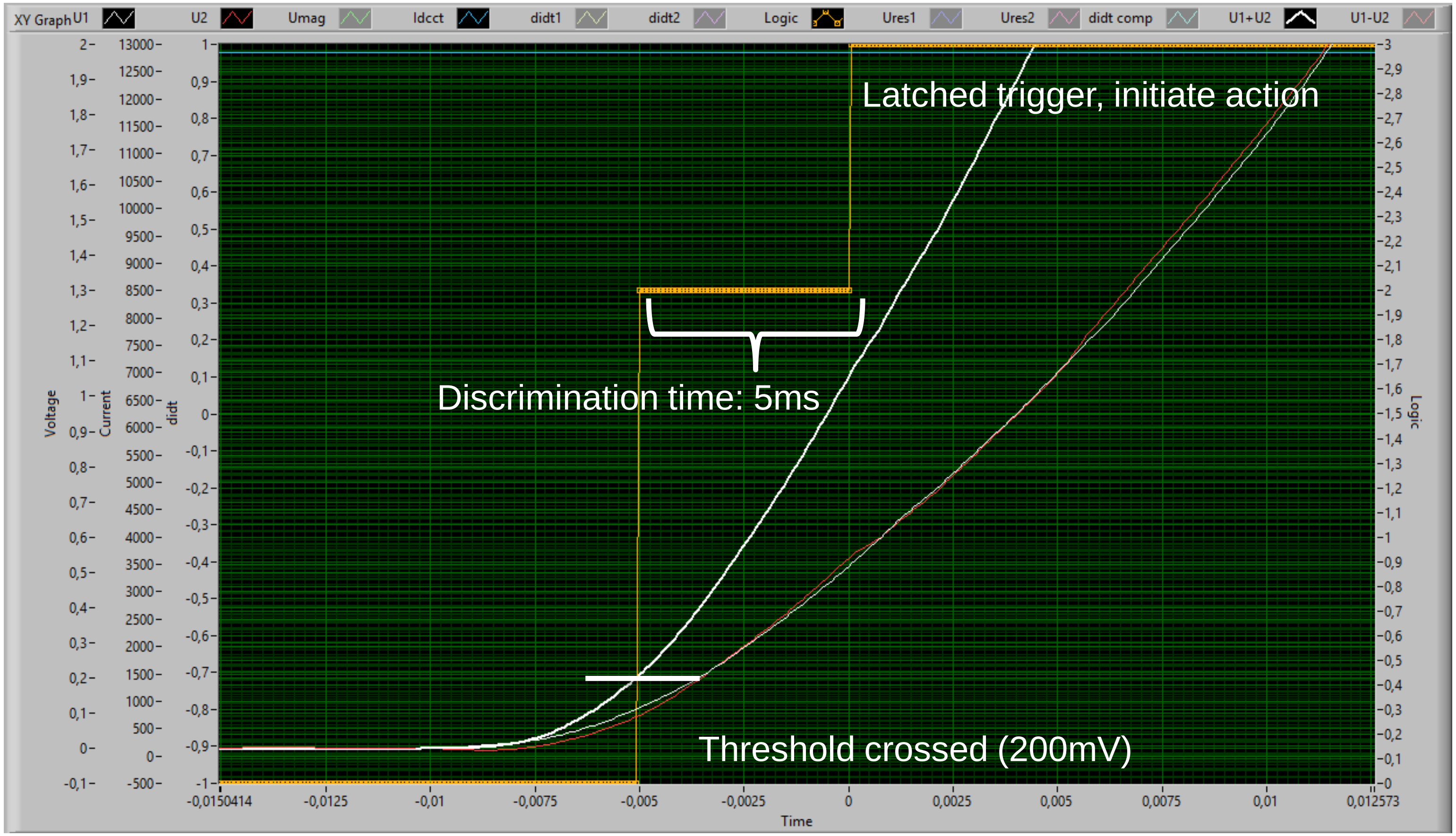
- 6 primary inputs, 4 logic blocks in parallel
- Dynamic thresholds and discrimination times

Operational experience: 11T dipole prototype



- Four different current dependent settings for threshold and discrimination time

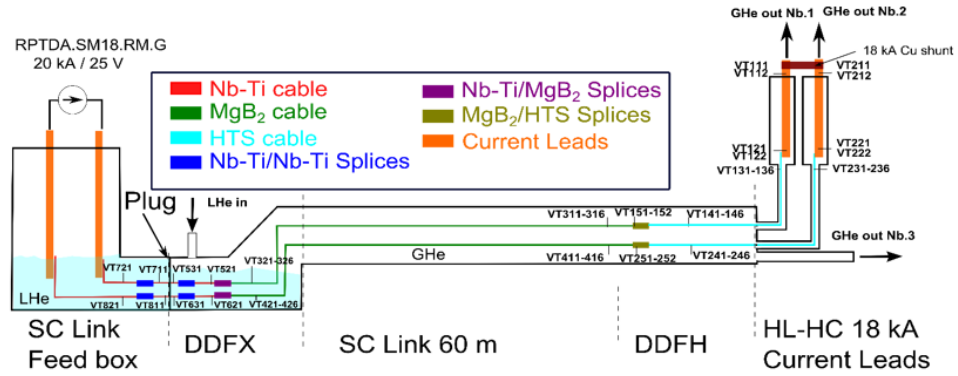
Operational experience: 11T dipole prototype



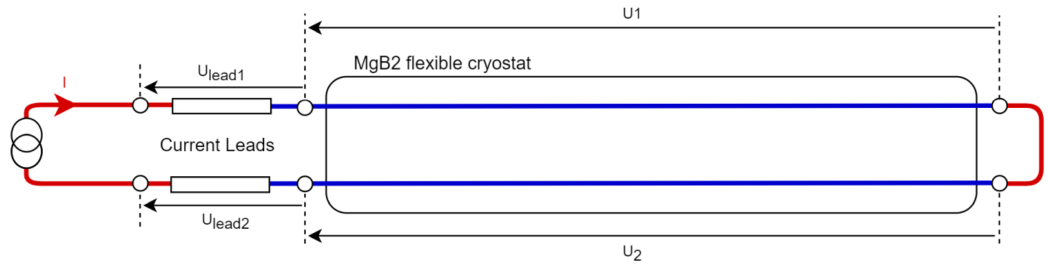
- Training quench at 12.8kA flat top

Operational experience: 18kA MgB_2 Link

Test setup:



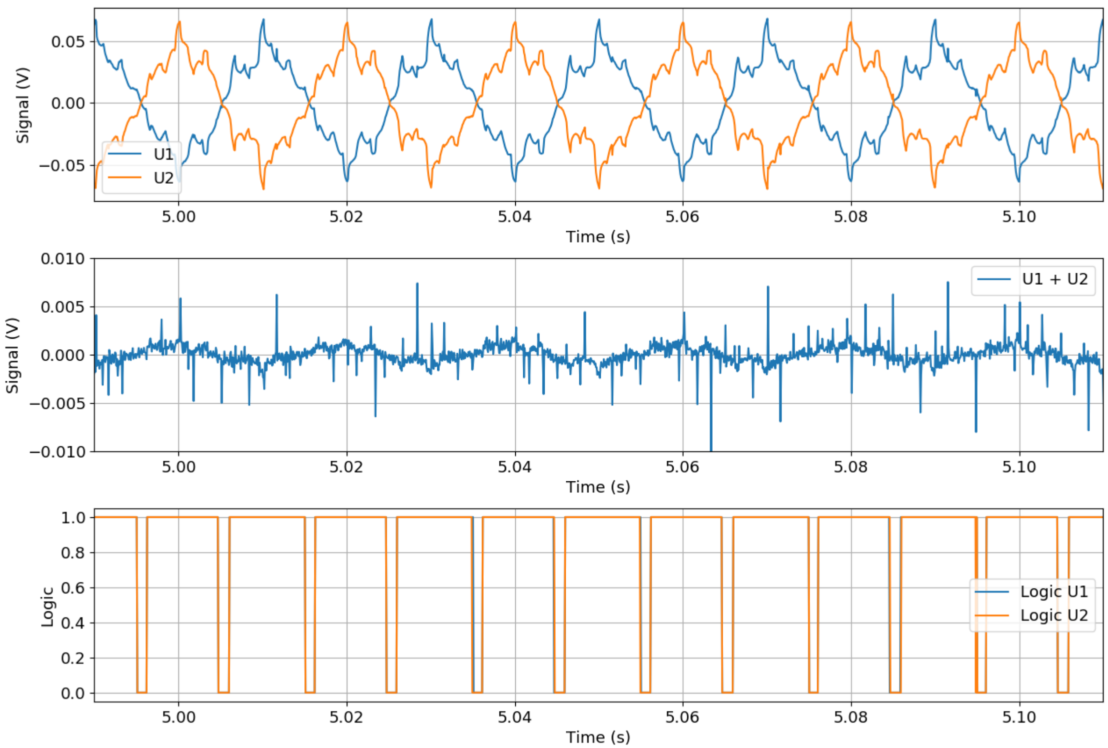
Electric circuit:



Protection: |U1 + U2| < Thres_comp_link (5mV, 50ms discrimination, no filters)
|U1| < Thres_abs_link, |U2| < Thres_abs_link
(10mV, 50ms discrimination, no filters)

|Ulead1 + Ulead2| < Thres_comp_lead (3mV, 8ms disc., no filters)
|Ulead1| < Thres_abs_lead, |Ulead2| < Thres_abs_lead
(6mV, 8ms discrimination, no filters)

Operational experience: 18kA MgB_2 link



- Discrimination filters very effective (50Hz noise 120mVpp present in the signals)
- No trip of QDS during whole test
- Good proof of concept for final Hi-Lumi QDS

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Outlook

- Development on UQDS will continue
- Deployment in test-benches
  (B163 & FAIR this year)
- Deployment in LHC in 2020 for 11T dipole
- Ethernet based communications controller development has to be finished
- Continue work on channels (double channel, special function channels)
- Full potential of FPGA platform to be exploited (use math blocks for FIR filters etc.)
- …

Conclusion

- A modular and flexible system with good performance and radiation tolerance had been designed
- Unit was used on several tests in CERN's magnet test facility protecting Nb_3Sn magnets, HTS current leads and a MgB_2 link
- First use in LHC will be 11T dipole quench detection
- Baseline system for most HiLumi quench detection systems (LS3)

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