CMOS Active Pixel Sensors

Luciano Musa (CERN)

Belle II VXD Open Workshop, CERN, July 8-10, 2019

ALICE "photographed" with ALPIDE , *courtesy of M. Mager*

Outline

① Prelude

- Development of CMOS APS for detection of single charged particles

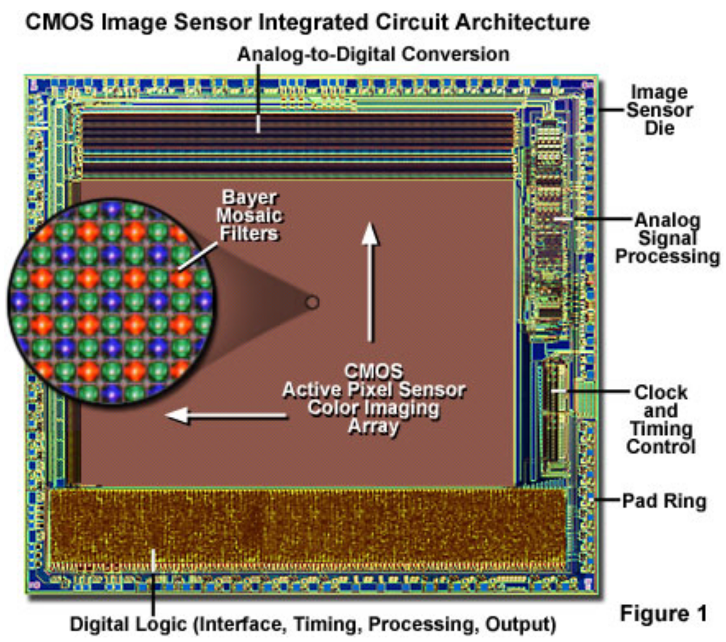
② First use of CMOS APS in HEP

- STAR Heavy Flavor Tracker, ALICE Inner Tracking System, …

③ Novel Developments

- Fully depleted sensors, wafer-scale integration, back-side processing

CMOS Image Sensor (CIS)



Source: Olympus (optical microscopy)

(Re)-invented in the early '90

- All-in-one: Electronic Camera On Chip
- Standard CMOS technology
  - ➪ lower production cost significantly
  - ➪ simpler integration of complex functionalities
- Very small pixels (today ~1μm, 40M pixel)
- Single low-supply and much lower power consumption
- Increased speed (column- or pixel- parallel processing)

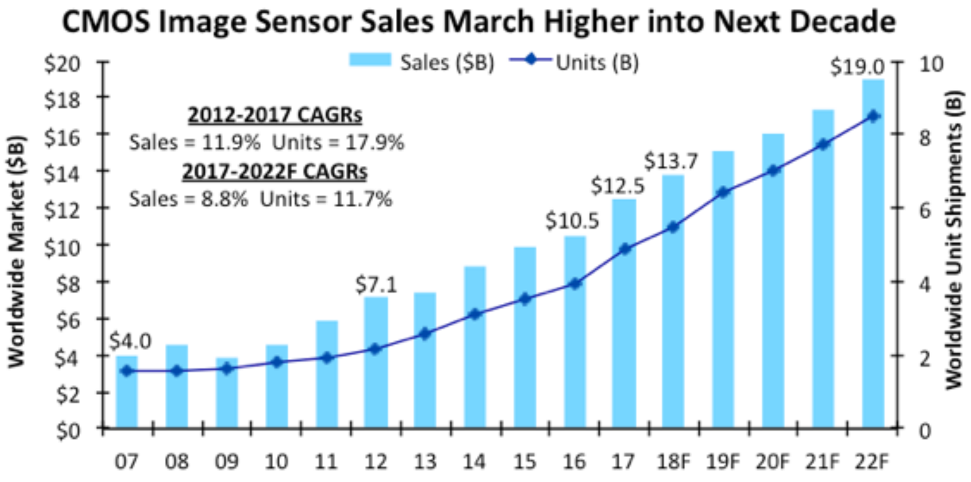
camera phones, vehicles, machine vision, human recognition and security systems

➪ drive CMOS image sensors development and sales

cellular camera phones account for 62% of the sales

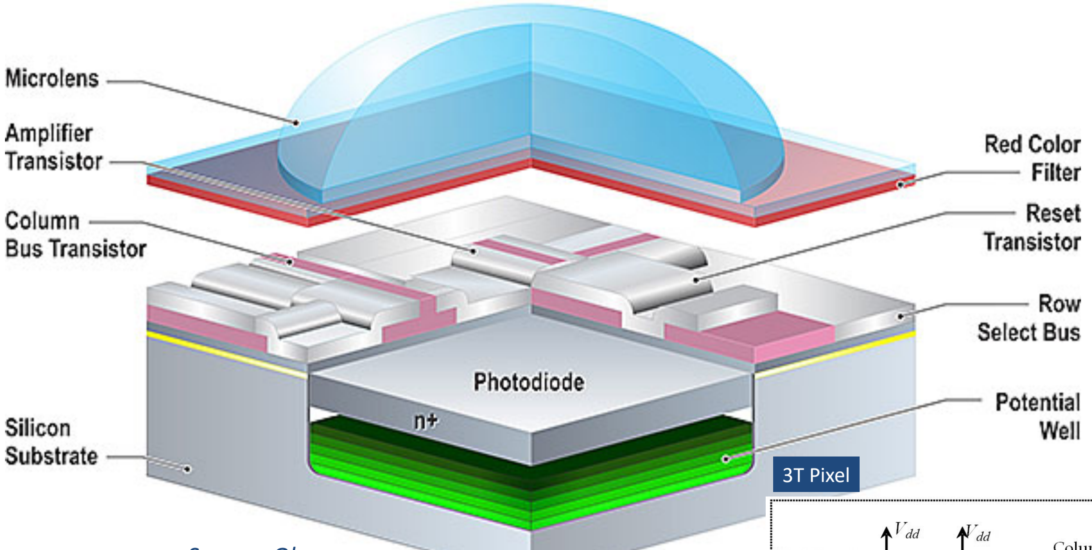
90% of the total image sensor sales in 2017

it was 74% in 2012, 54% in 2007

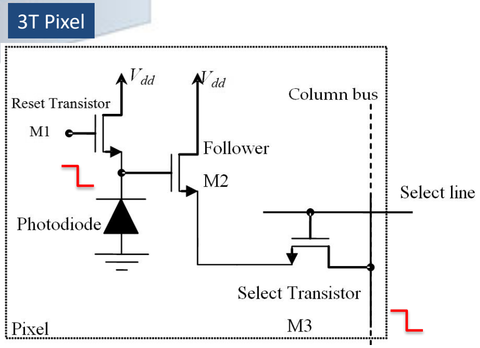


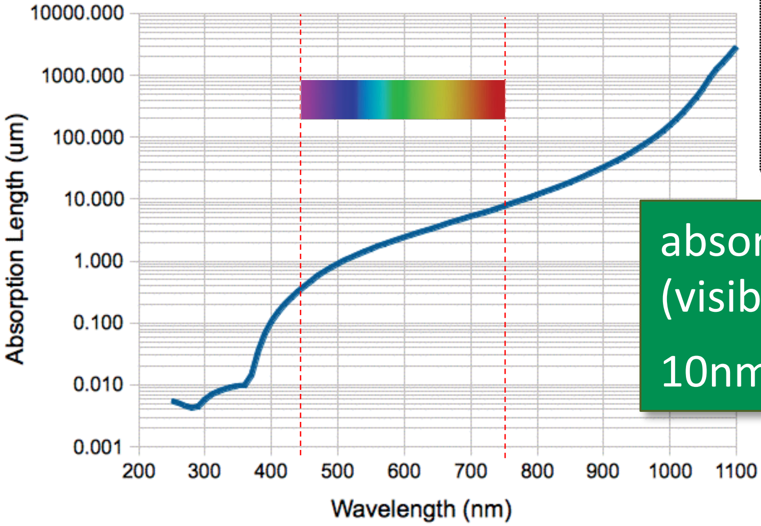
Source: IC Insights

Structure of a CIS Pixel



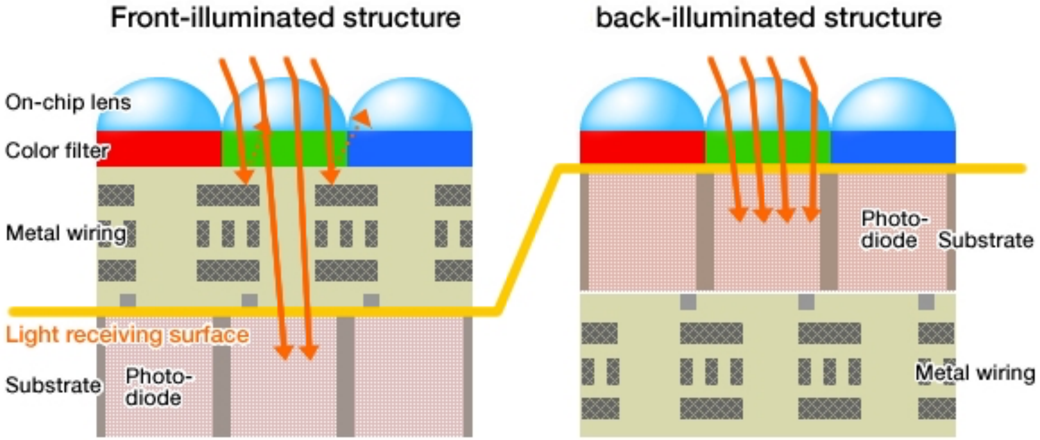
Source: Olympus

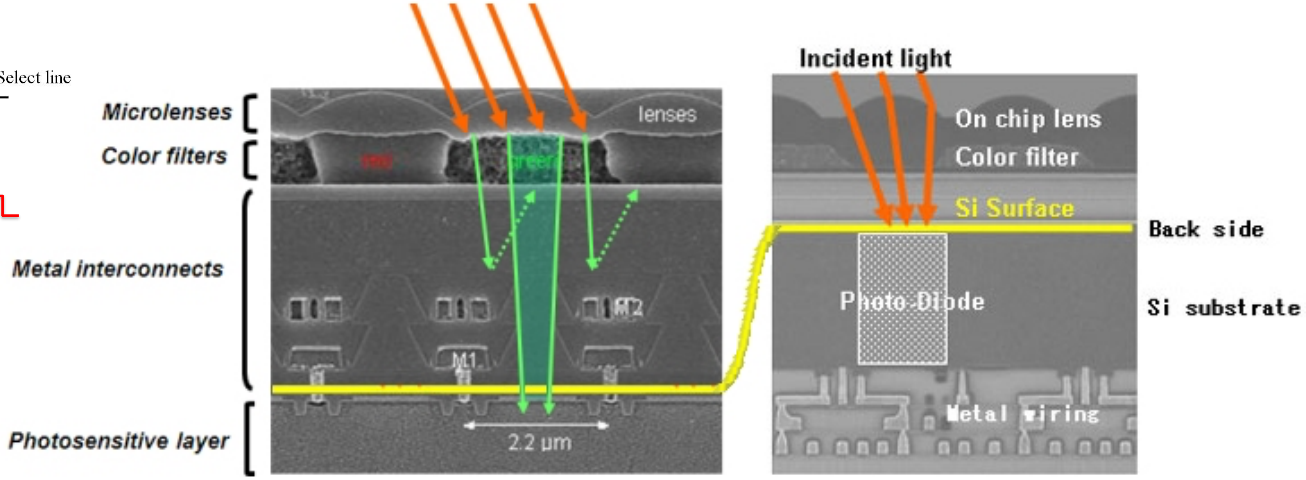




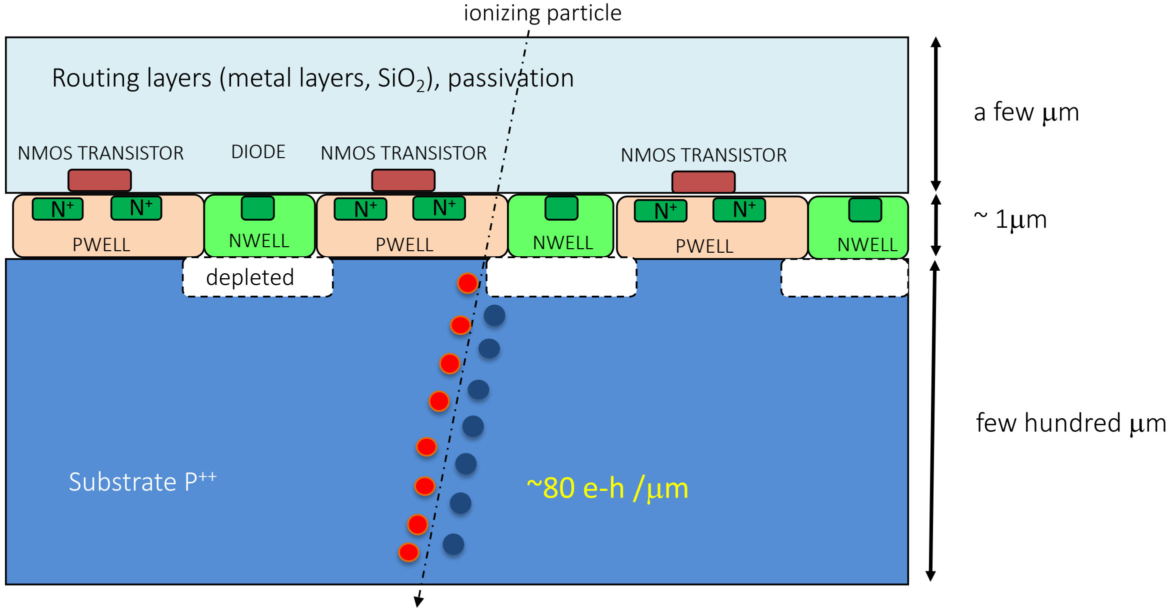
absorption depth (visible light):

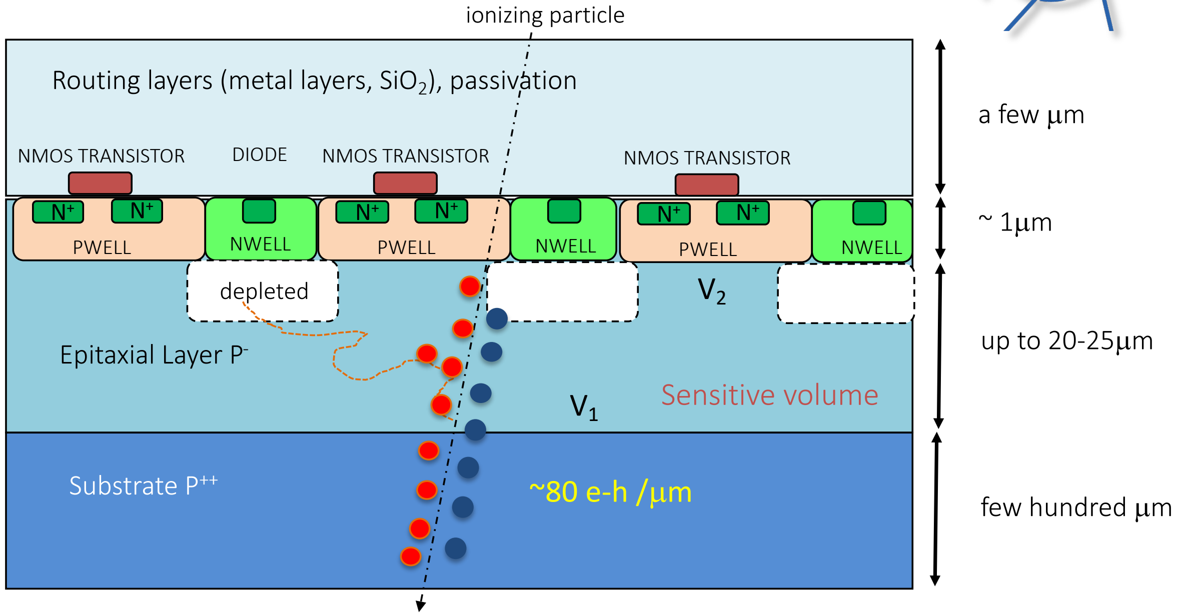
10nm – 5μm





Detection of charged particles in CMOS APS





In a standard CMOS image sensor (in the early days) the photodiode is implanted in low-resistivity silicon

Depletion region is shallow
charge collection efficiency is low

Moreover the detector element covers only a small fraction of the pixel area

… not suitable for the measurement of single charged particles

Use of an epitaxial layer with doping few order of magnitude smaller than one of the p++ substrate

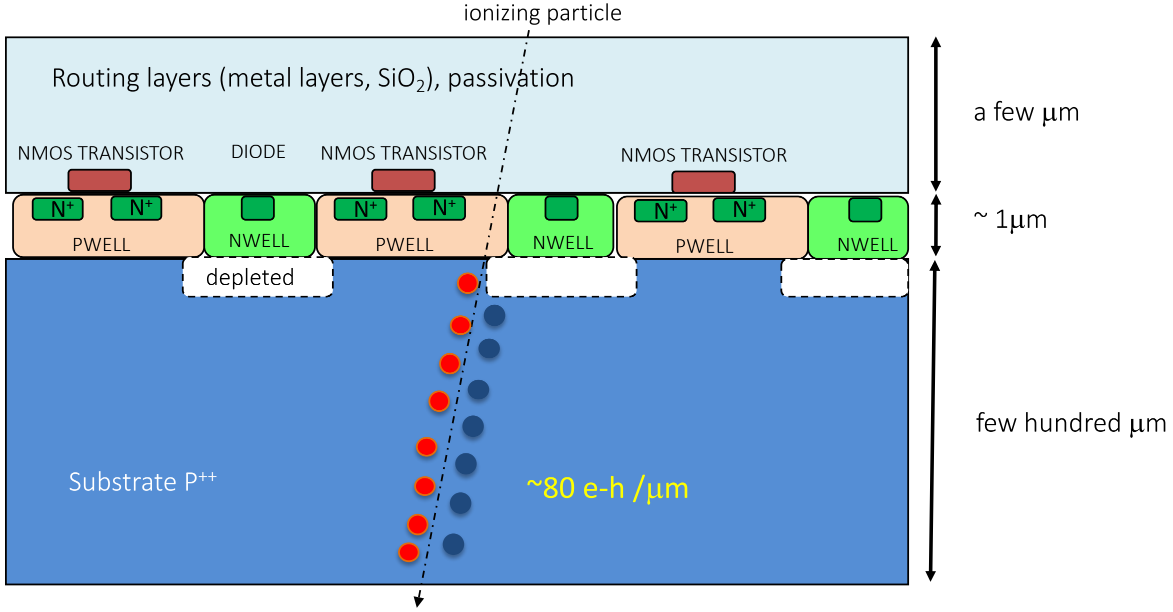
Potential barriers at boundaries

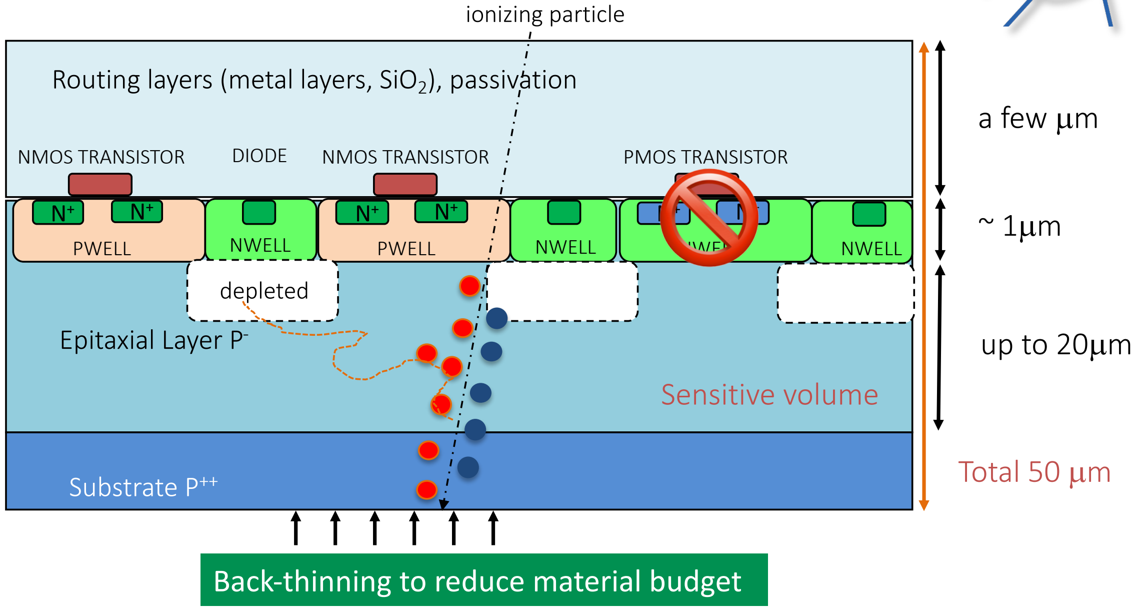
$$V_1 = \frac{kT}{q} ln \frac{N_{sub}}{N_{epi}} \qquad V_2 = \frac{kT}{q} ln \frac{N_{PWELL}}{N_{epi}}$$

which keep minority carriers confined in the epi-layer ....

… till they reach the depleted region underneath the NWELL

Detection of charged particles in CMOS APS





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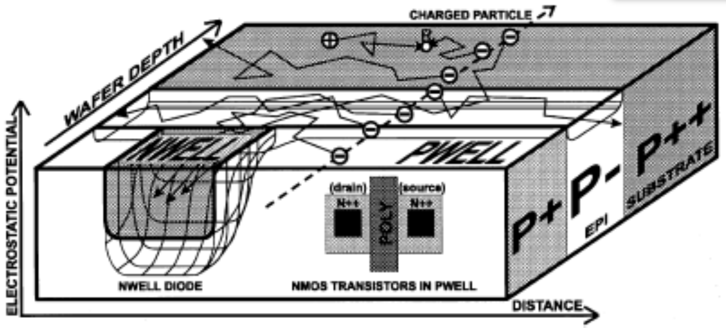
The inception of CMOS APS for charged particle tracking

A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology

R. Turchetta[a,*], J.D. Berst[a], B. Casadei[a], G. Claus[a], C. Colledani[a], W. Dulinski[a], Y. Hu[a], D. Husson[a], J.P. Le Normand[a], J.L. Riester[a], G. Deptuch[b,1], U. Goerlach[b], S. Higueret[b], M. Winter[b]

NIM A 458 (2001) 677-689



In a standard CMOS image sensor the photo diode was integrated in low-resistivity silicon

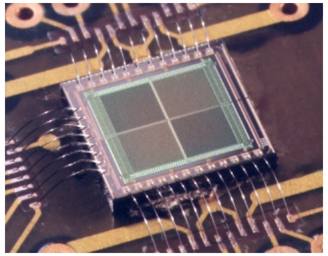
The charge collection diode is made of the junction between the NWELL and the P-type epitaxial layer

Integration of a sensor in 0.6μm CMOS process (twin P and N tubs)

- Implanted in lightly doped (P^-) epitaxial silicon layer
- Grown on top of the highly doped (P^{++}) substrate

courtesy of PICSEL group (IPHC)

Mimosa1 – 1999
AMS 0.6 μm

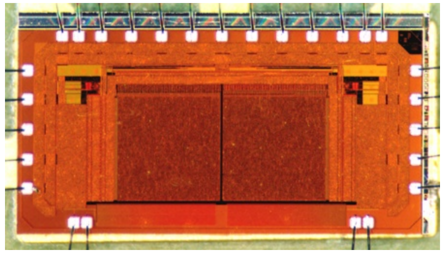


20μm pixel

Mimosa2 – 2000
MIETEC 0.35 μm

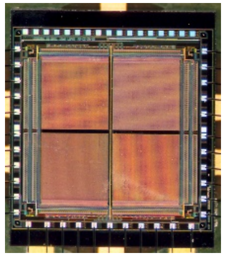
20μm pixel

Mimosa3 – 2001
IBM 0.25 μm



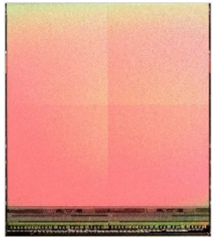
8μm pixel

Mimosa4 – 2001
AMS 0.35 μm



20 μm pixel

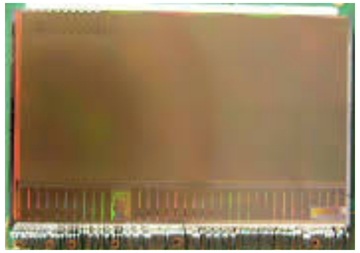
Mimosa5 – 2001
AMS 0.6 μm



17 μm pixel

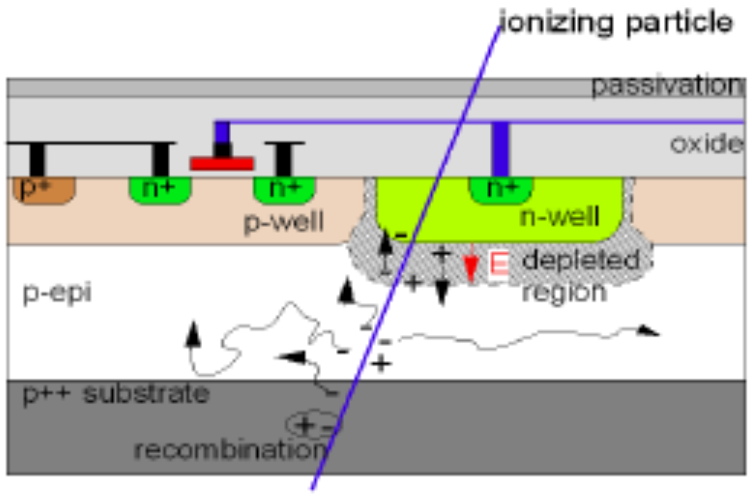
. . .

Mimosa26 – 2008
AMS 0.35 μm



18.4 μm pixel

Development of CMOS APS – MIMOSA series



courtesy of PICSEL group (IPHC)

p-type crystalline epitaxial layer hosts n-well charge collector

Signal is generated in a high-resistivity (~ 1 kΩcm) epi-layer ~20μm thick

Early versions with thin and lower resistivity epi-layer

epi-layer not fully depleted ⇨ charge collection (mostly) by diffusion
typical charge collection time < 100ns

R&D mostly with AMS 0.6μm/0.35μm and TJ 0.18μm technologies
(but exploratory also with MIETEC 0.35, IBM 0.25, TSMC 0.25, STM 025, XFAB 0.6/0.35)

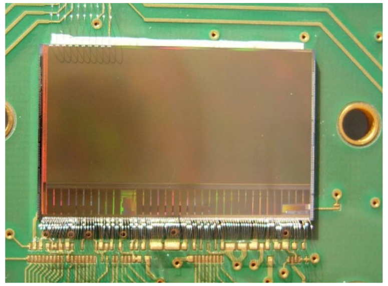
Sensitive to radiation induced displacement damage in the epi layer
⇨ ok for applications with up to ~ 10^{12} 1MeV N_{eq}/cm^2

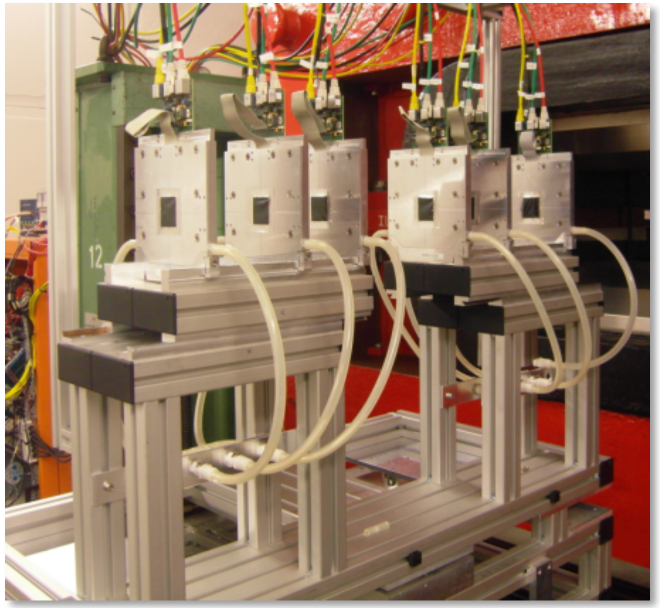
Only NMOS transistors in the active area

⇨ 2T or 3T in-pixel circuit, rolling shutter architecture for matrix analogue readout

Mimosa26 – 2008 (AMS 0.35 µm)

- 18.4 µm pixel pitch 576 x 1152 pixels
- First MAPS with integrated zero-suppression
- Used for several applications, also for EUDEET telescope

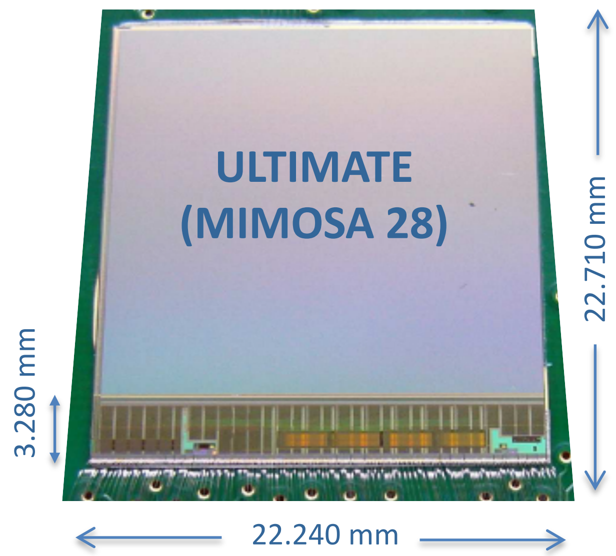




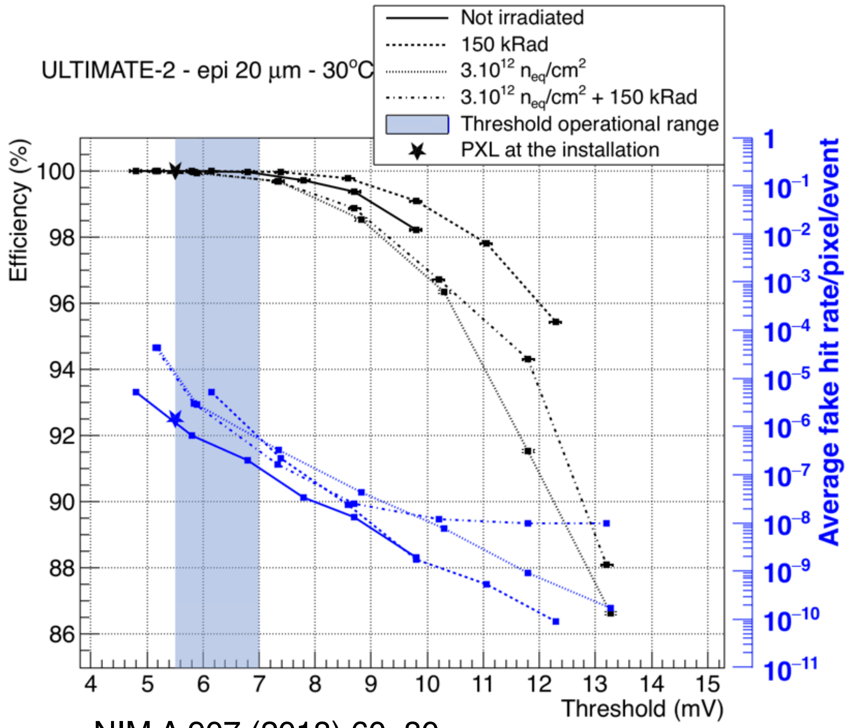
courtesy of PICSEL group (IPHC)

Ultimate (MIMOSA-28) for STAR HFT - First use of CMOS APS in HEP

MIMOSA-28, 2011, AMS 0.35μm

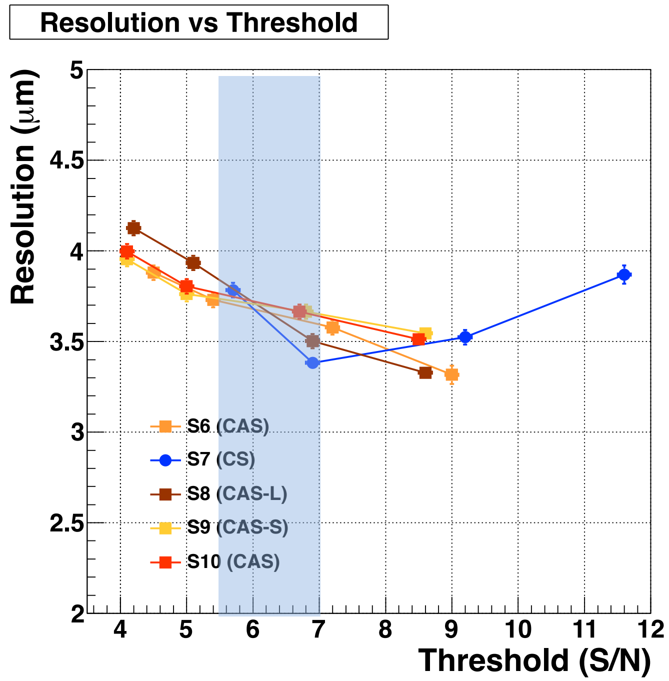


courtesy of PICSEL group (IPHC)



NIM A 907 (2018) 60–80

ENC ≤ 15 e^- at 30-35 °C



Single point resolution ≈ 3.7μm

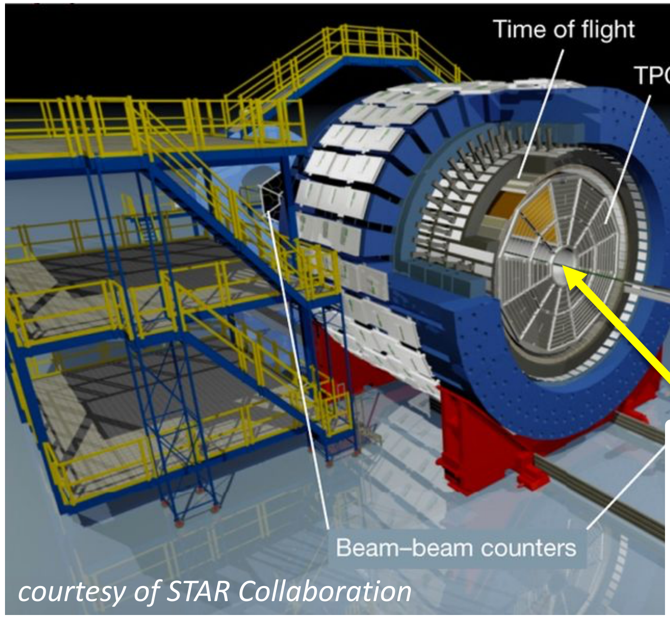
Matrix

- pixel size: 20.7 μm x 20.7 μm
- 928 rows x 960 columns ~ 1M pixel
- in-pixel circuit: 2T structure
- Correlated Double Sampling

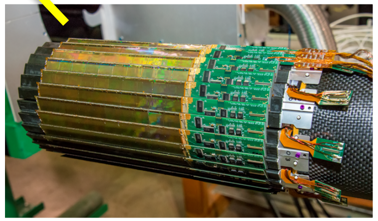
Periphery

- end-of-column discriminators and zero suppression
- memory (1500 words), 2 LVDS output @160 MHz
- 185.6 μs integration time
- ~160 mW/cm² power dissipation

First use of CMOS APS in HEP - STAR Pixel Detector



courtesy of STAR Collaboration



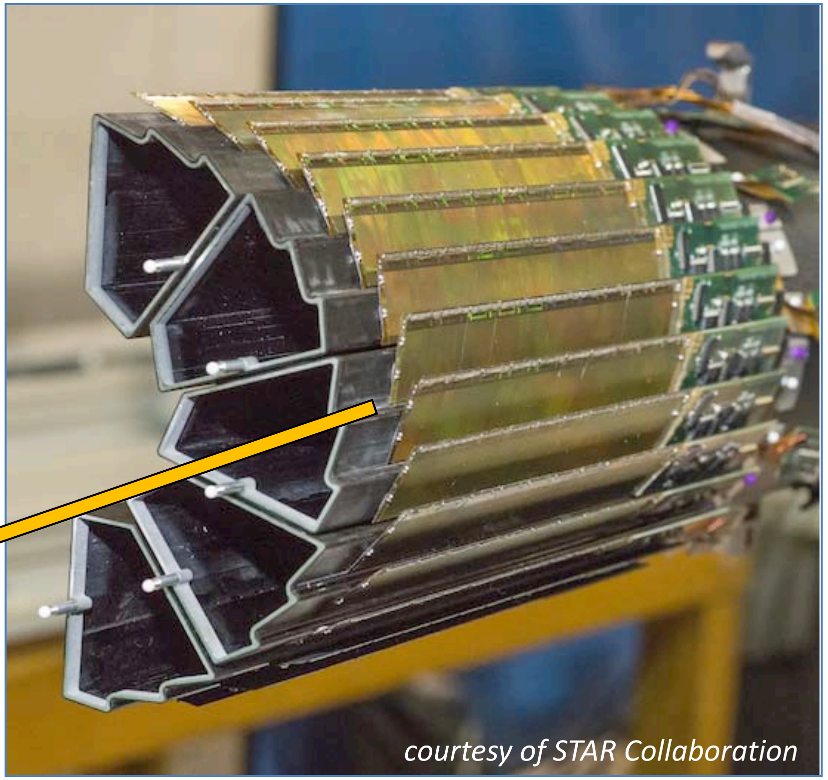
356 M pixels on ~0.16 m^2 of Silicon

Full detector Jan 2014, Physics Runs in 2015-216

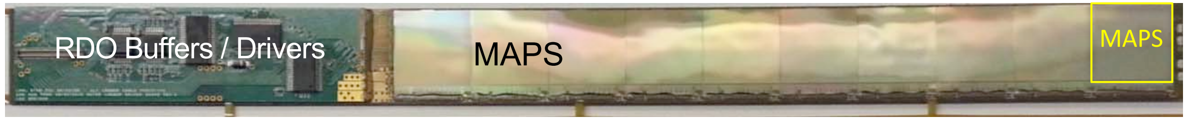
Radiation length (1st layer): x/X_0 = 0.39% (Al conductor cable)

- 2 layers (2.8cm and 8cm radii)
- 10 sectors total (in 2 halves)
- 4 ladders/sector

20 to 90 kRad / year
2*10^{11} to 10^{12} 1MeV n_{eq}/cm^2


courtesy of STAR Collaboration

Ladder with 10 MAPS sensors (~ 2×2 cm^2 each)



courtesy of STAR Collaboration

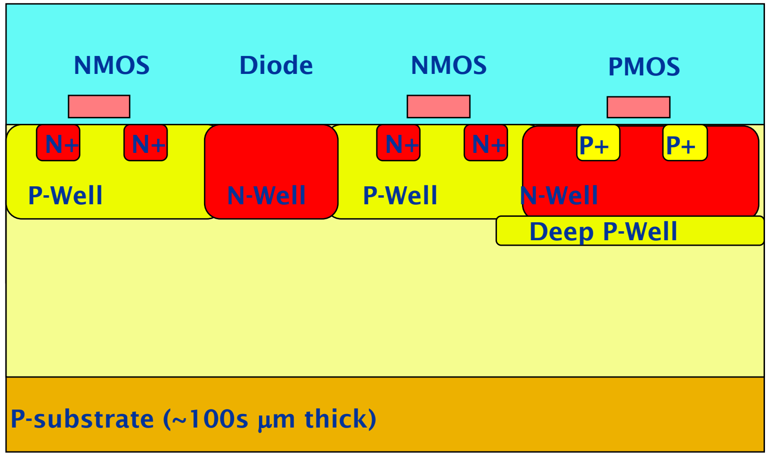
2-layer kapton flex cable with Al traces

"CMOS Sensor Development in Strasbourg"
J. Baudot, Tuesday

The INMAPS Process – STFC development in collaboration with TJ

"Monolithic Active Pixel Sensors (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixel"

R. Turchetta et al. , Sensors 2008, 8, 5336-5351; DOI: 10.3390/s8095336

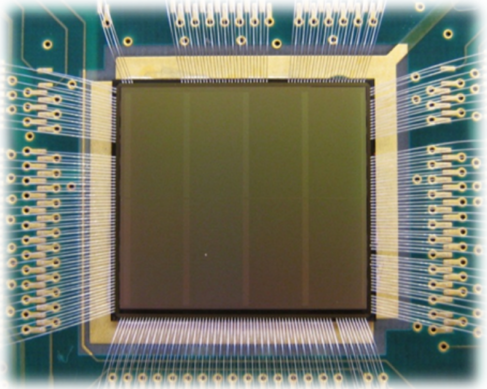


Standard CMOS with additional deep P-well implant Quadruple well technology

100% efficiency and CMOS electronics in the pixel

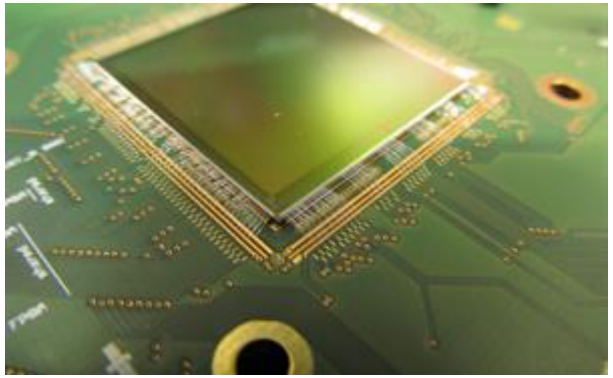
New generation of CMOS APS for scientific applications with complex CMOS circuitry inside the pixel (TowerJazz CIS 180nm)

TPAC - for ILC ECAL (CALICE)



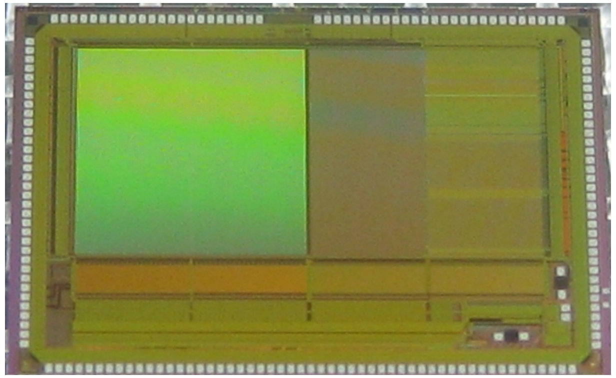
50μm pixel

PIMMS – TOF mass spectroscopy



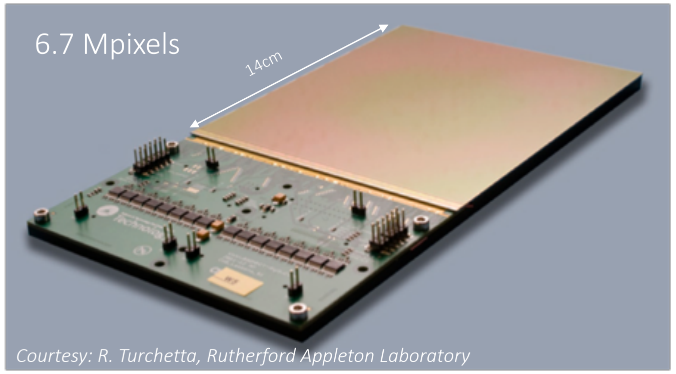
70μm pixel

CHERWELL – Calorimetry/Tracking



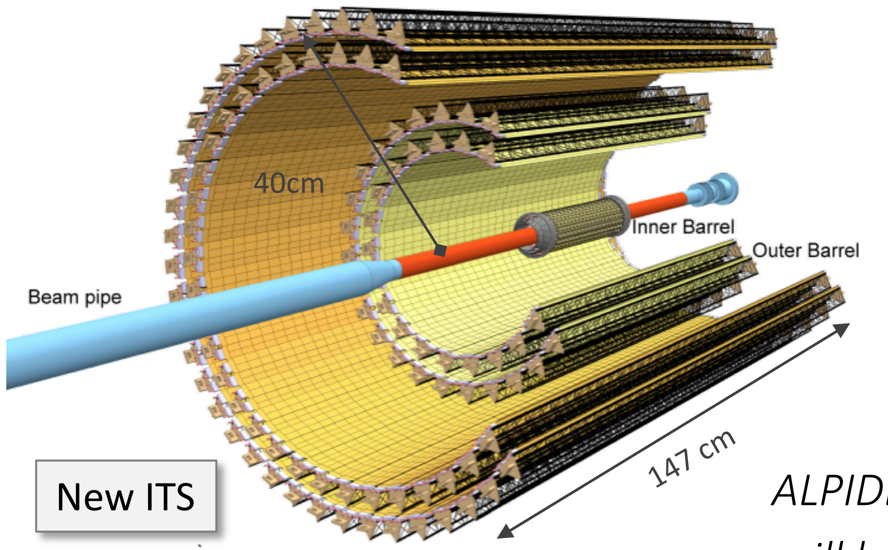
48 μm x 96 μm pixel

LASSENA – medical X-ray imaging



50μm pixel, waferscale (14cm x 14cm)

New ALICE ITS: closer to IP, thinner, higher position resolution



New ITS

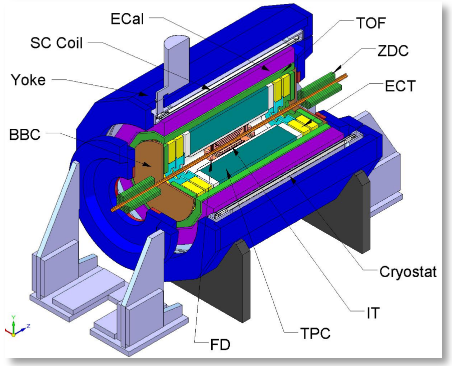
$1.5 \leq \eta \leq 1.5$

7 layers, 12.5 Gpixels covering $10m^2$, with $5\mu m$ position resolution

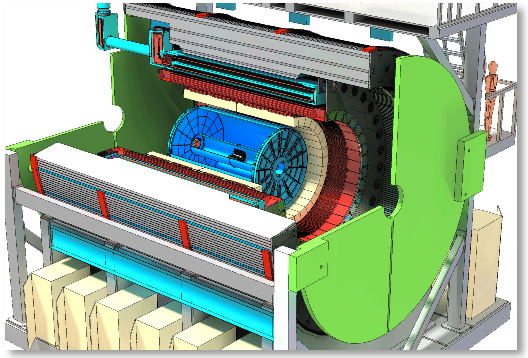
Closer to IP:	39mm ➡ 22mm
Thinner:	~1.14% ➡ ~ 0.3% (3 inner layers)
Smaller pixels:	$50\mu m \times 425\mu m$ ➡ $27\mu m \times 29\mu m$

ALPIDE (ALICE Pixel Detector) - Developed for the ALICE upgrade (ITS and MFT) will be used for several other HEP detectors and other applications

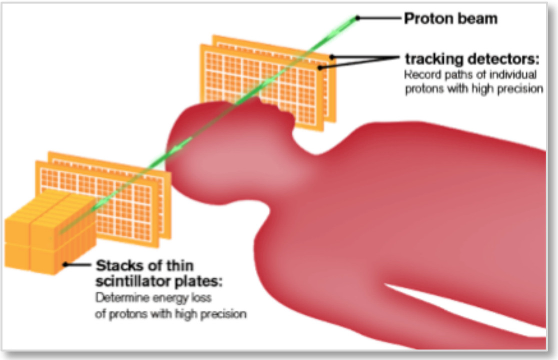
NICA MPD (@JINR)



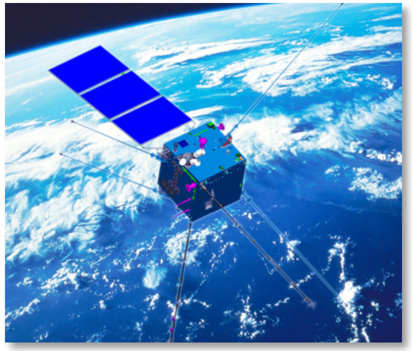
sPHENIX (BNL)



proton CT (tracking)



CSES – HEPD2

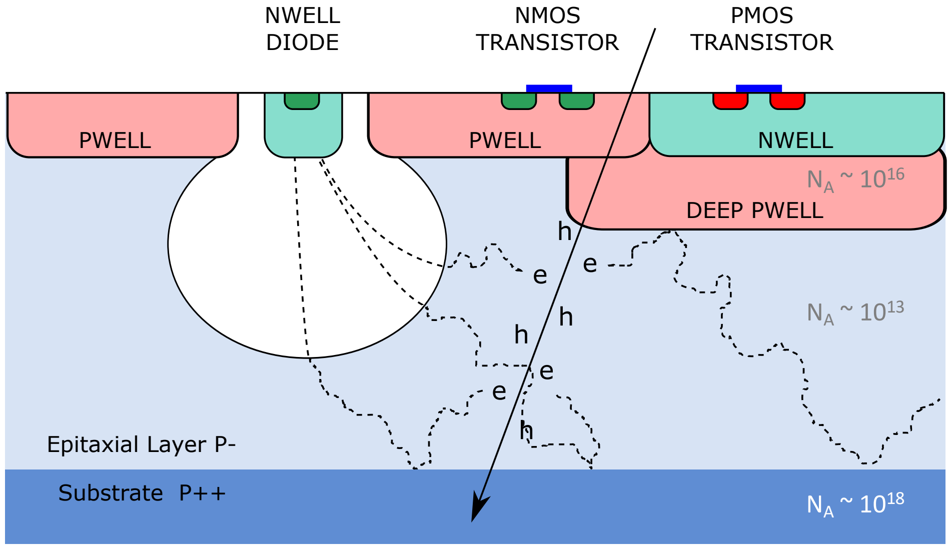


...

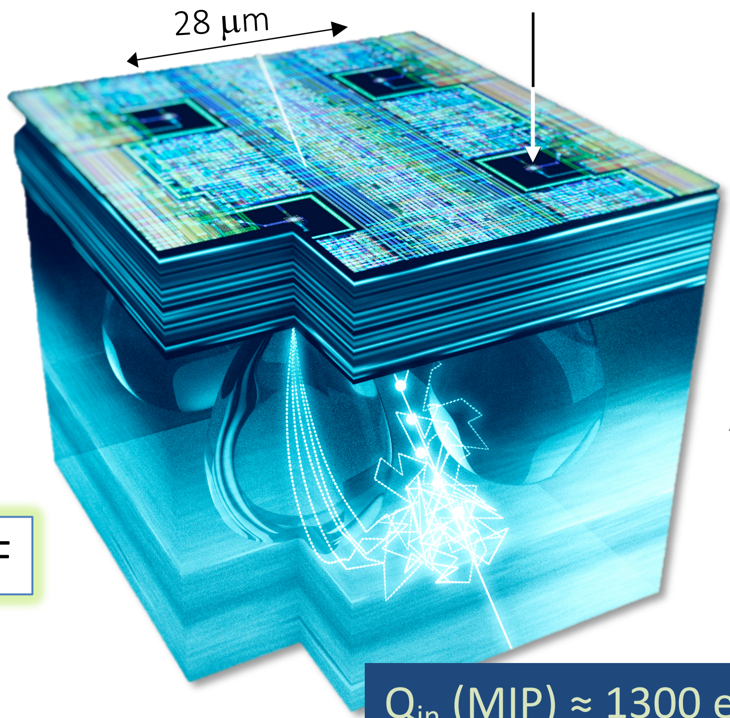
ALPIDE Sensor

CCNU, CERN, INFN (Torino & Cagliari), IPHC, IRFU, NIKHEF, Yonsei

CMOS Pixel Sensor using TJ 0.18μm CMOS Imaging Process



pixel capacitance ≈5 fF (@ V_{bb} = -3 V)



2 x 2 pixel volume

$C_{in} \approx 5$ fF

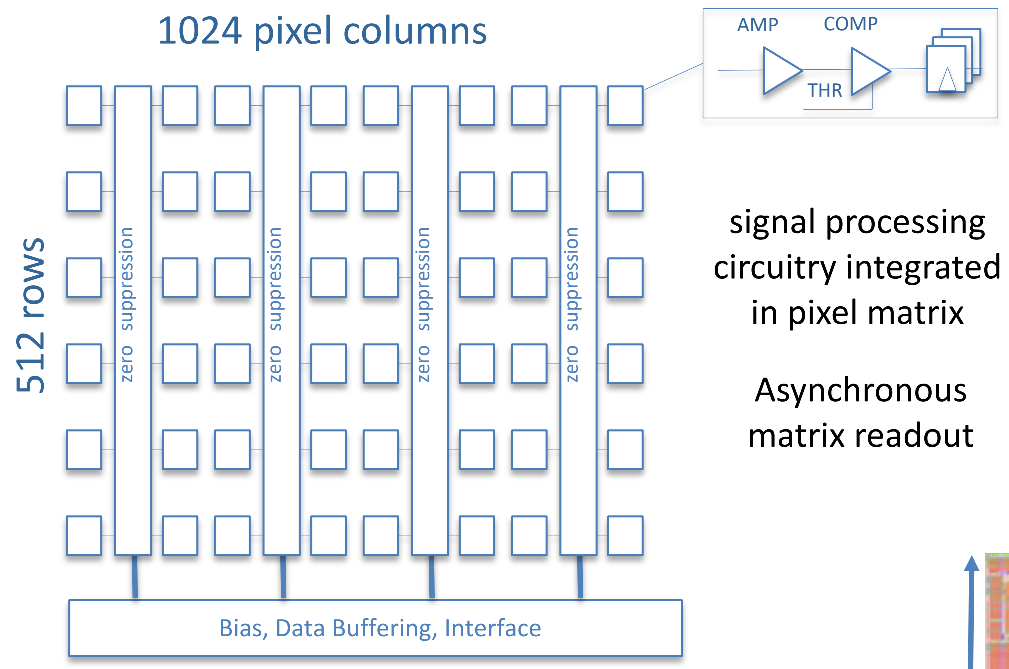
Artistic view of a SEM picture of ALPIDE cross section

Q_{in} (MIP) ≈ 1300 e ⇨ V ≈ 40mV

- High-resistivity (> 1kΩ cm) p-type epitaxial layer (25μm) on p-type substrate
- Small n-well diode (2 μm diameter), ~100 times smaller than pixel => low capacitance (~fF)
- Reverse bias voltage (-6V < V_{BB} < 0V) to substrate (contact from the top) to increase depletion zone around NWELL collection diode
- Deep PWELL shields NWELL of PMOS transistors

➔ full CMOS circuitry within active area

ALICE PIxel DEtector (ALPIDE)



signal processing circuitry integrated in pixel matrix

Asynchronous matrix readout

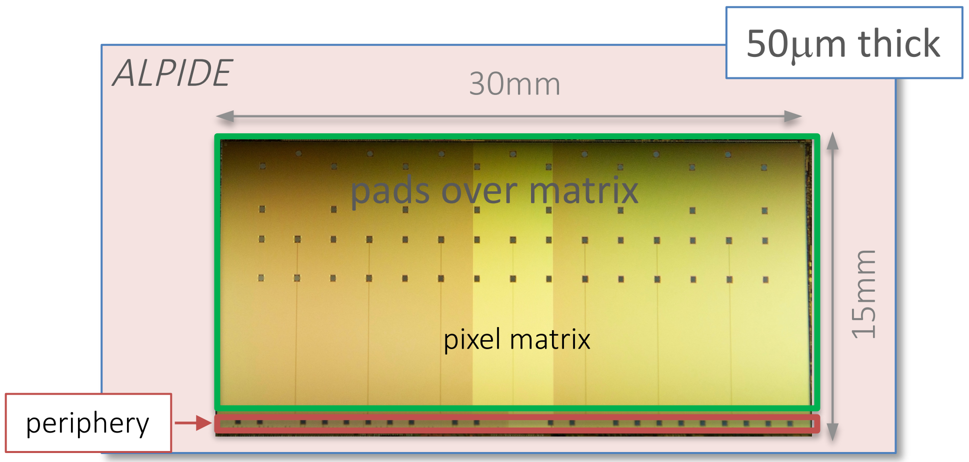
$130{,}000$ pixels / cm^2 $27\times29\times25\ \mu m^3$

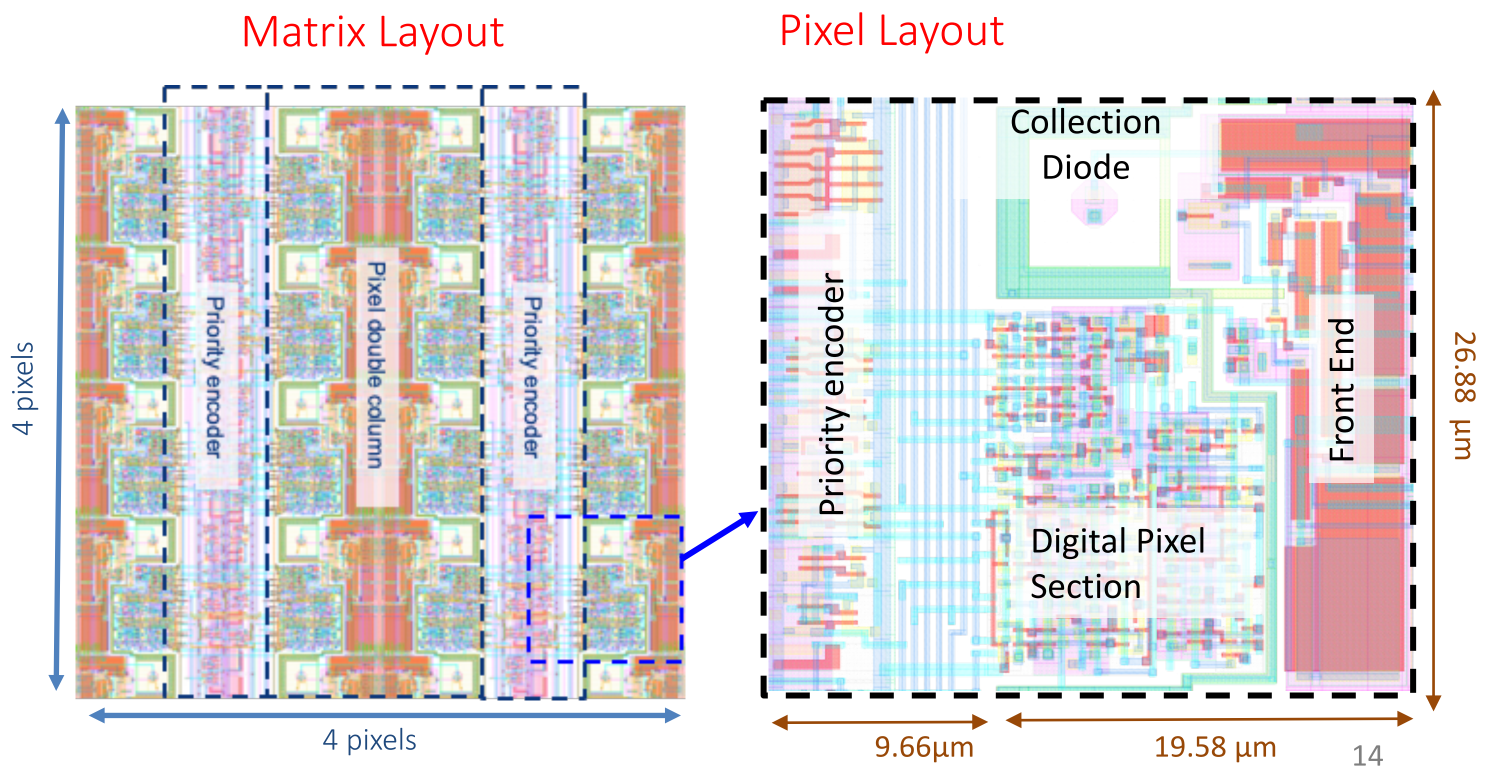
charge collection time <30ns (V_{bb} = -3V)

Max particle rate: > 100 MHz/cm^2

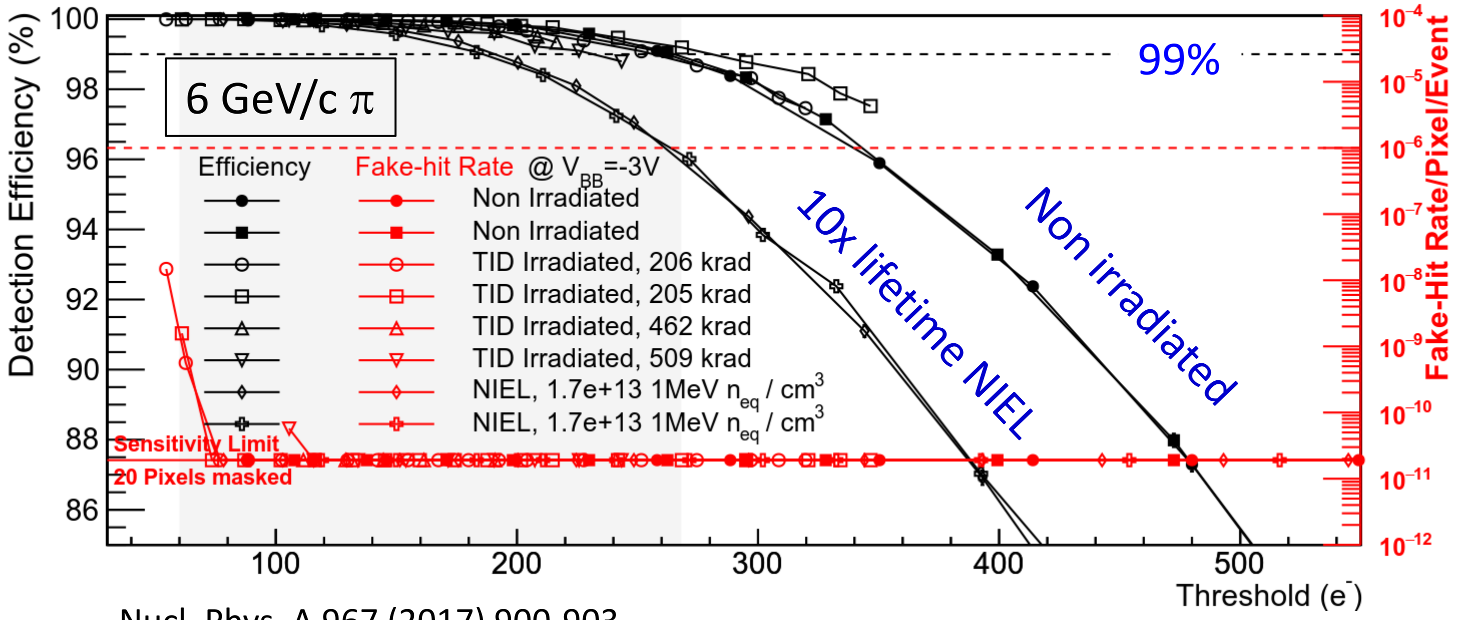
fake-hit rate: < 1 Hz/ cm^2

power : < 40mW/cm^2 (only 6.2 mW/cm^2 in the matrix)





ALICE PIxel DEtector (ALPIDE)

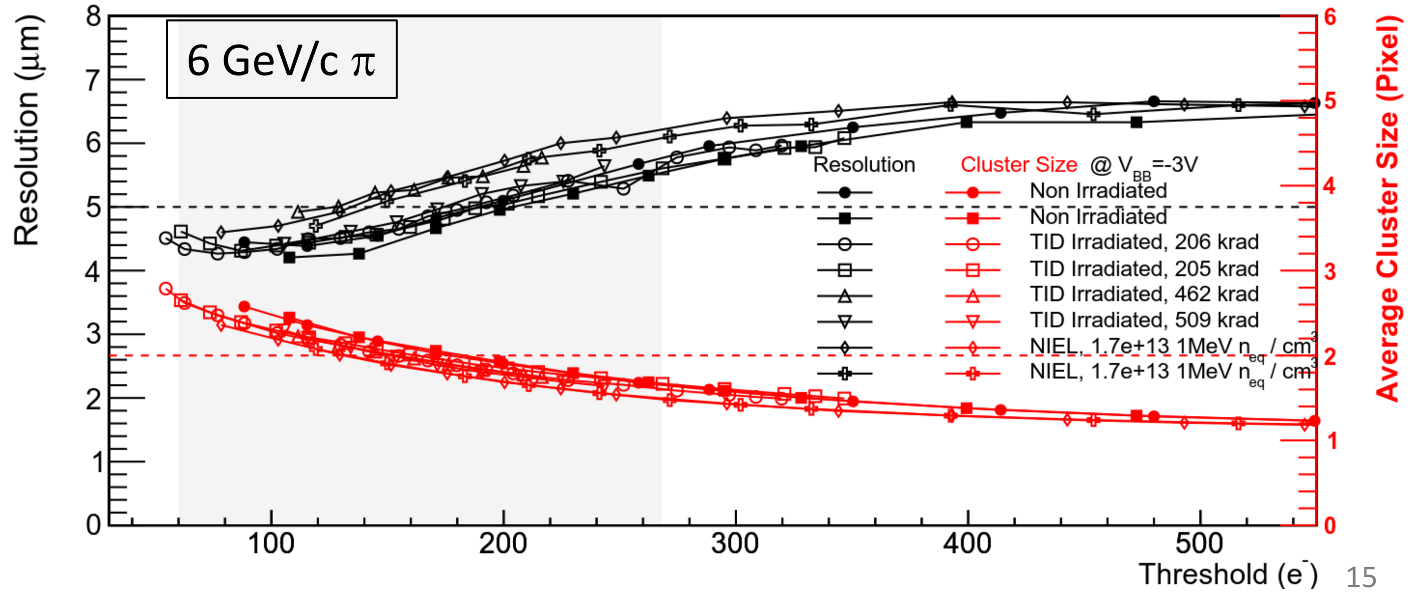


Nucl. Phys. A 967 (2017) 900-903

Large operational margin with only 10 masked pixels (0.002%), fake-hit rate $< 2 \times 10^{-11}$ pixel/event

Non irradiated and TID/NIEL chips similar performance

Nucl. Phys. A 967 (2017) 900-903

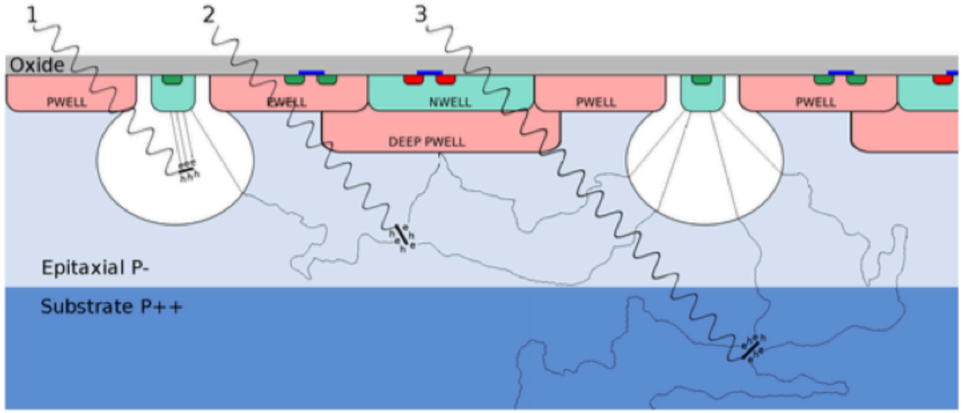


5 μm resolution @ 200 e^- threshold

Chip-to-chip negligible fluctuations

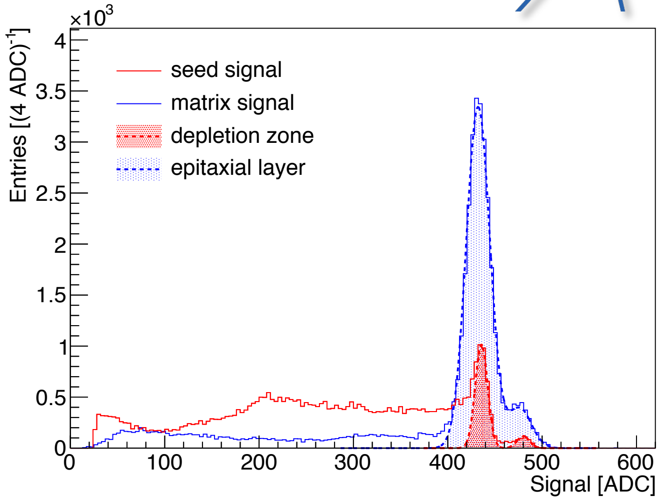
"ALPIDE Experience and developments"
G. Aglieri Rinella, Tuesday

X-ray detection in a sensor with TJ std process



^{55}Fe: two X-Ray emission modes:

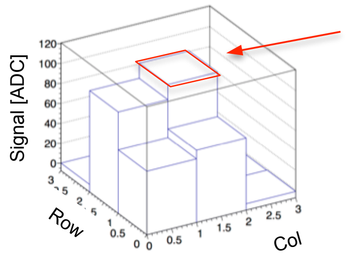
1. K-α: 5.9keV (1640 e/h in Si), rel. freq.: 89.5%, attenuation length in Si: 29μm
2. K-β: 6.5keV (1800 e/h in Si), rel. freq.: 10.5%, attenuation length in Si: 37μm

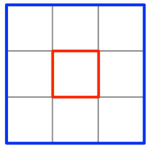


For X-ray absorption in sensors fabricated with the std process, three cases can be defined

J. Van Hoorne NSS 2016

1. Absorption in depleted volume: charge collected by drift, no charge sharing, single pixel cluster
   - These events populate the calibration peak in the signal histogram
   - Charge collection time expected to be <1ns





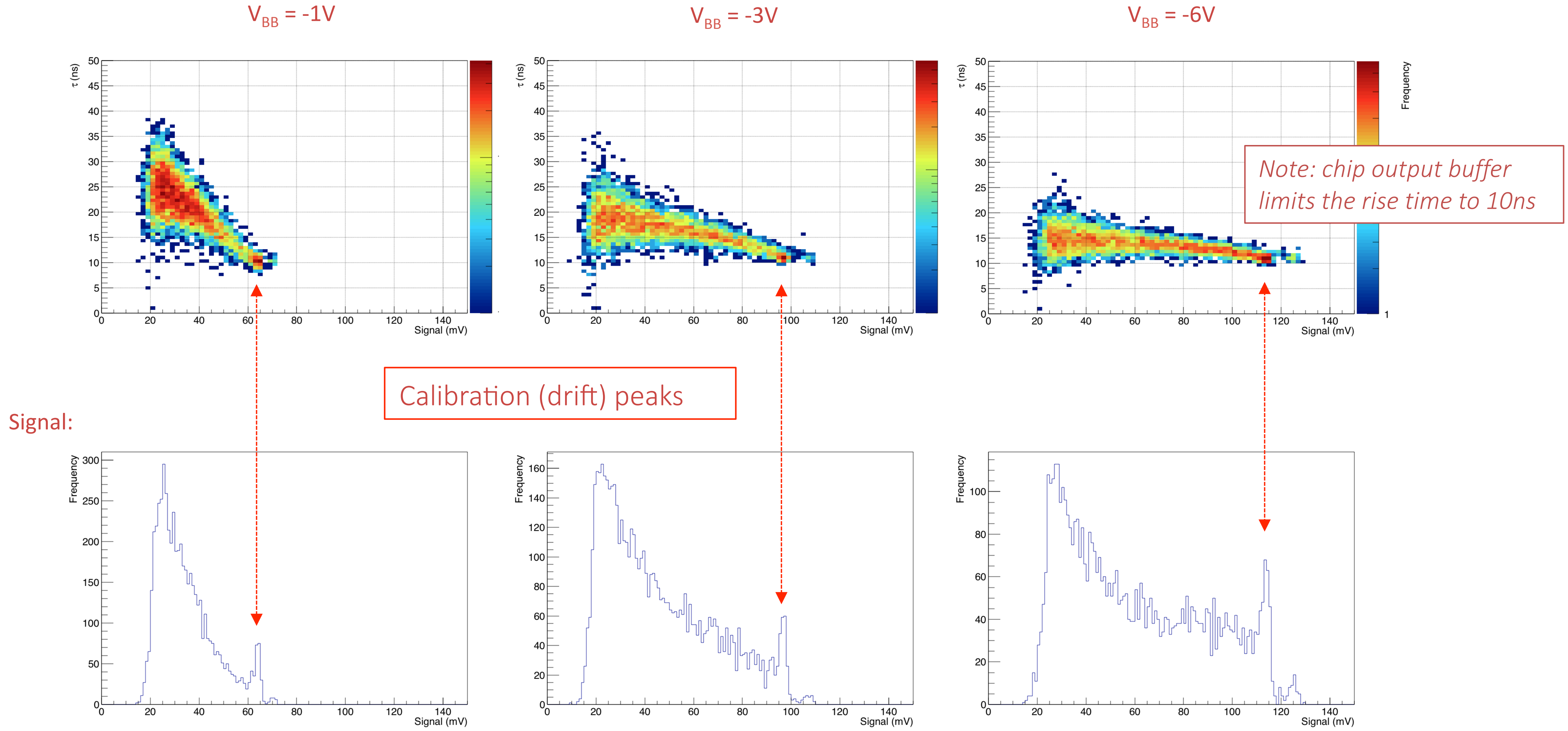
2. Absorption in non depleted volume of the epitaxial layer: charge partially collected by diffusion and then drift, charge sharing depending on position of X-Ray absorption
   - Charge collection time expected to be dependent on distance of X-Ray absorption from the depleted volume, and longer than events of case 1.

3. Absorption in substrate
   - Contribution depending on depth of X-Ray absorption, and charge carrier lifetime within substrate

TJ standard process – charge collection time and seed signal

Tests performed on investigator chip (same pixel as ALPIDE) with analogue readout

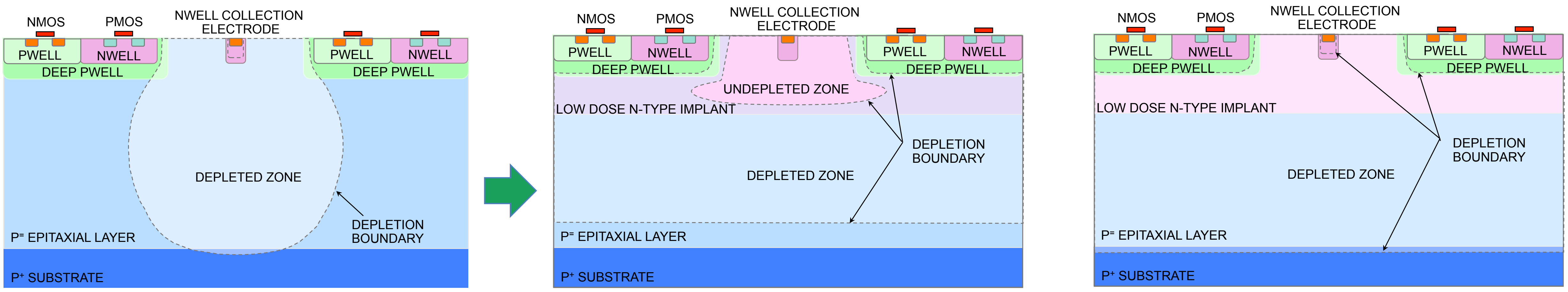
Pixel size: 28 x 28 μm^2, CE: 2 x 2 μm^2 centered in a 8 x 8 μm^2 opening, P-well & substrate @ -6V, CE @ 1V



Towards better radiation tolerance and timing: modified process

Main damage mechanism: displacement damage (Non-Ionizing Energy Loss or NIEL)

Collect signal charge FAST before it gets trapped => depletion and large electric field…



Standard, not fully depleted | Not fully depleted at low reverse bias | Depletion at higher reverse bias

Additional implant for full depletion (no changes in sensor and circuit layout)

Separation of collection electrode from junction.

➪ order of magnitude improvement in radiation tolerance

Side development of ALICE for ALPIDE ➪ The ALICE investigator and prototype ALPIDE chips exist with both flavors

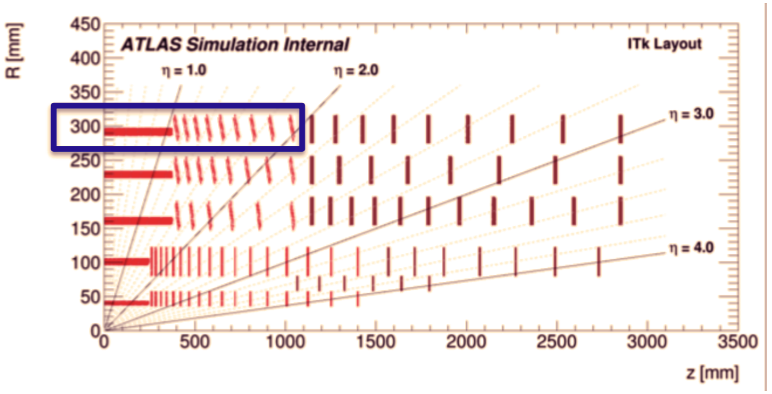
NIMA 871 (2017) pp. 90-96. https://dx.doi.org/10.1016/j.nima.2017.07.046

➪ Triggered development in ATLAS H. Pernegger et al, 2017 JINST 12 P06008

New developments for ATLAS ITk L4

Outermost layer of ITk Pixel Barrel

- 2016 quad modules
- 3m^2

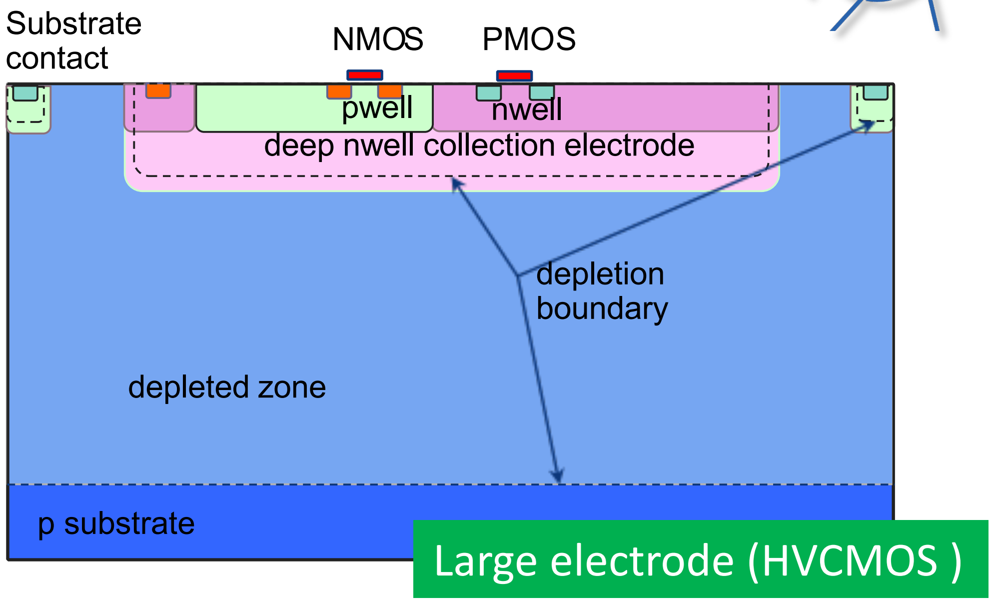


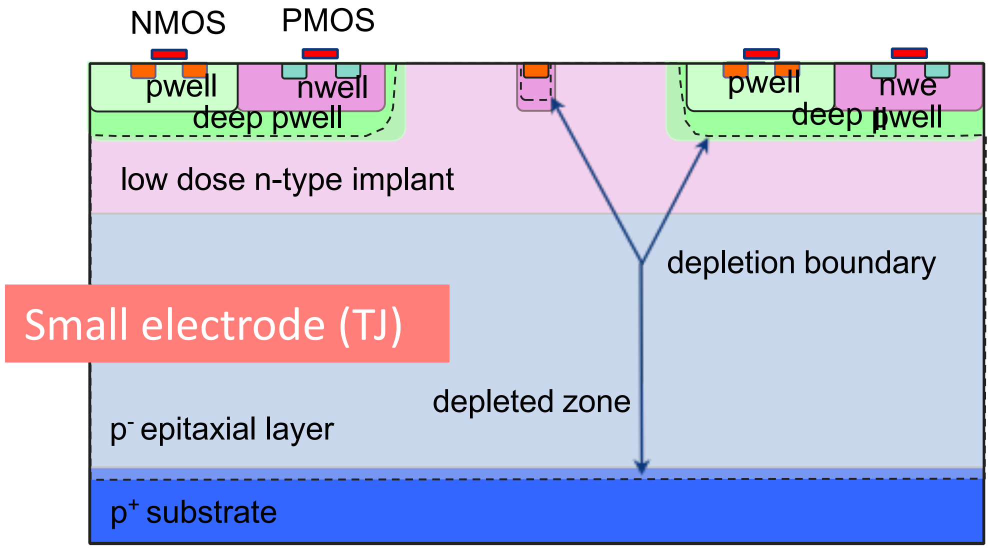
For 4000 fb^{-1}

- TID = 80 Mrad
- NIEL = 1.5 x 10^{15} n_{eq}/cm^2

Monolithic CMOS sensors were considered as option for the outermost layer

- Saves bump bonding for 45% of outer barrel system
- Cost reduction and reduce module assembly time





Three developments on three technologies

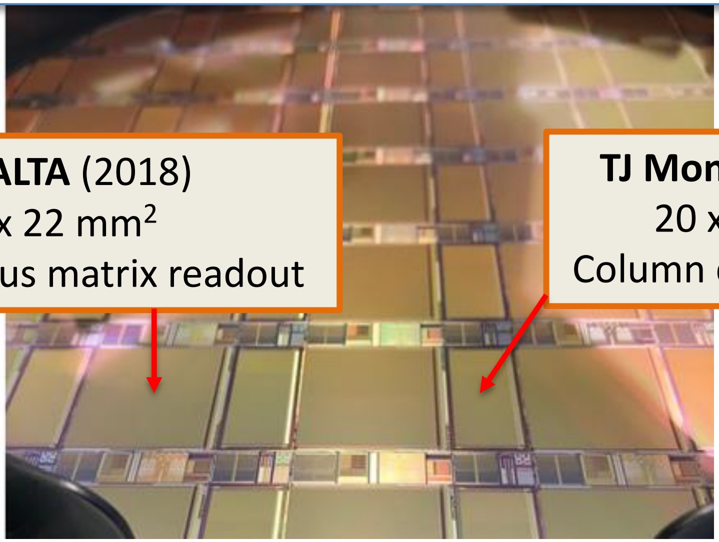
- Large CE: AMS ➪ TSI (ATLASPix) → *"HV-CMOS", I. Peric, Tuesday*
- Large CE: LFOUNDRY (Monopix)
- Small electrode: TJ modified process (MALTA, Monopix)

"CMOS Sensor development in Bonn", N. Wermes, Tuesday

New developments for ATLAS ITk: small electrode TJ modified process

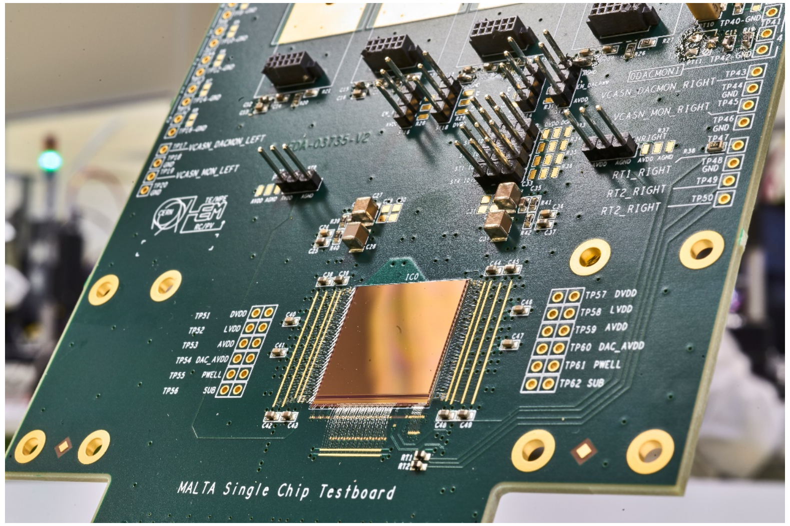
Analogue front-end optimized for timing, based on ALPIDE

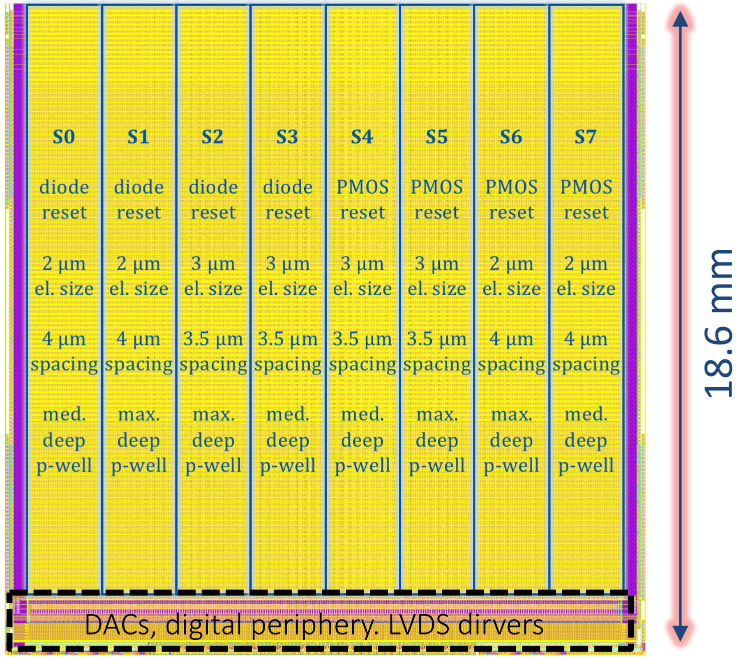
Design of two large scale demonstrators
Collaboration CERN - Bonn



TJ MALTA (2018)
20 x 22 mm^2
Asynchronous matrix readout

TJ MonoPix (2018)
20 x 10 mm^2
Column drain readout



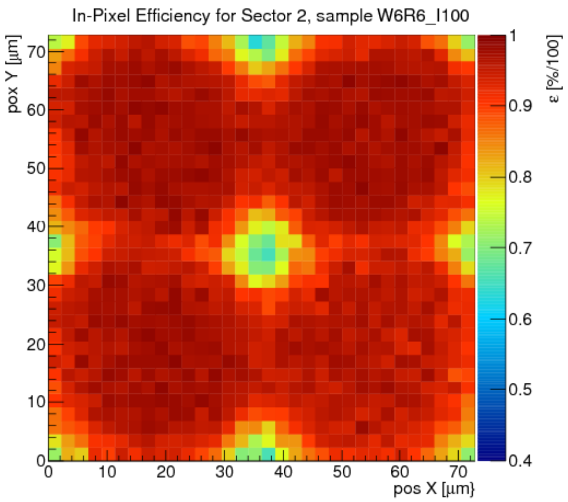


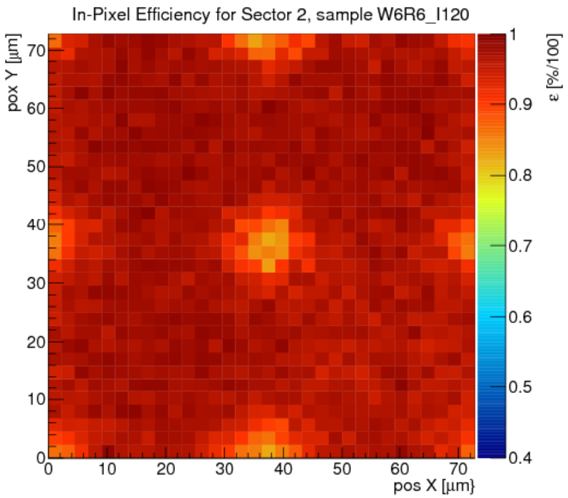
MALTA: Monolithic Pixel Detector from ALICE to ATLAS

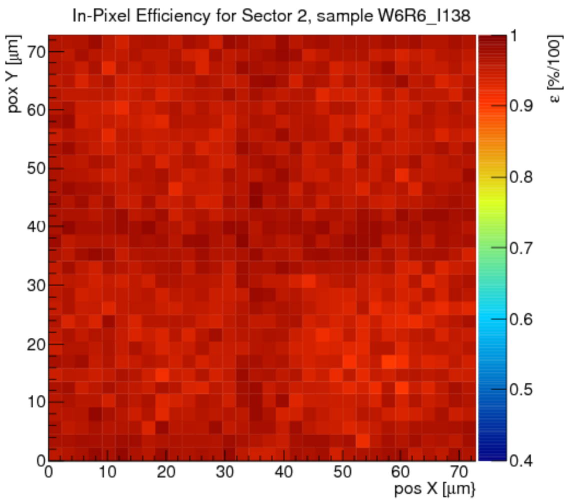
- The 512 x 512 pixel (36.4µm x 36.4 µm) – 8 sectors
- Front-end is a development from the ALPIDE one
- Design based on low-power analogue front-end and an asynchronous architecture to readout the pixel matrix

Enrico Junior Schioppa, VCI, 2019

MALTA – efficiency in test beam before and after irradiation

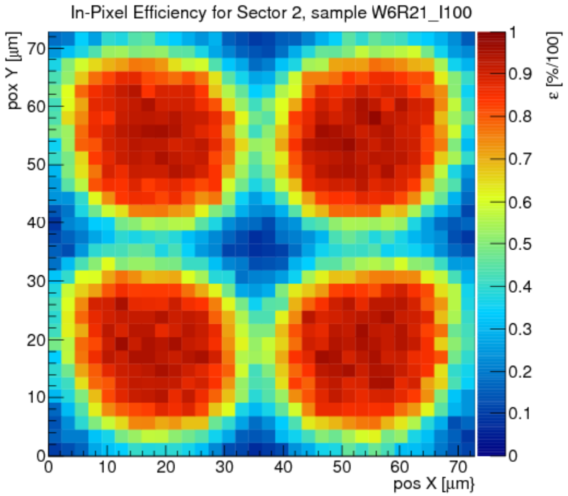


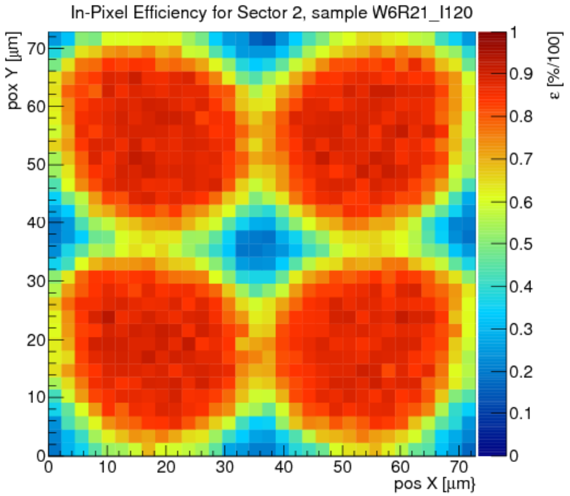




Unirradiated:
lowering the threshold gives the full efficiency

Decreasing threshold from ~600 e^- to ~250e- (unirradiated) / ~350e^- (irrad.)





Could not reach
Lower threshold
(RTS + Making issues)

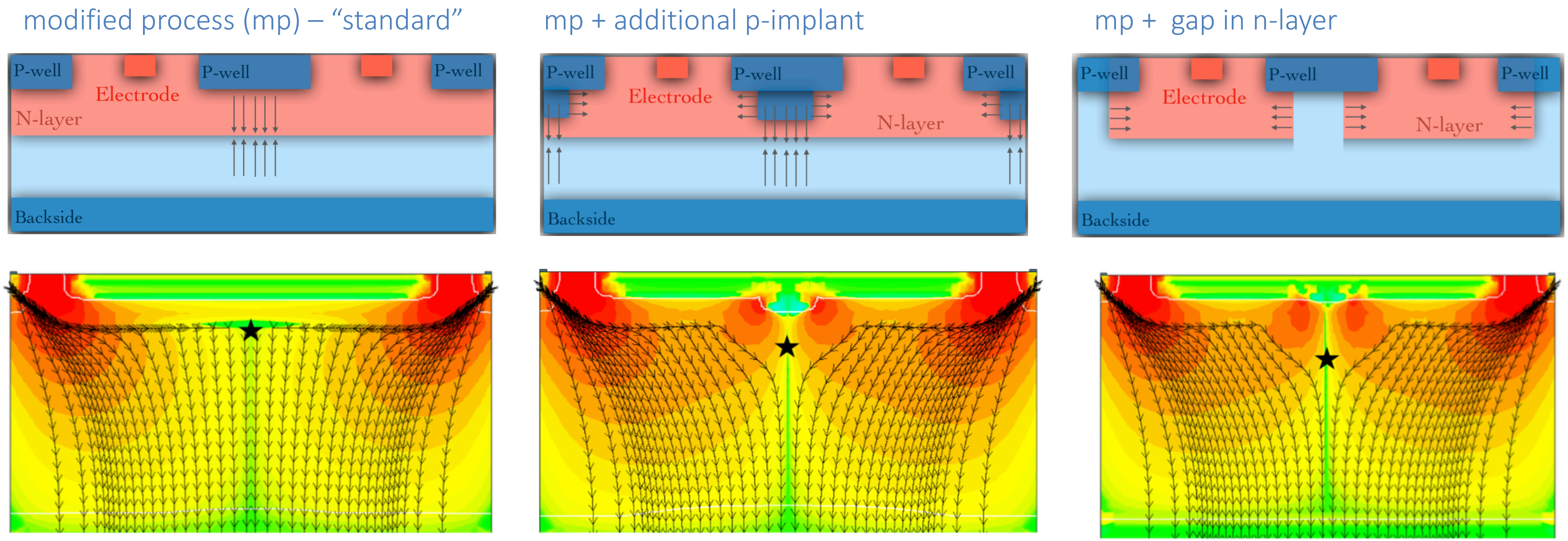
Test of new prototype circuits (Mini-Malta) with fixes for both problems are well advanced

Neutron irradiated
5×10^{14} n_{eq}/cm^2

Inefficiency at pixel edges due to low lateral electric field

Enrico Junior Schioppa, VCI, 2019

MALTA – efficiency in test beam before and after irradiation



3D TCAD Simulaitons, Magdalena Munker (CERN), Pixel 2018 (Taipei - Dec 2018)

TJ modified process: E field minimum at pixel corners => charges pushed to the minimum before they propagate to CE

Additional p-implant or gap in n-layers for improved lateral field: bend the field towards the CE, shorted drift path

“Thin Pixel Optimization for CLIC”, D. Dannheim, Tuesday

Mini-MALTA sensor - optimization of "process modification"

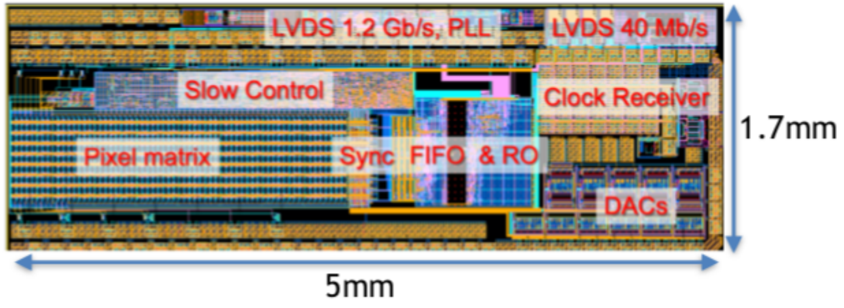
Developed to demonstrate $10^{15}\ n_{eq}/cm^2$ radiation hard TJ180 matrix with small electrodes

- 36μm pixel pitch, 3μm electrode
- Based on previous MALTA and MonoPix chip

courtesy of H. Pernegger

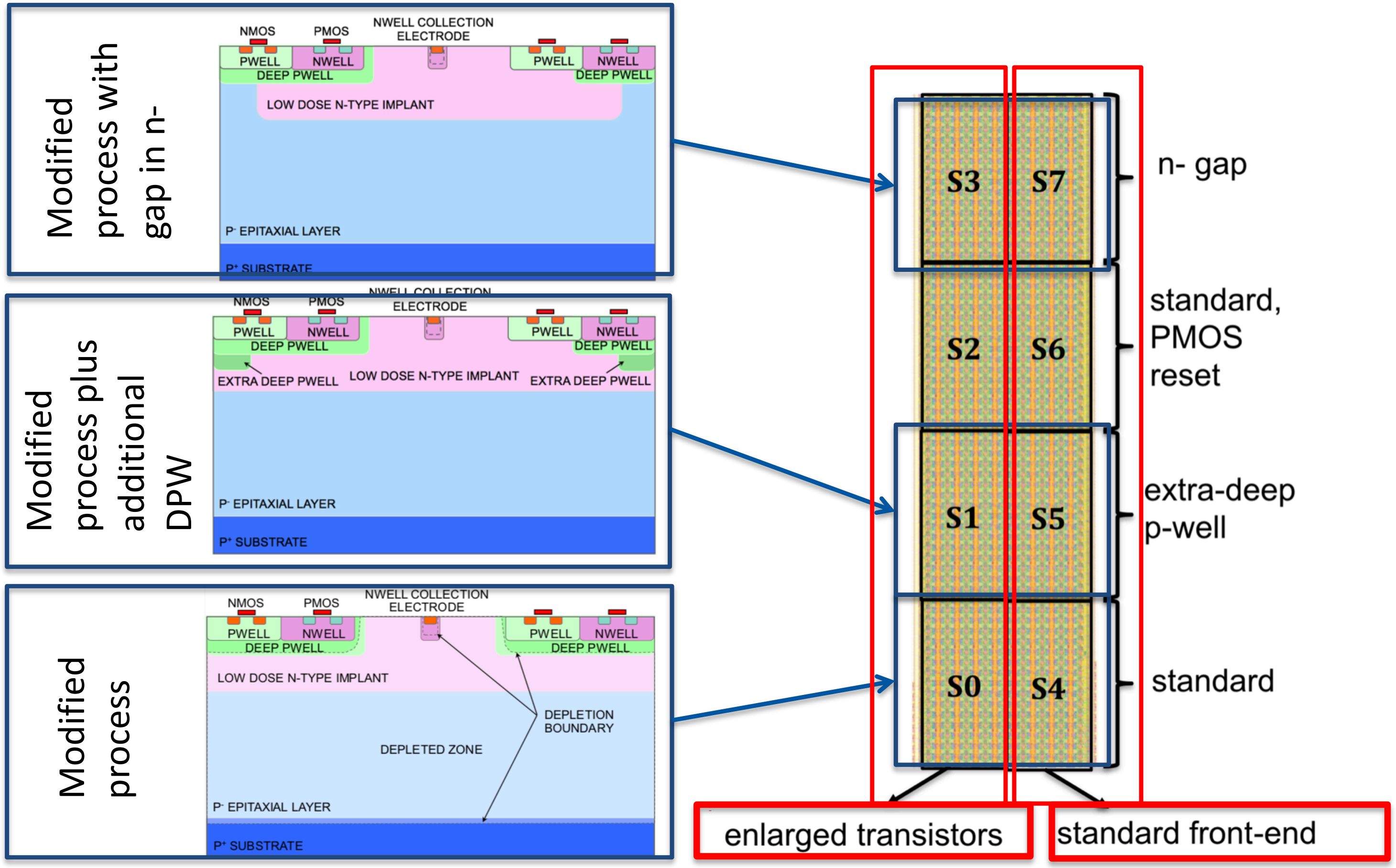
Main strategy

- Improved front-end to achieve larger gain, lower threshold (down to 120e^- measured) and improve RTS noise
- Improve charge collection in pixel corners through modification of implant structures



https://doi.org/10.1088/1748-0221/14/05/C05013

https://doi.org/10.1088/1748-0221/14/06/C06019

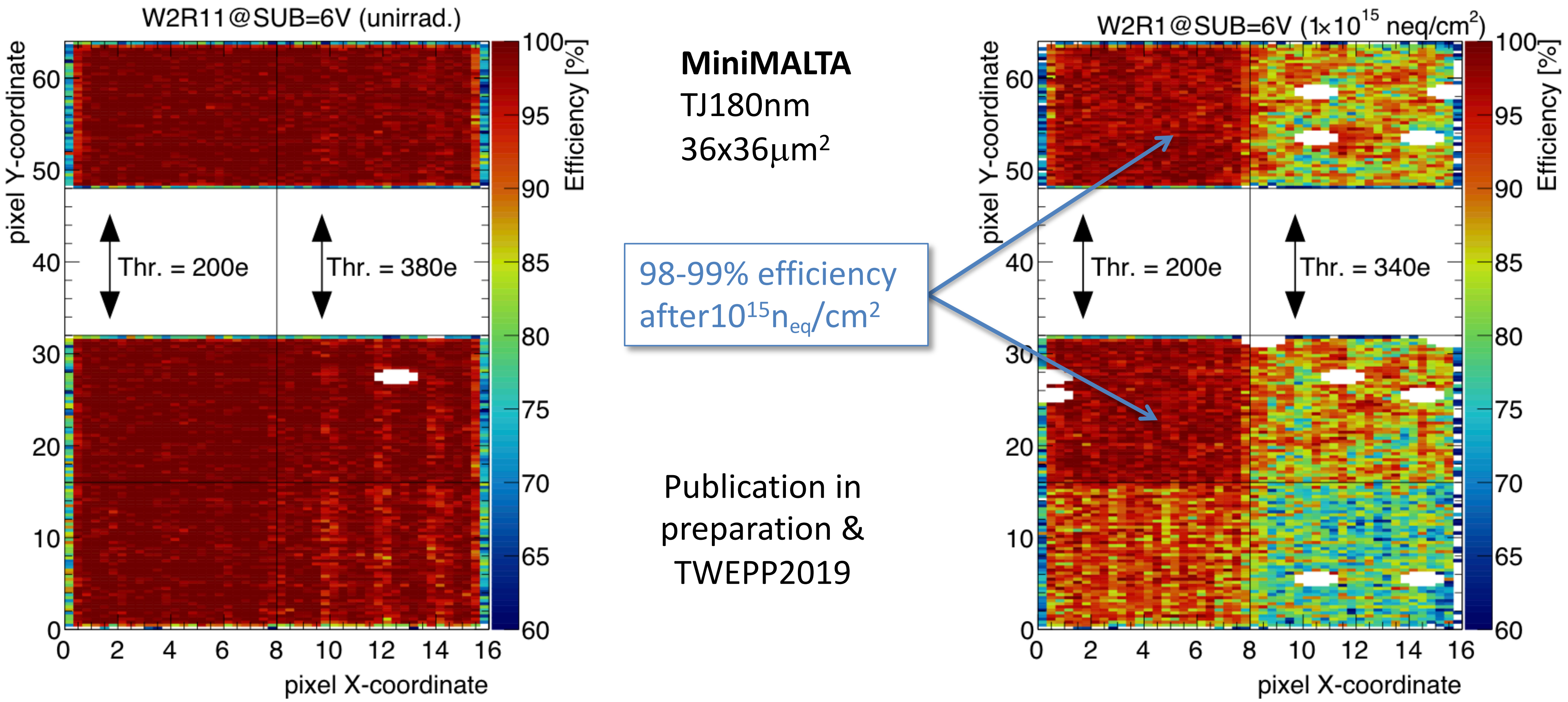


Mini-MALTA sensor - optimization of "process modification"

Preliminary beam test results show that **>98% efficiency is reached after 10^{15} n_{eq}/cm^2** through the combination of front-end improvements and charge collection improvement in the pixel corners

courtesy of H. Pernegger

Efficiency before/after 10^{15} n_{eq}/cm^2 irradiation



MiniMALTA
TJ180nm
36x36μm^2

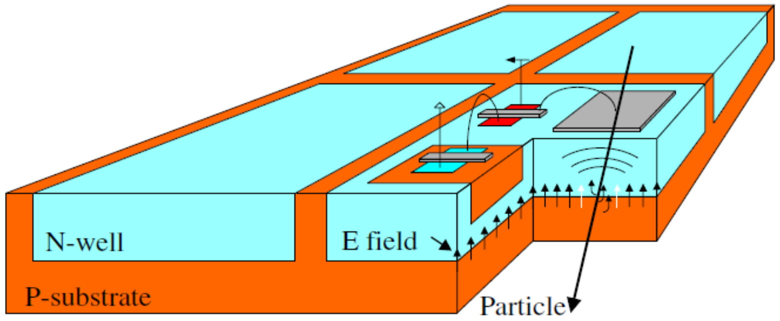
Publication in preparation & TWEPP2019

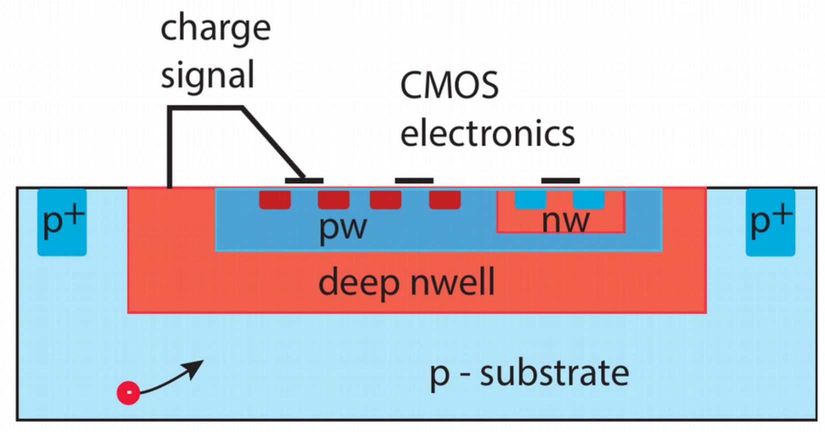
HV CMOS – developments for the Mu3e tracker and the ATLAS ITk

- Compatible with standard CMOS technology
- Triple well process on p-type substrate (20- 1000 Ω cm)
- Prototypes with var CMOS processes (AMS, TSI, LFounfry)

The HV CMOS Collaboration

I. Peric et al., NIM A 582 (2007) 872

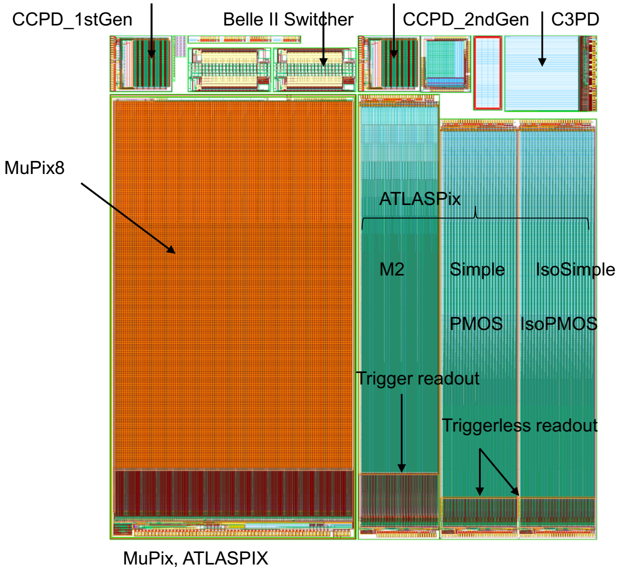




- The collection diode occupies a large part of the pixel
- Electronic circuits inside deep n-well
- HV O(60 – 120V) contacts at the top side
- MUPIX8 pixel: 80x81 μm^2

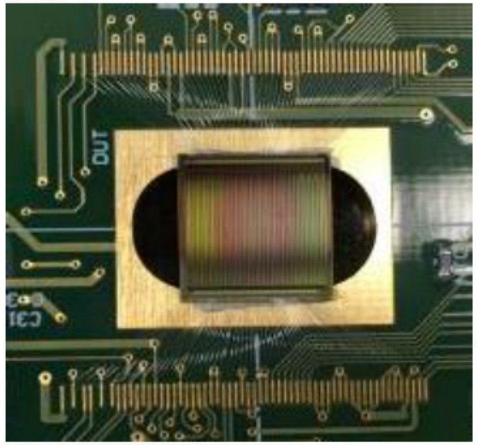
- Circuitry in the collection diode introduces additional sensor capacitance
- Keep pixel circuitry as simple as possible
- Confine digital circuitry at the periphery

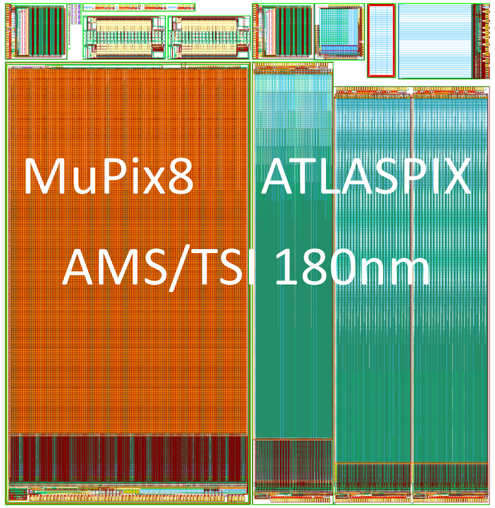
"HV-CMOS", I. Peric, Tuesday



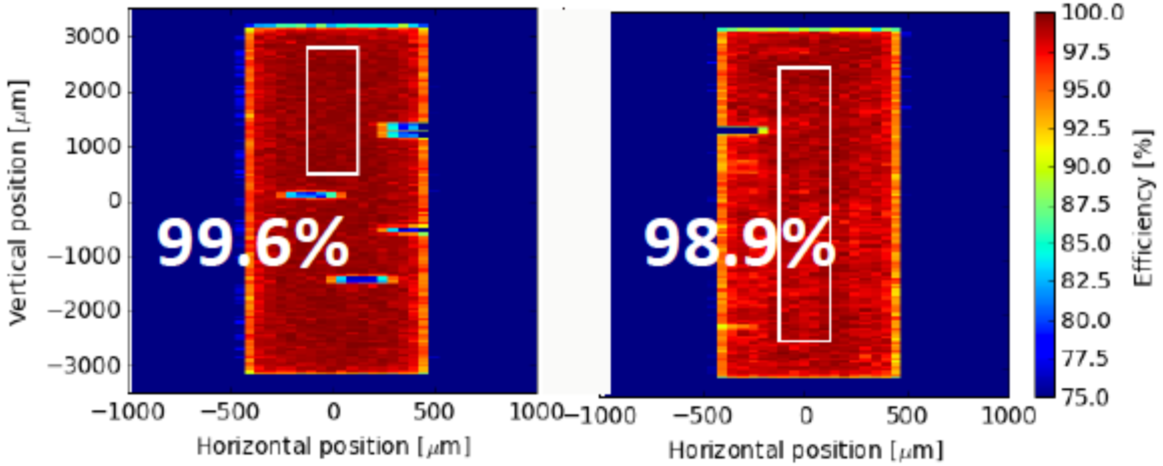
courtesy of I. Peric and A. Schoening

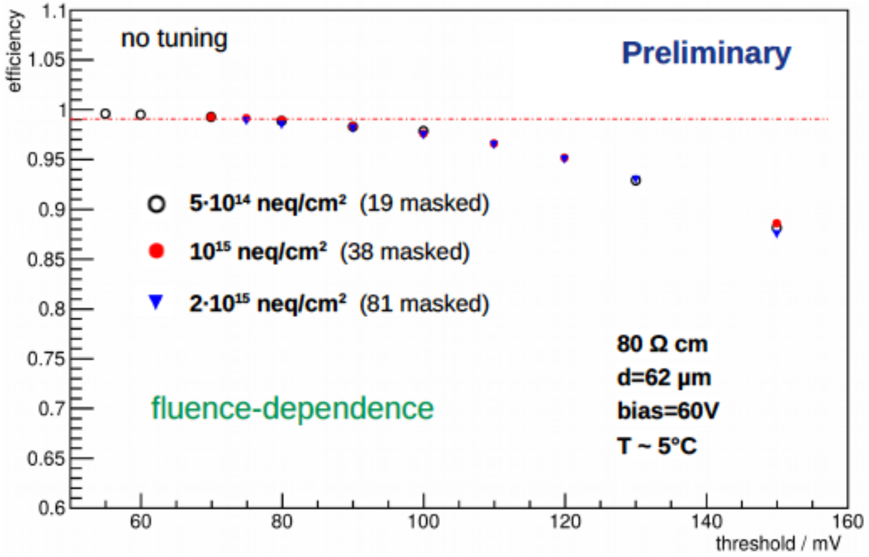
Better sensor radiation tolerance and timing: Large collection electrode





Efficiency non-irradiated after 1.14 E15 n_{eq}/cm^2





T. Hirono et al., https://doi.org/10.1016/j.nima.2018.10.059

"CMOS Sensor development in Bonn", N. Wermes, Tuesday

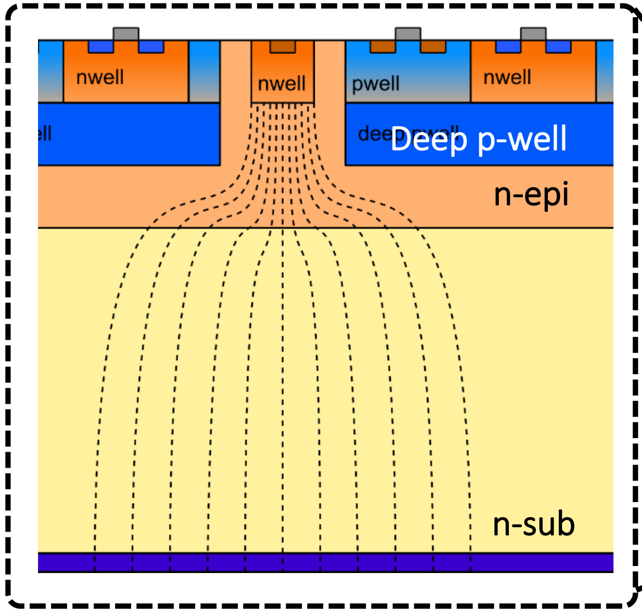
courtesy of I. Peric and A. Schoening

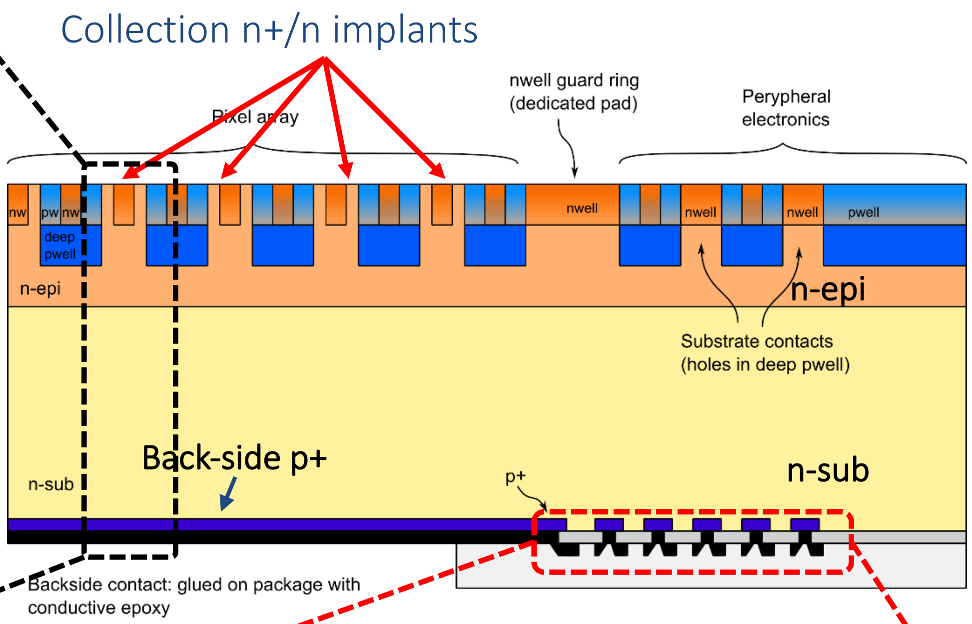
"HV-CMOS", I. Peric, Tuesday

INFN projects SEED and ARCADIA: two phases of the same development

The SEED project successfully demonstrated a fully depleted, up to 300 µm thick MAPS sensor

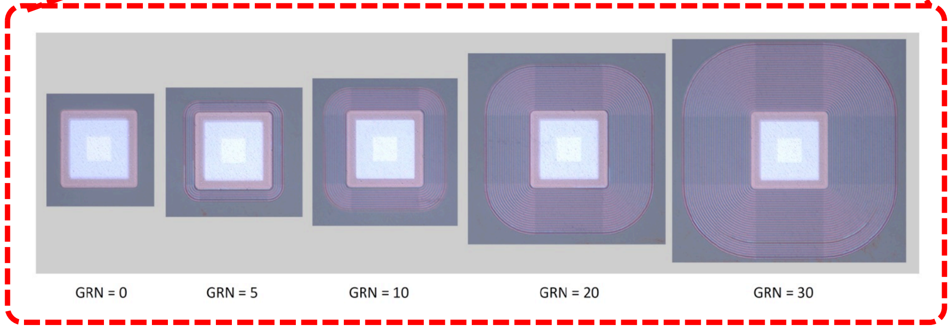
- LFoundry 110nm CMOS process.
- Sensor nodes are n-type implantation (become insulated only with full substrate depletion)
- The high resistivity, floating zone n-type substrate is depleted by negative voltage at the p+ backside
- Deep pwell implantations allows implementing full CMOS gates





- Double-sided lithography was used for the processing of the backside layers (5 extra masks)
- The backside p+ implantation was done after thinning the substrate, and activated with laser annealing
- To avoid early breakdown, termination structures with floating guard rings have been added at the borders

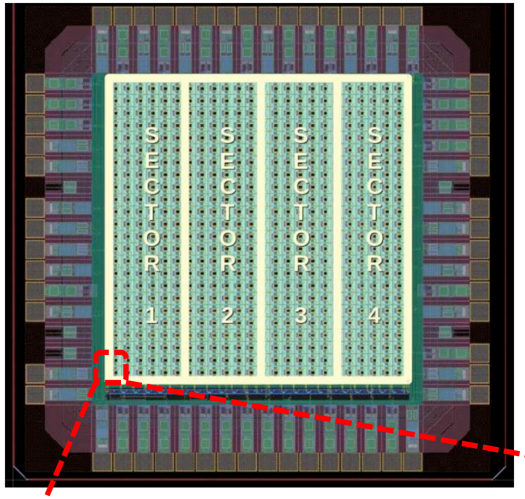
Courtesy of P. Giubilato



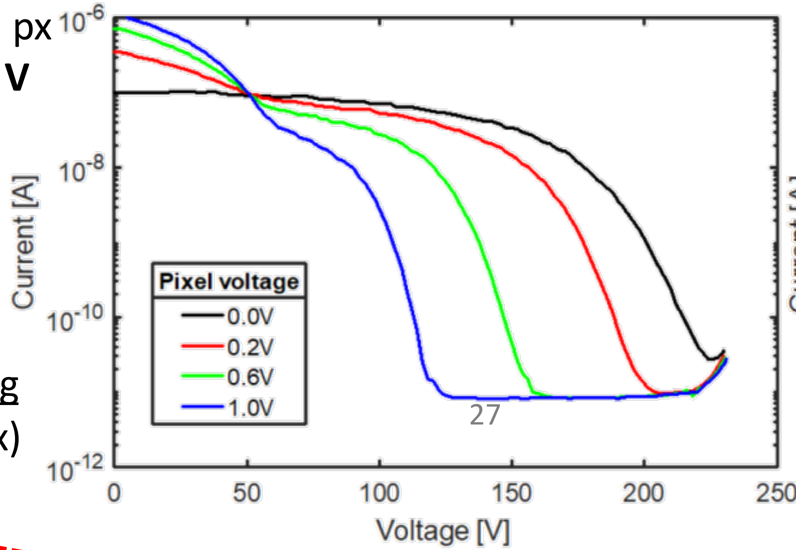
Different guard-rings on the backside diodes

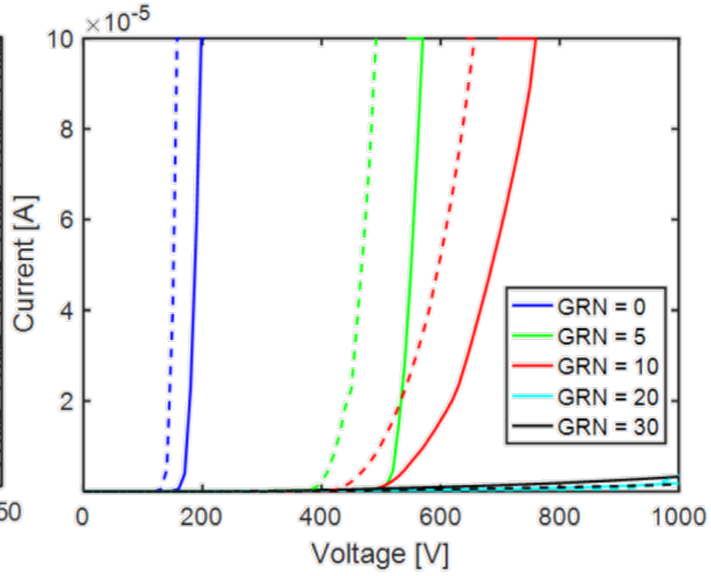
INFN projects SEED and ARCADIA: two phases of the same development

The SEED sensor has been paired with a simple readout electronics tailored for testing the sensor characteristics, including CDS and baseline restoration on-pixel in a 50 x 50 μm^2 pixel pitch.

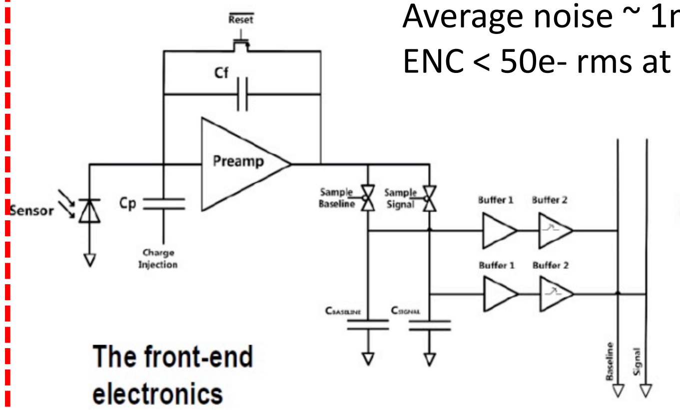


- Die area: 2×2 mm^2, 50 µm px
- low voltage operation: **1.2 V**
- 4 independent sectors
- Snapshot shutter (70 fF storage)
- Node capacitance: 40 fF
- Baseline regulator
- Correlated double sampling
- 5 MHz readout speed (max)



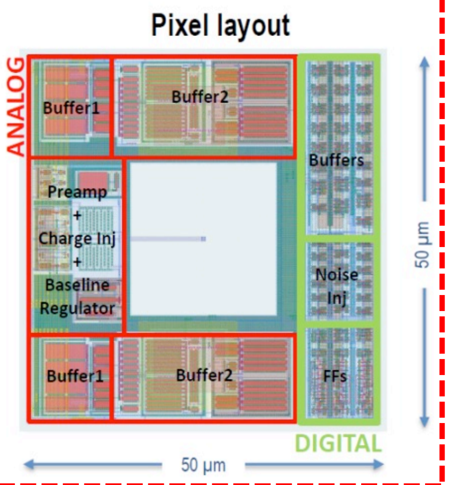


Full depletion between 100 and 200V (300 µm thick), then punch-trough starts

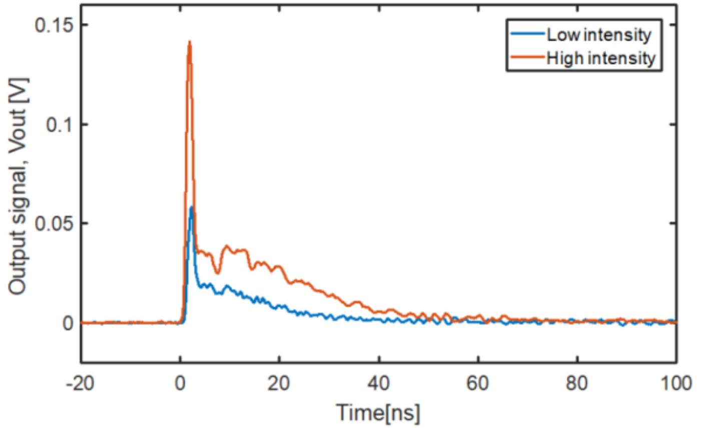


The front-end electronics

Average noise ~ 1mV:
ENC < 50e- rms at RT



Fast charge collection when fully depleted (1ps FWHM laser with external 1 GHz amplifier)



Courtesy of P. Giubilato

CMOS APS – wafer-scale integration

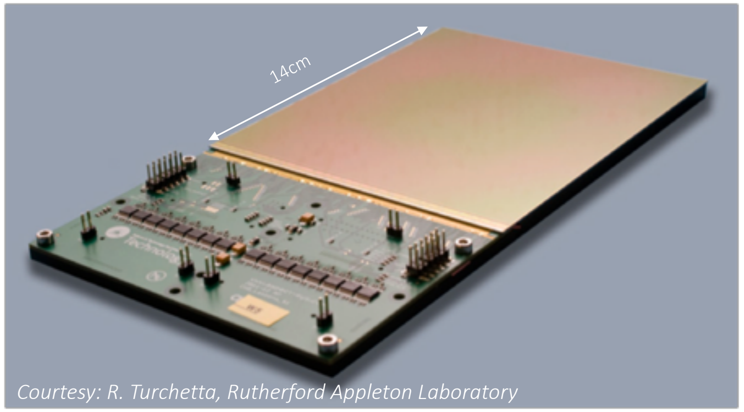
Photolithographic process defines wafer reticles size ➪ Typical field of view O(2 x 2 cm^2)

Reticle is stepped across the wafers to create multiple identical images of the circuit(s)

A stepping process called "stitching" allows building sensors of arbitrary size, the only limit being the size of the wafer.

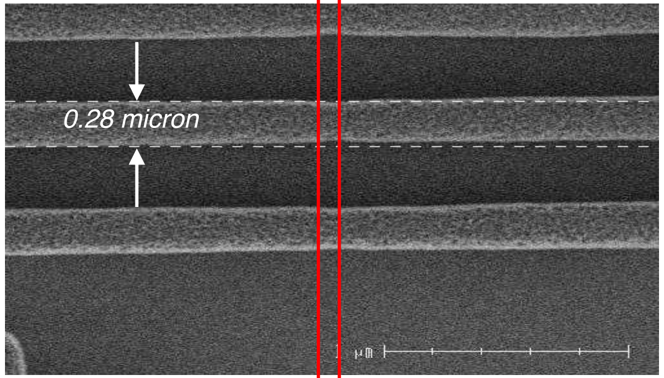
- Reticle made of blocks
- Printing only individual blocks at each step with a tiny well-defined overlap

These days, stitching is widely applied in the digital imaging industry (e.g. large flat panels for medical and dental X-rays)



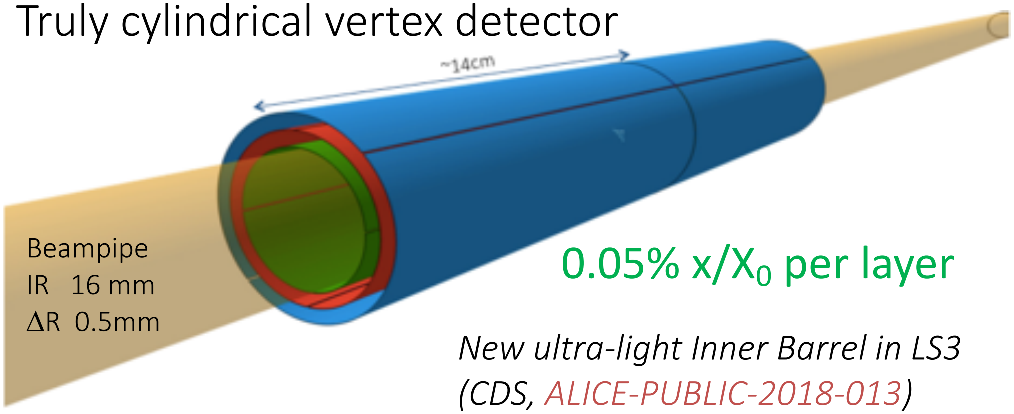
Courtesy: R. Turchetta, Rutherford Appleton Laboratory

Seamless stich boundary



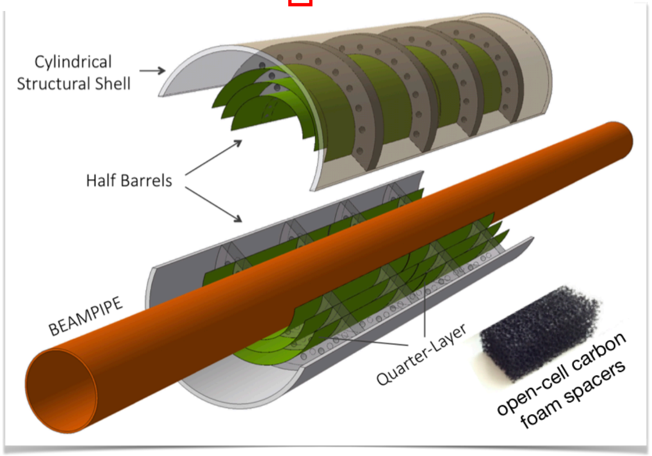
Ultra-thin chip (<50 um): flexible with good stability

Truly cylindrical vertex detector



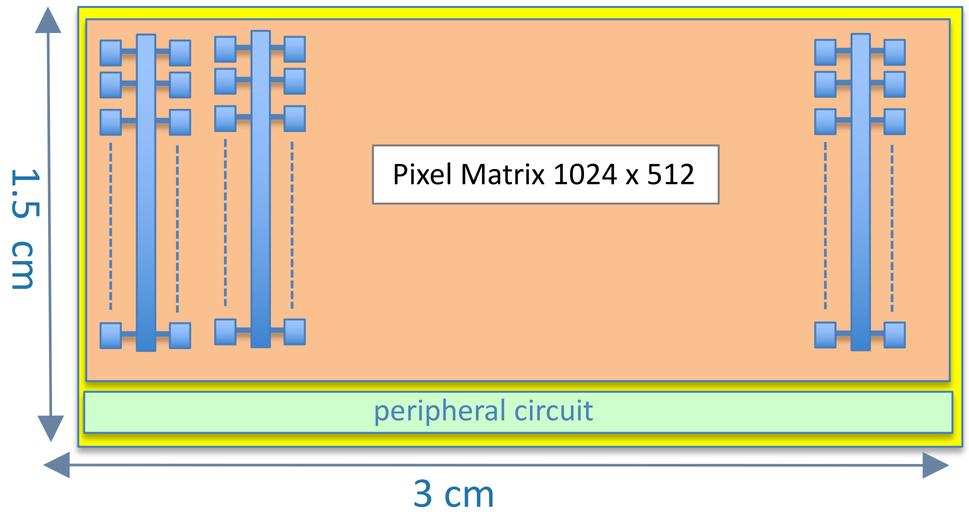
0.05% x/X_0 per layer

New ultra-light Inner Barrel in LS3 (CDS, ALICE-PUBLIC-2018-013)

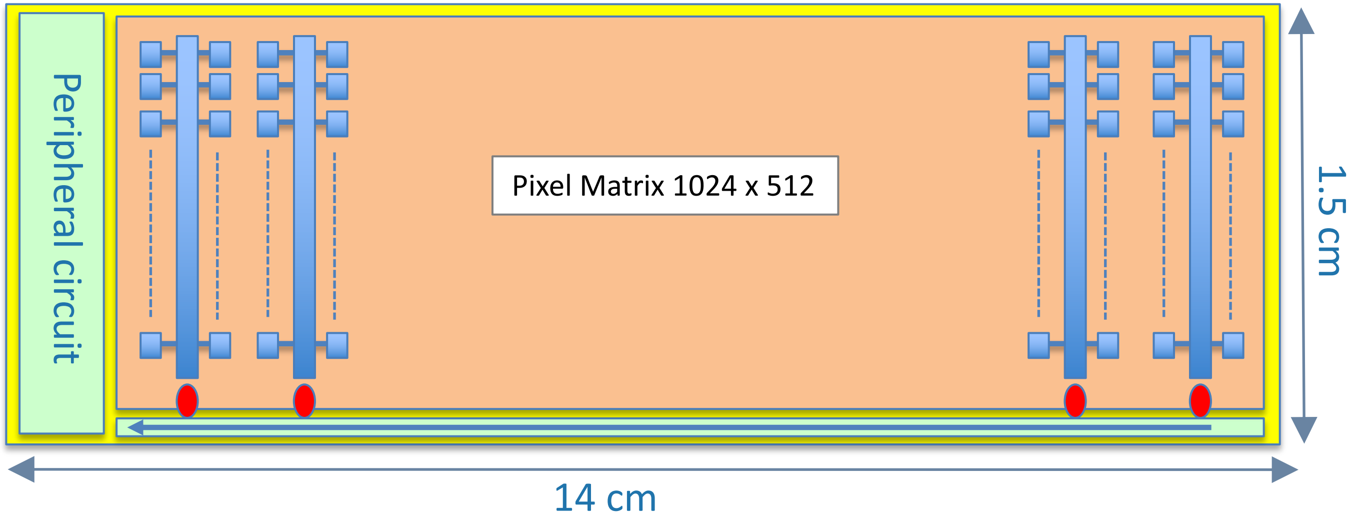


CMOS APS – wafer-scale integration

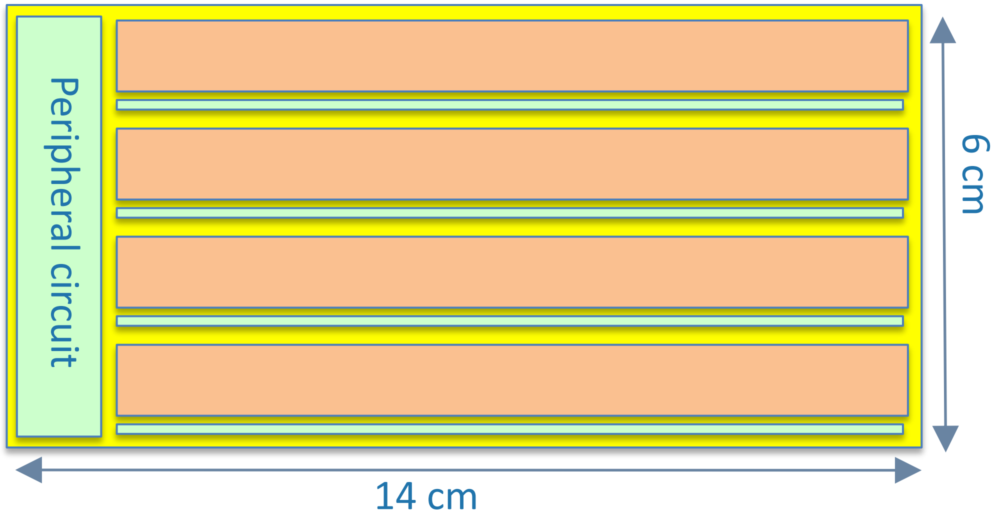
ALPIDE Chip



1D stitched sensor (z direction)

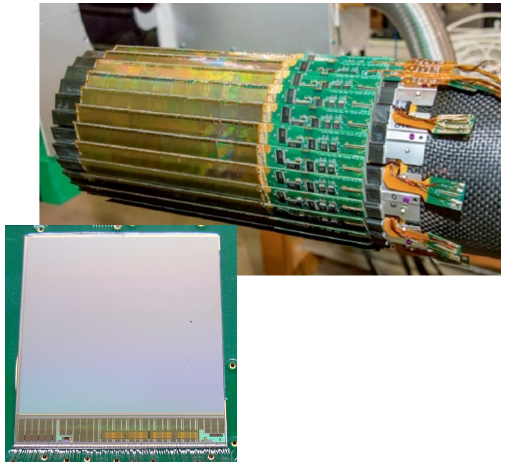


2D stitched sensor – wafer-scale

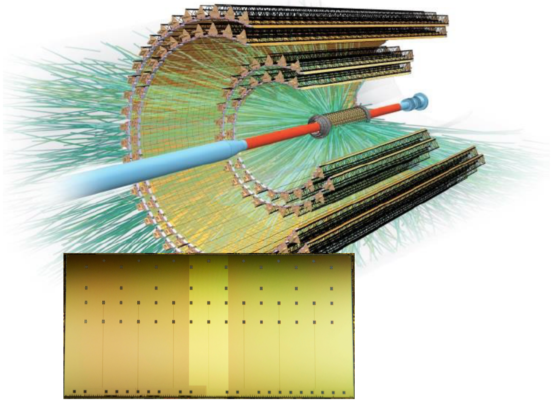


Parameter	ALPIDE	Wafer-Scale Sensor Light
Technology node	180nm (Tower)	< 65nm/28nm (Tower or X)
Silicon thickness	50um	< 40um
Pixel size (um^2)	27 x 29	O (10 x 10)
Chip dimensions (mm^2)	15 x 30	Scalable up to 280 x 100
Front-end pulse duration	~5ms	~ 200ns
Time resolution	~1ms	<100ns (<10ns CLIC)
Max particle fluence	> 100MHz/cm^2	> 100MHz/cm^2
Max particle readout rate	10 MHz/cm^2	~ 100MHz/cm^2
Power Consumption	40mW/cm^2	< 20mW/cm^2 (pixel matrix)
Detection efficiency	>99%	99%
Fake hit rate	<10^{-7} event/pixel	<10^{-7} event/pixel
NIEL radiation tolerance	~3x 10^{13} 1MeV n_{eq}/cm^2	10^{14} 1MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10MRad

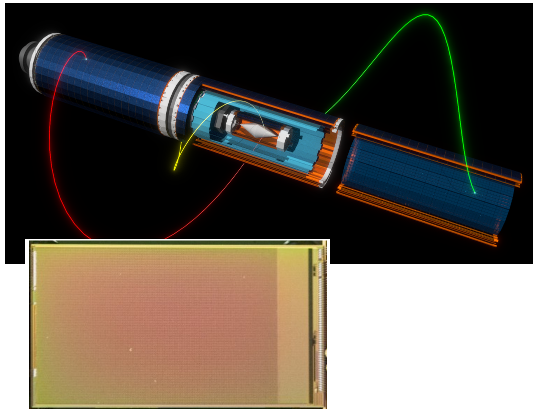
Concluding Remarks



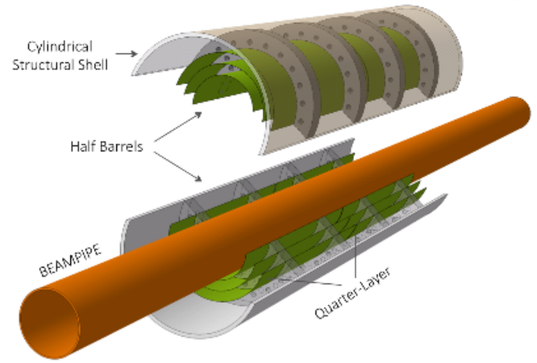
MIMOSA28 in STAR
First CMOS APS system in HEP



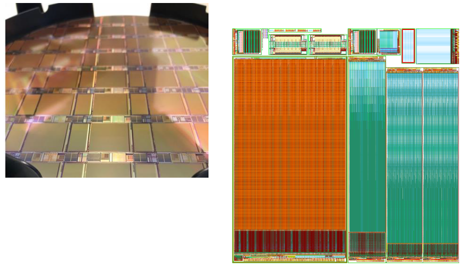
ALPIDE in ALICE
First CMOS APS in HEP with sparse readout similar to hybrid sensors
First MAPS in HEP to cover 10 m^2



Mupix 8 for Mu3e Tracker
HV-CMOS
First fully depleted CMOS APS



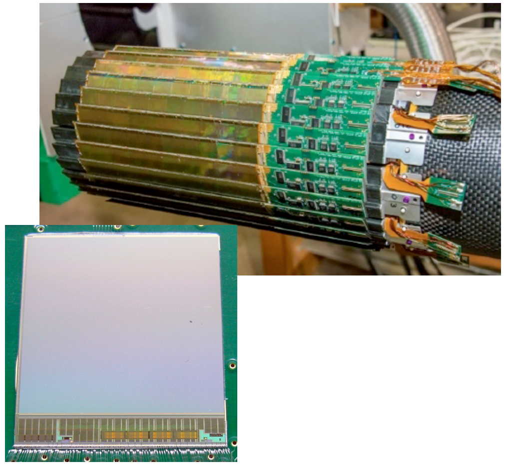
ALICE
Stitching for low-mass cylindrical tracker



ATLAS MAPS development
Increased radiation tolerance and timing performance (+ serial powering …)

- After years of R&D, monolithic sensors for HEP move to CMOS APS in mainstream technology
- Such large area, monolithic, low power pixel sensors are enabling devices for many applications in HEP, like vertexing, large-area tracking, digital calorimetry, time-of-flight
- Different approaches to optimize power vs radiation hardness

Concluding Remarks



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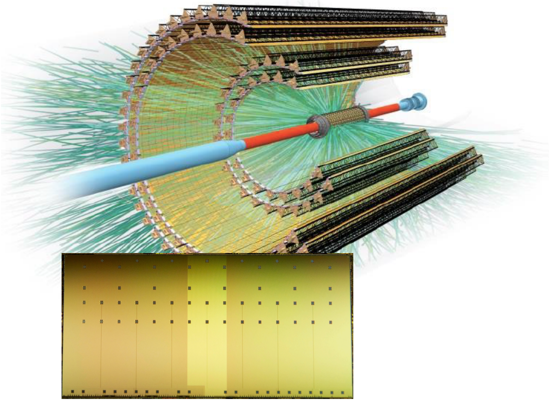
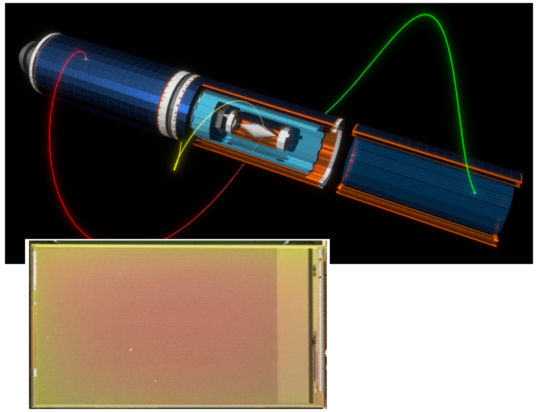
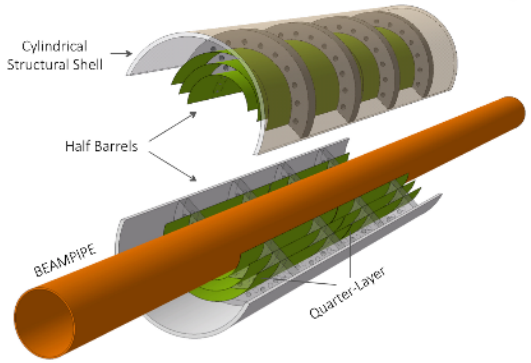
First CMOS APS system in HEP



ALPIDE in ALICE
First CMOS
readout sin
First MAPS

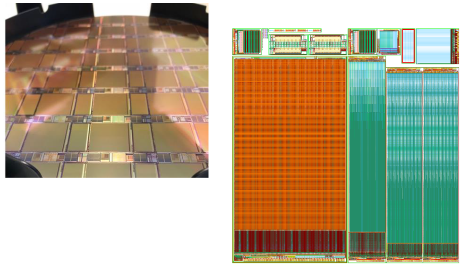


u3e Tracker
eted CMOS APS



ALICE
Stitching for low-mass cylindrical tracker

Thank You!



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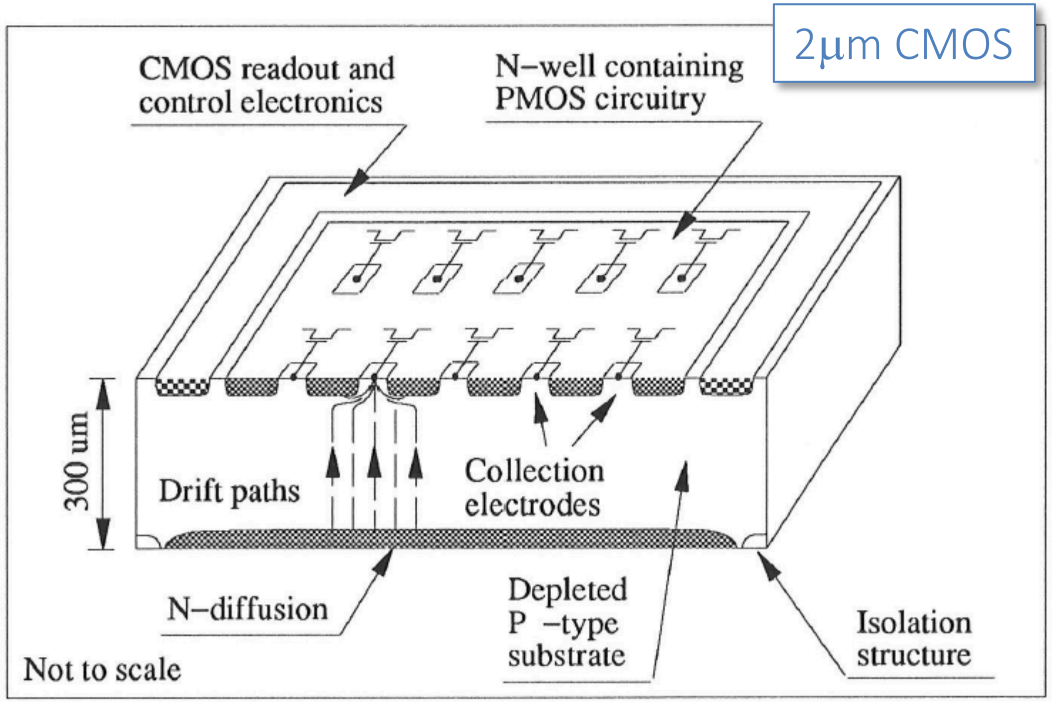
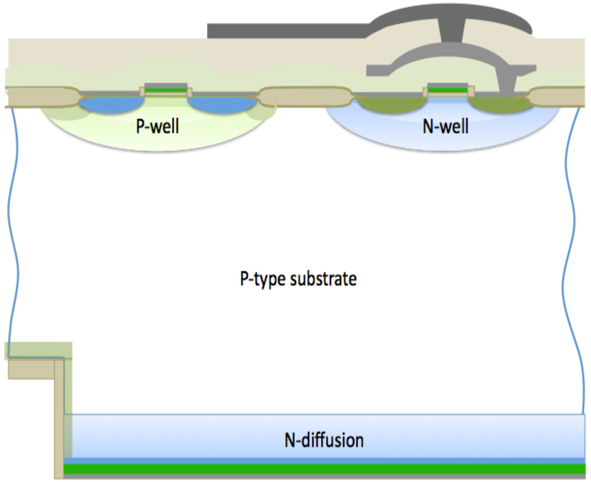
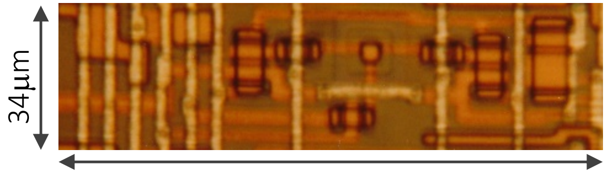
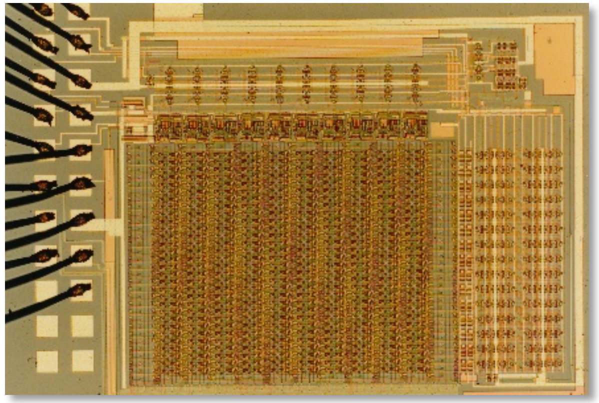
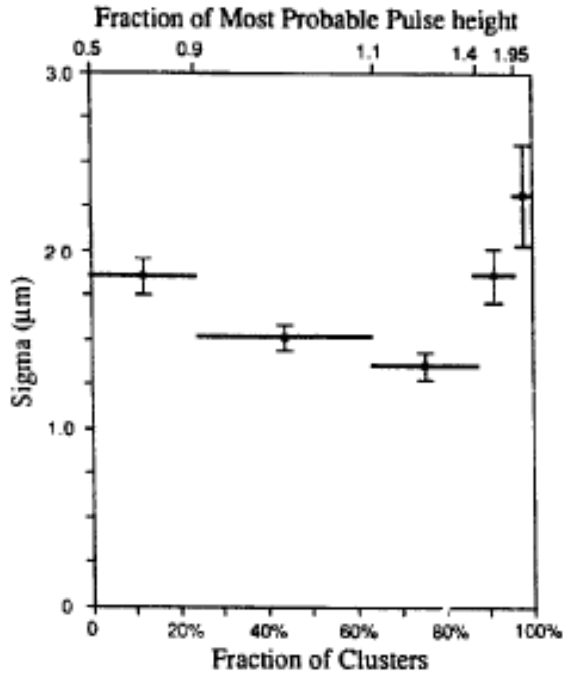
- Different approaches to optimize power vs radiation hardness











Stanford Nanofabrication Facility (BiCMOS + double-sided processing)

- Separation of junction from collection electrode
- Better than 2 μm position resolution even at large pitch due to good S/N

C. Kenney, S. Parker, J. Plummer, J. Segal, W. Snoeys et al. NIM A (1994) 258-265, IEEE TNS 41 (6) (1994), IEEE TNS 46 (4) (1999)

Courtesy of W. Snoeys

Fully depleted MAPS – small electrodes with TJ modified process

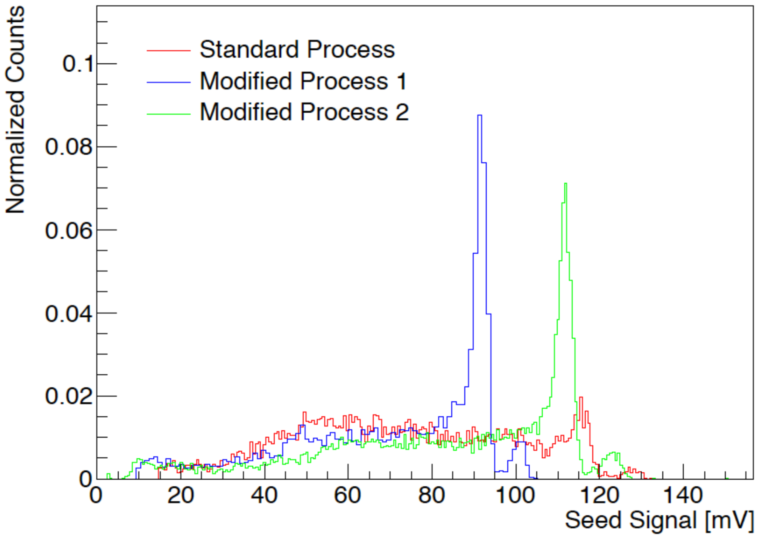
Signal and cluster distribution from a ^{55}Fe source for standard and modified process

Modified Process 1 = higher dose, Modified Process = lower dose

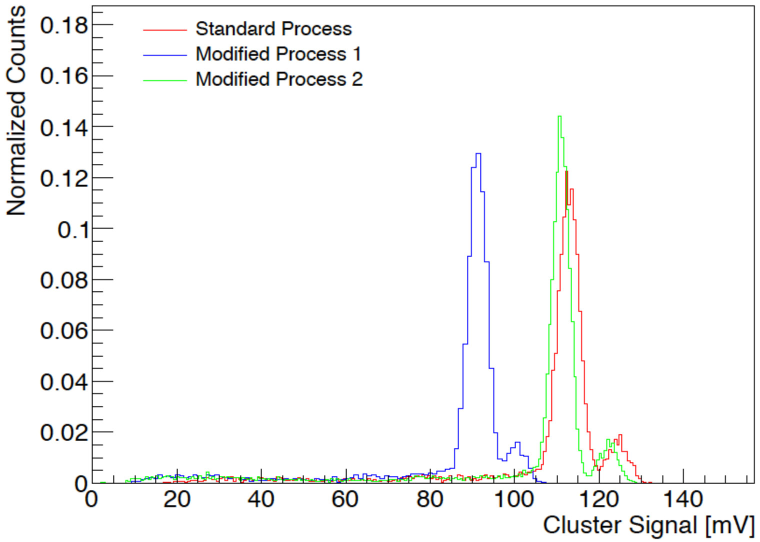
J. Van Hoorne et al., NSS 2016

Tests performed on investigator chip (same pixel as ALPIDE)

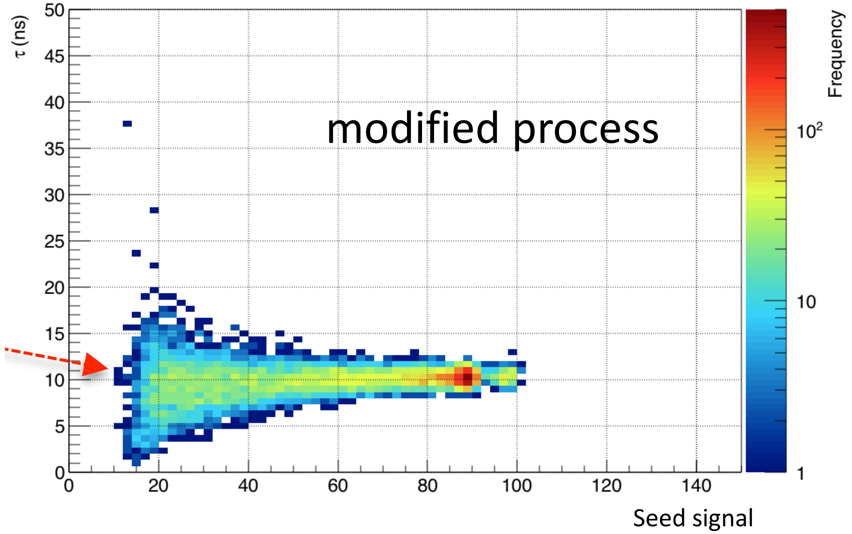
Pixel size: 28 x 28 μm^2, CE: 2 x 2 μm^2 centered in a 8 x 8 μm^2 opening, P-well & substrate @ -6V, CE @ 1V



(A) Seed signal



(B) cluster signal



Note: chip output buffer limits the rise time to 10ns

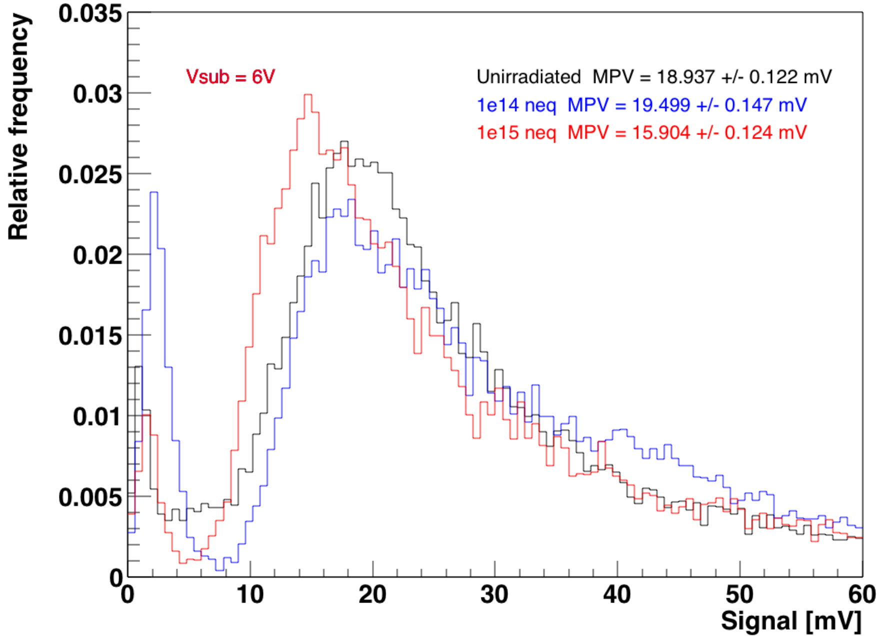
- For a lower dose (MP1) no sensor capacitance penalty
- For modified process, larger fraction of single pixel clusters (see also fraction of signal within the peak in A)

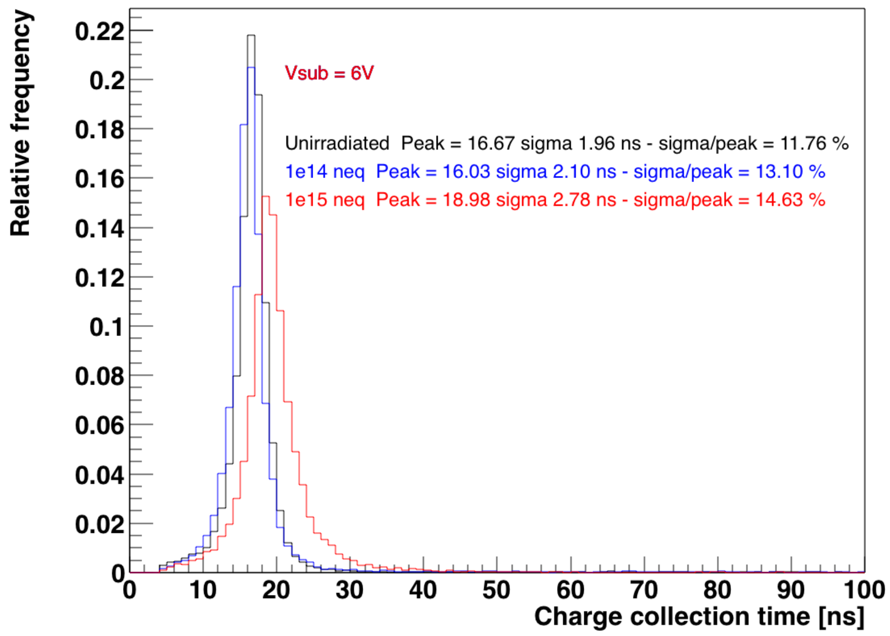
TJ modified process – charge collection time

^{90}Sr measurements on modified process samples (different setup, different pixel w.r.t. before)

- Non-irradiated
- 1 x 10^{14} 1MeV n_{eq}/cm^2 (NIEL) and 100krad (TID)
- 1 x 10^{15} 1MeV n_{eq}/cm^2 (NIEL) and 1Mrad (TID)

H. Pernegger et al 2017 JINST 12 P06008





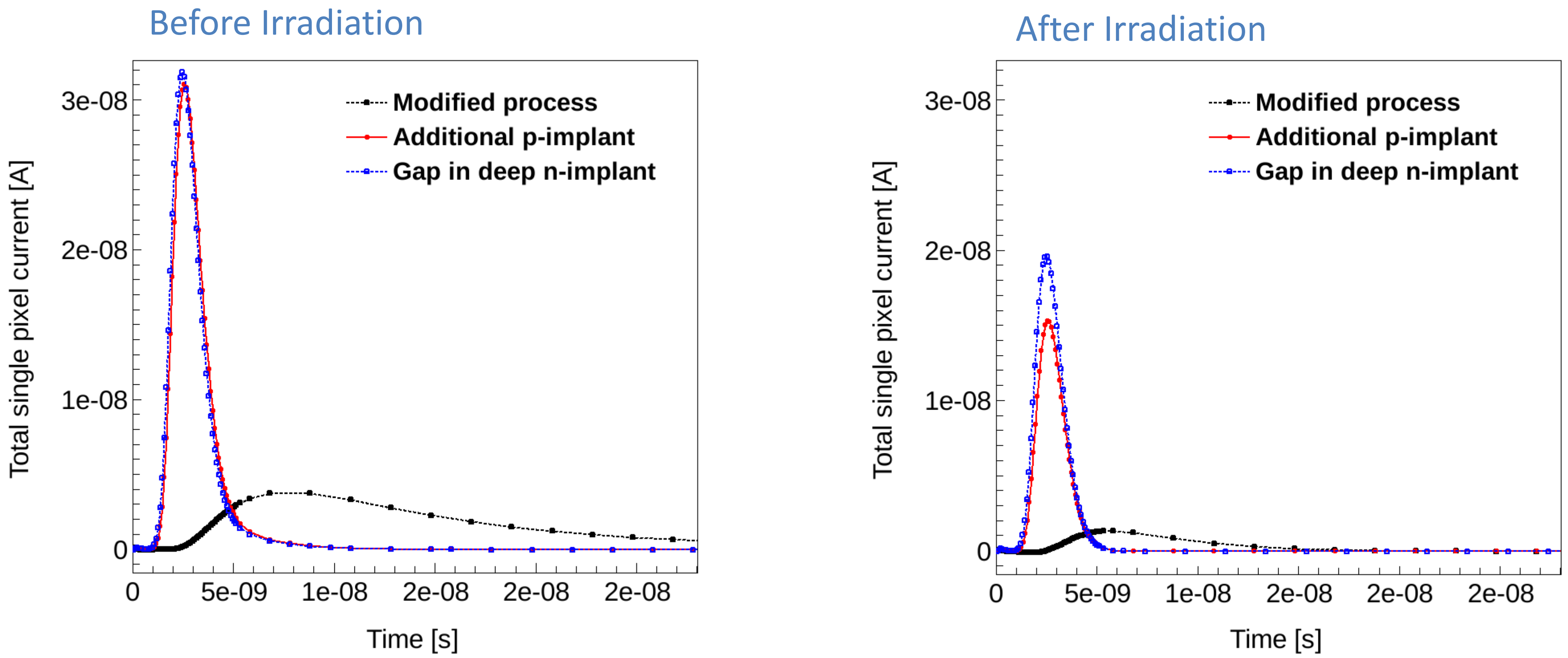
Tests performed on investigator chip (different pixel wrt to ALPIDE) *Note: chip output buffer limits the rise time to 10ns*

Pixel size: 50 x 50 μm^2, CE: 3 x 3 μm^2 centered in a 18 x 18 μm^2 opening, 25μm epi

TJ modified process with additional p-implant or with gap in n-layer

Current pulse signal

Magdalena Munker (CERN), Pixel 2018 (Taipei - Dec 2018)



Significantly faster charge collection for design with additional p-implant and gap in n-layer

New prototypes with both type of further process modifications are presently being tested