DEPFET for tracking applications
(actually all about Belle II PXD was said already)

- An attempt to look into the future -
DEPFET Basics

(J. Kemmer, G. Lutz, 1987)

- fully depleted sensitive volume
- internal amplification
- Charge collection in "off" state, non-destructive read-out on demand
- Pixel size and sensor thickness scalable in wide range (20 µm .. ~1000 µm)
- CCE and noise independent on size and thickness
$g_q = \frac{dI_D}{dQ} = \frac{g_m}{C_{ox}}$

$I_D \sim \frac{1}{L^{1/2}} \quad g_q \sim \frac{1}{W^{1/2}} \quad g_q \sim t_{ox}^{1/2} \quad g_q \sim I_D^{1/2}$

(Ideal transistor theory - neglecting short channel effects)

$g_q$ for of the latest DEPFET generation (large Belle II sensors): $\sim 0.5 \text{ nA/e}$
improving $g_q$

- Better $g_q$ by reducing L (obvious)
  - Limitation by avalanche generation at Drain
  - Higher noise, loose S/N

- Next generation of DEPFETs (A. Bähr)
  - Shaping of drain implant to reduce el. Field

- Possible improvement (simulation)
  - 500 pA/e- $\rightarrow$ 2000 pA/e- (L~1µm)

- Test project for next generation DEPFETs scheduled
  - Various L, implant parameters, improving litho ...
  - **DEPFETs with “SuperGq” soon available**

- Better $g_q$:
  - better S/N $\rightarrow$ spectroscopic applications (ENC>1e-)
  - Higher signal $\rightarrow$ always good
Opportunities – simple scaling

Better $g_q$ means in tracking applications
- Higher MIP signal → **thinner sensitive area**
- Smaller bias current → **less power in pixel area** $g_q \sim I_D^{1/2}$
- Thinner gate isolator → **higher radiation tolerance**

Effect of TID on DEPFET operation → threshold voltage shift of the external gate
- Has to be compensated, i.e. $V_{gate}$ (and Clear_gate) need adjustment with increasing TID
- In principle no problem, performance of the sensors changes only marginally

As an example:
- Reduce $L$ and $t_{ox}$ by 2x → $g_q$ is 2x better
- At the same time $\Delta V_{th}$ is 4x better

\[
g_q \sim \sqrt{\frac{t_{ox}}{L^3}}, \quad \Delta V_{th} \sim t_{ox}^2
\]
Speed considerations

- DEPFET sensor is operated in rolling shutter modus (read-clear ... )
  - Minimize power consumption in sensitive area
  - ~0.5 W (1000 pixels on) in sensitive area
  - ~1 W for the Switchers
  - ~7.5 W at end-of-stave (mostly ADCs of DCD)

- The price to pay is speed
  - PXD has 192 gate lines (four-fold), read in 20µs → ~100 ns for read-clear cycle

- Speed improvement possible with faster processing for each row ("gate")
  - ASIC related limitations → faster ADCs possible (parallel processing), also reduction of bits (binary?)
    - Currently we have 8 bits → better resolution than just binary read-out
  - Settling time of signals on matrix → faster switcher & reduce RC constants on matrix (metal system)

- Overall, in this configuration, an improvement of **more than 2x or 3x not realistic**

- **Is this the end? Or can we change something on the module?**
We don’t want to change too much, actually

a) oxidation and back side implant of top wafer

Top Wafer

Handle <100> Wafer

b) wafer bonding and grinding/polishing of top wafer

c) process → passivation

open backside passivation

d) anisotropic deep etching opens "windows" in handle wafer
The basic idea – evolution rather than revolution

PXD2019
- 1000 DCD channels
- 192 SWB channels

90° turn: 3x speed
- 3072 DCD channels
- 62 SWB channels

2x smaller pixels in Z another 2x occupancy
- 6144 DCD channels
- 62 SWB channels

Another 2x possible with faster DCD! \( \rightarrow \) 12x improvement in occupancy, \( \sim 3\mu s \) per frame in reach
What do we need for this?

- Improve DEPFET pixel cell
  - Higher $g_q$ ....

- Improvement of the metal system on the module
  - technology development planarization (started)
  - 3rd Alu layer on module
  - Possibly 2nd Cu layer

- New ASICs → go for the best available technology – profit from huge micro-electronics industry
  - DCD: smaller, more channels, less ADC bits, faster, driving capability .... → has to be slim, thin, small bump pitch ...
  - SWB: improved driving capabilities, more channels .. → has to be thin, small bumps (material)
  - Do we need a module controller chip (off-module driver, sequencer ..)

- Assembly
  - Basically business as usual, bit of R&D for flip chipping of thin ASICs to balcony and thin sensitive region
  - Technology is under control

- Need to refine the concept, discuss, define R&D steps ... we are not starting from scratch!

- One important part already quite advanced ...
A spin-off of SOI approach: thinned all-silicon module with integ. cooling

- idea: integrate channels into handle wafer beneath the ASICs
- channels etched before wafer bonding → cavity SOI (C-SOI)
  - Wafer bonding being installed at HLL → independent supply and design
- full processing on C-SOI, thinning of sensitive area
- micro-channels accessible only after cutting

Small team within DEPFET PXD: Bonn, HLL, IFIC
- 2nd iteration already, spare you with details for now.. See following talks
Material assessment of possible all-silicon module

Design of current PXD modules with moderate changes

- Balcony wider for DCDs: 5 mm
- Thinner sensitive area: 50 µm and 30 µm
- Frame in standard thickness 450 µm (was 525 µm for PXD)
- Copper 100% on balcony and 10% in sensitive area: 5 µm
- 10k bumps on balcony
- DCDs thinned to 100 µm and 50 µm
- "Sub-millimeter channels" in balcony with H2O or He(?)

- H2O cooling,
- 100 µm DCD,
- 50 µm DEPFET

He cooling,
- 50 µm DCD,
- 30 µm DEPFET

Total: 0.15 %X₀

Total: 0.22 %X₀

Total: 0.20 %X₀
In Summary

- **Belle II PXD: the first full vertex detector based on DEPFETs!**
  - Overall performance of the modules meets the requirements at SuperKEKB
  - Many lessons learned
    - One of the most important ones: have to make the system more user friendly!

- **New DEPFETs with improved properties in the pipeline**
  - Higher amplification ($g_q$)
  - More radiation tolerant
    - Thinner gate dielectrics
    - Thinner bulk $\rightarrow$ higher doping $\rightarrow$ inversion point towards higher NIEL dose

- **Changing the read-out direction** together with the design of new read-out and steering ASICs could meet the requirements at an factor 5 upgraded SuperKEB (background, rad. tolerance)

- **Deployment of micro-channel cooling** opens the way to an highly integrated module with better performance and with an even smaller material budget