DMAPS DEVM'TS IN LFOUNDRY & TOWERJAZZ

NORBERT WERMES (UNIVERSITY OF BONN)

REPRESENTING (FOR THE DESIGNS)

BONN, CERN, CPPM, IRFU/CEA (STILL OPEN) COLLABORATION

wider (still open) collaboration

Birmingham, Glasgow, Oxford, Ljubljana, Milano/Bologna

INTRODUCING DMAPS

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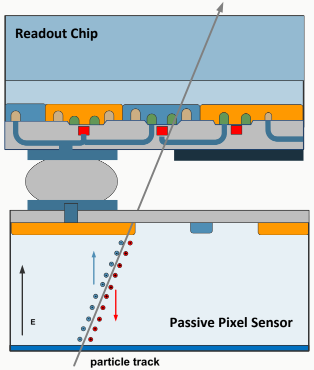
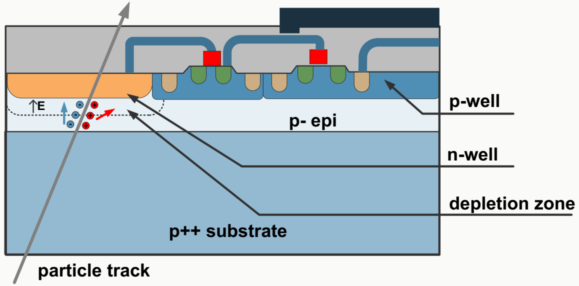
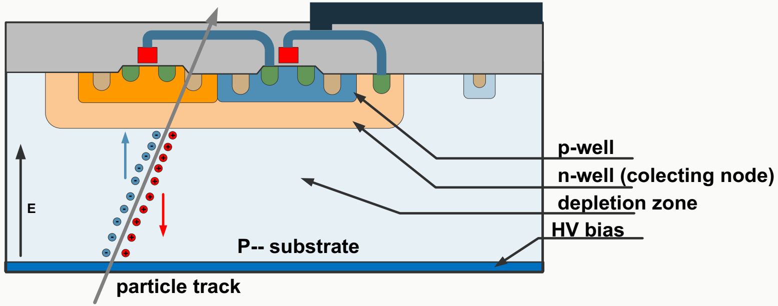
Hybrid detector



MAPS detector



Depleted monolithic active pixel sensor



→ D = depleted via $d \sim \sqrt{\rho \cdot V}$ (> kΩ cm; > 150 V)

→ Easier to produce than hybrid pixels or DEPFET

→ Industrial PROS: much lower module cost, large wafers, fast turn-arounds and large throughput

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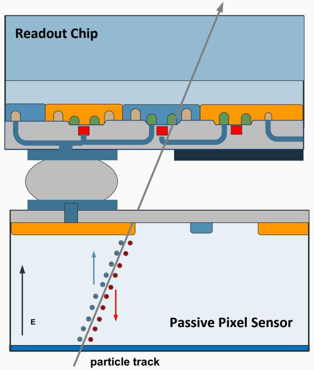

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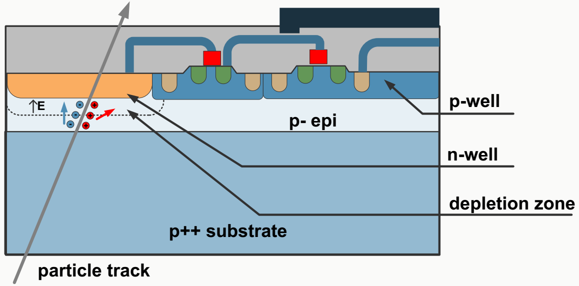

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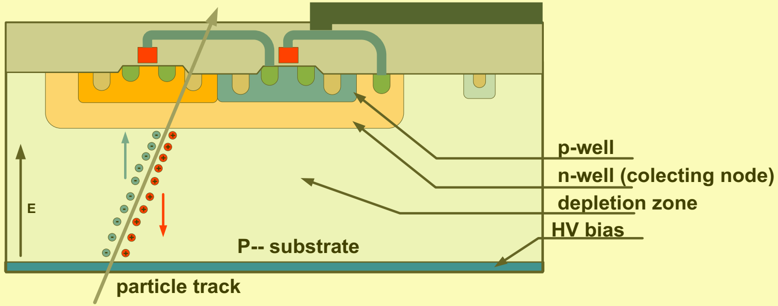

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RATE AND RADIATION LEVELS

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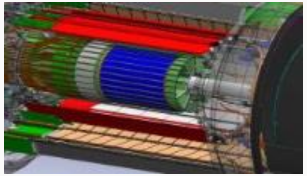
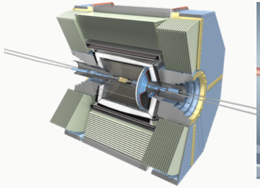
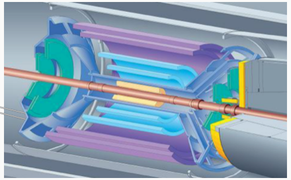
STAR



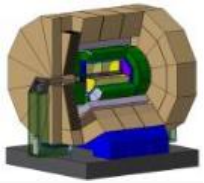
Belle II



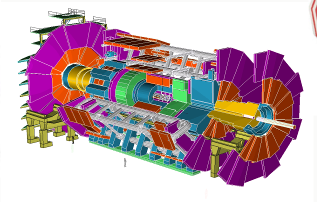
ALICE-(HL)-LHC

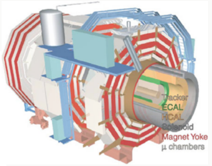


ILC



ATLAS





CMS

	STAR	Belle II	Belle II upgrade	ALICE-LHC heavy ion	ILC	LHC pp	HL-LHC-pp	
							Outer	Inner
BX-time (ns)	110	2	2	20 000	350	25	25	25
Particle Rate (kHz/mm^2)	4	400	1 100	10	250	1 000	> 1 000	> 10 000
Φ (n_{eq}/cm^2)*	> 10^{12}	10^{14}	10^{15}	> 10^{13}	10^{12}	2×10^{15}	1-2 × 10^{15}	2×10^{16}
TID (Mrad)*	0.2	20	500 (?)	0.7	0.4	80	100	> 1000

*per (assumed) lifetime
LHC, HL-LHC: 7 years
ILC: 10 years
Belle II: 5 years

in need for
- much less material (0.1 % X_0)
- higher resolution (< 5 µm)

RATE AND RADIATION LEVELS

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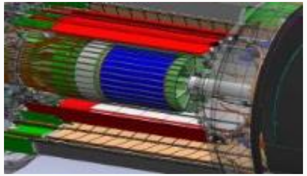

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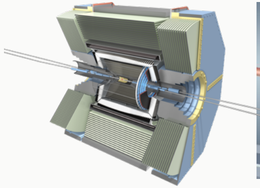

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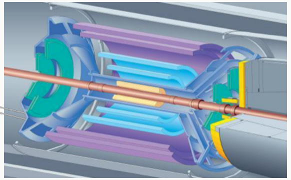

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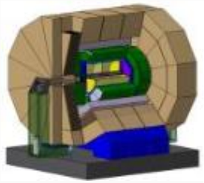

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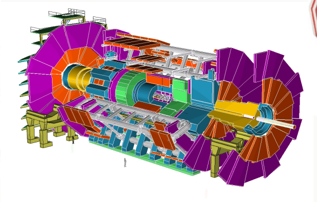

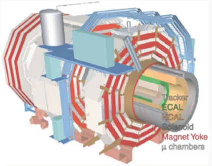

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TWO APPROACHES FOLLOWED (NOTHING SPECIAL ABOUT FABS)

another large FF design shown by Ivan

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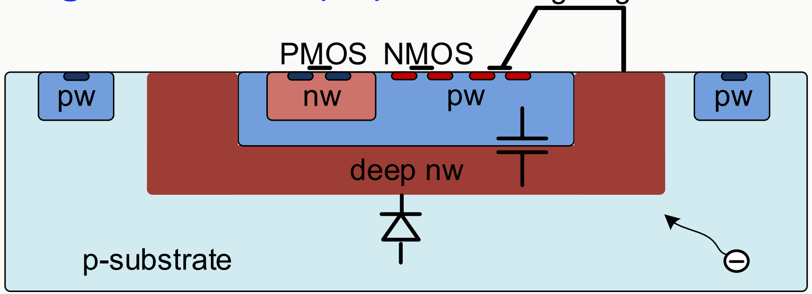
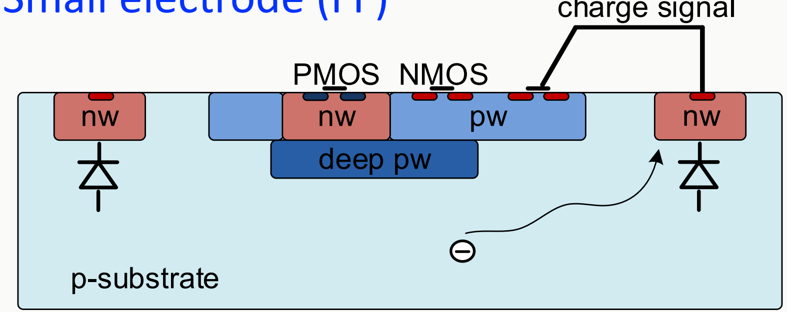
Large electrode (FF)



Small electrode (FF)



Electronics **inside** charge collection well

- **large fill factor** (better: large collection electrode)
  → no low field regions
  → on average **short(er) drift** distances
  → less trapping -> **radiation hard**
- **Larger (>100 fF)** sensor **capacitance**
- **additional well-well capacitance** (>100 fF)
  → noise & speed/power penalties
  → possible x-talk (digital to sensor)

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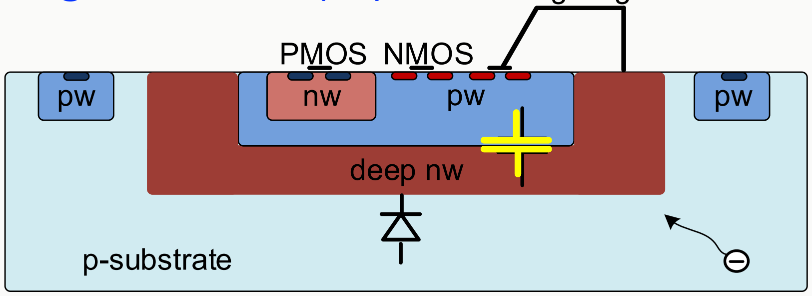

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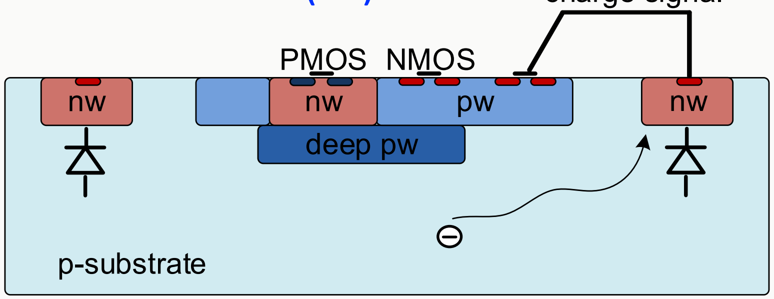

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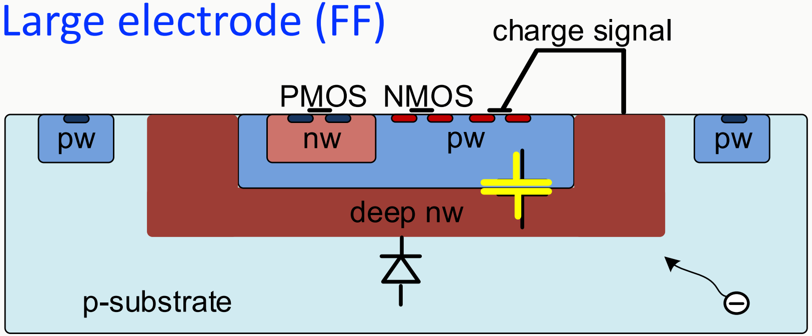

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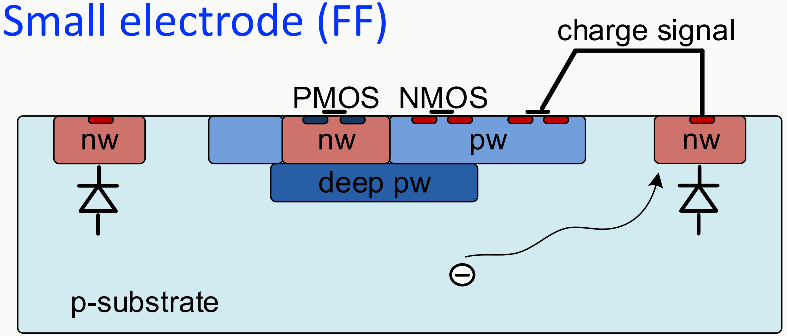

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$$ENC^2_{\mathrm{thermal}} \approx \frac{4}{3}\frac{kT}{g_m}\frac{C}{\tau_f}$$

power

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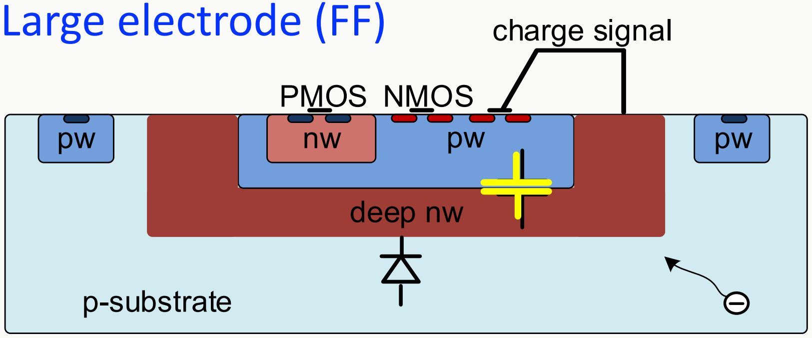

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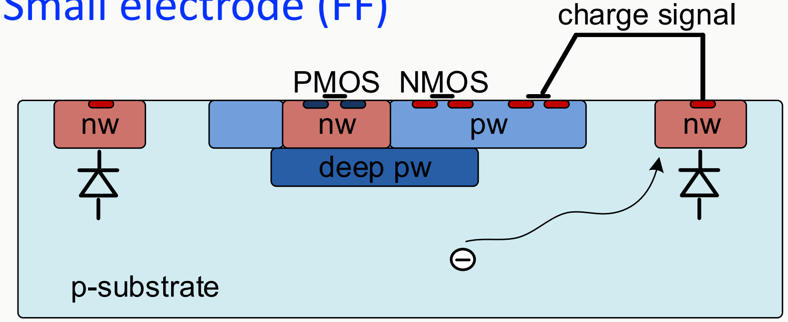

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power

Electronics **outside** charge collection well

- **small fill factor**
  → **very small sensor capacitance (< 5fF)**
  → noise low, speed high, power low
- on average longer drift distances and low field regions possible
  → **radhard hardness needs technology "improvements"**

PROCESS MODIFICATION – TOWERJAZZ 180 NM CMOS

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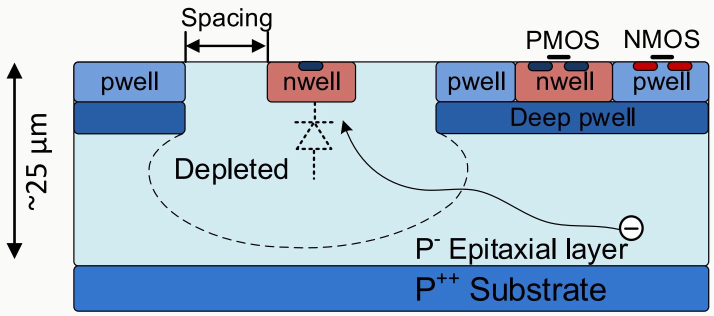
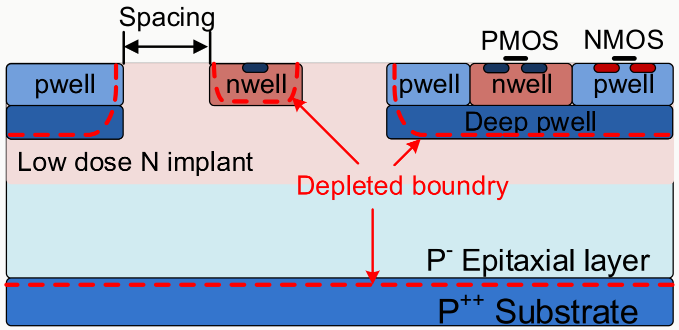


Standard process

- **ALICE ITS type**
- **High res.** **p**-type epi. (> 1 kΩ·cm)
  => thickness typ. **25 µm**
- Quadruple-well
  => deep pwell shields nwell => **full CMOS**
- **Reverse bias** typ. -6V
  => enhanced (but not yet full) depletion
  => some charge collected by diffusion only => slow



Modified process

- Additional planar medium dose **N implant**
  => depletion from two junction boundaries
  full volume can be depleted
  better charge collection in lateral direction
- Maintain small capacitance
- No significant circuit/layout changes

W. Snoeys et al. DOI: 10.1016/j.nima.2017.07.046

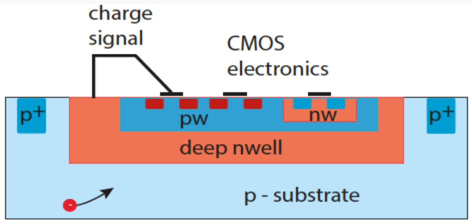
Different electrode (large/small) approaches lead to different

DMAPS

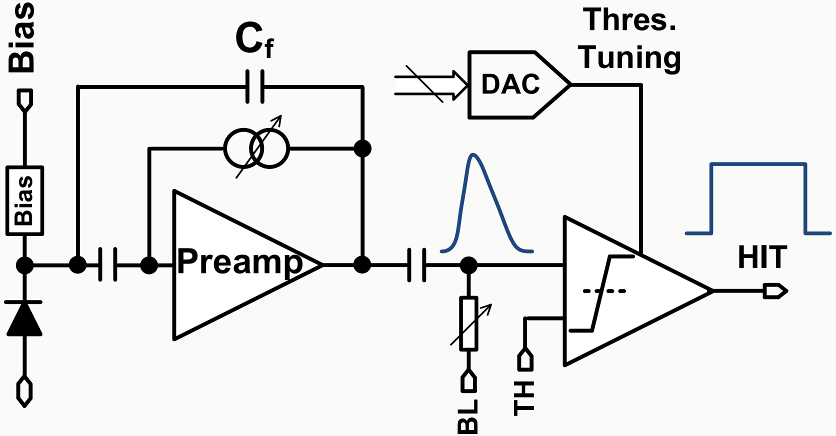
ANALOG FRONT ENDS (CHOICES)

ANALOG FRONT-ENDS - CSA VS. VOLTAGE AMPLIFIER

- large electrode



(a) Large fill-factor

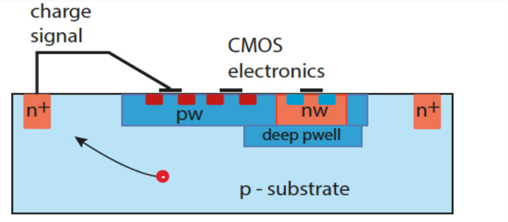


Charge Sensitive Amplifier

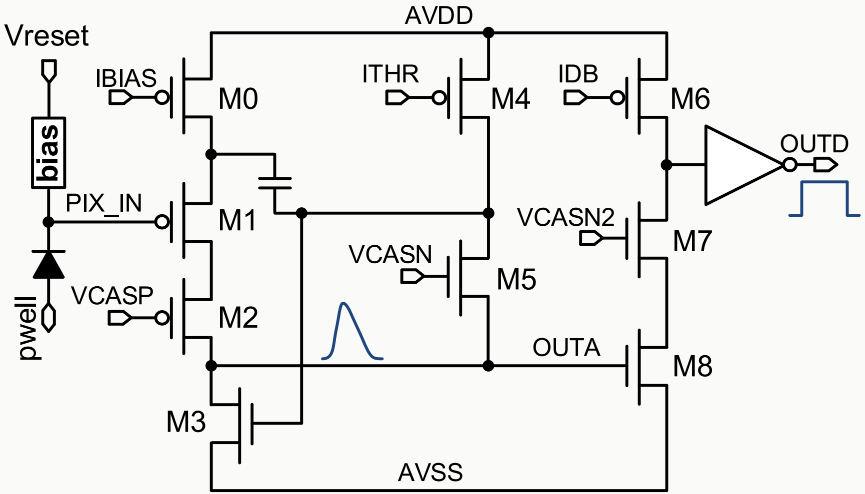
- Used for large electrode design
- Gain (ideally) independent of C_D
  => $g \sim 1/C_f$ (typ. $C_f \sim$ fF)
- $\tau_{CSA} \propto \frac{C_D}{g_m \cdot C_f}$, $ENC^2{}_{therm} \propto \frac{kT}{g_m} \frac{C_D^2}{\tau}$
  => need larger g_m (power) for large C_D
  => typ. power 10 – 20 µW per pixel
- In-pixel threshold tuning needed

ANALOG FRONT-ENDS - CSA VS. VOLTAGE AMPLIFIER

- small electrode



(b) Small fill-factor



D. Kim et al., doi 10.1088/1748-0221/11/02/C02042

<u>Voltage amplifier</u>

=> Profit from small sensor capacitance

=> large voltage signal @ input node

- Very compact design
  - => amplification + shaping in one stage
  - => simple inverter as discriminator
- Optimized power for required timing
  - => ~1 µW/pixel for 25 ns peaking time

DMAPS

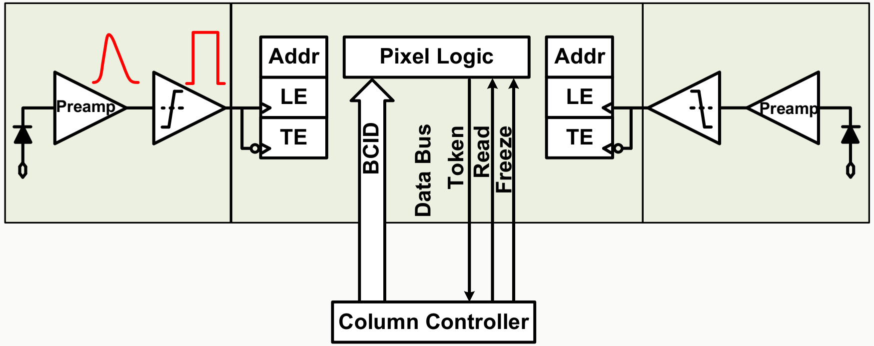
READOUT ARCHITECTURE CHOICES

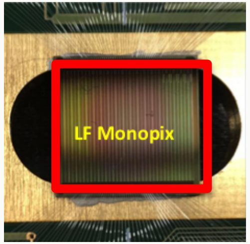
needed

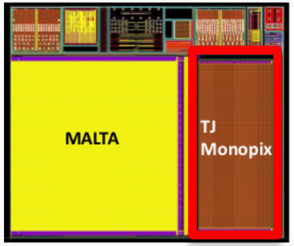
- Small pixels
- High logic (memory) density
- Fast shaping
- High data transmission bandwidth

DMAPS: COLUMN DRAIN ARCHITECTURE

DMAPS with synchronous readout => time stamping in matrix







- Well established scheme in ATLAS – FE-I3 like (current pixel detector)
  => sufficient rate capability for ITk outer and Belle II Upgrade
- Time reference (BCID) distributed in the matrix (small skew req.)
- ToA (arrival) & ToT (charge) recorded in pixel
- Hits read out following a token passing scheme on shared column bus
- In-pixel memories and digital R/O logic

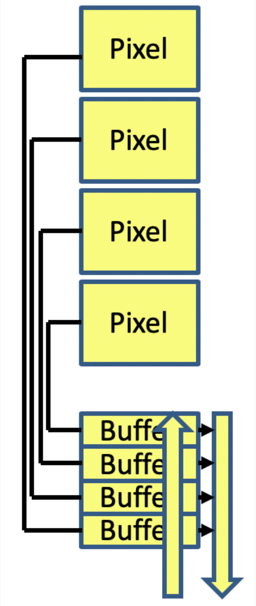
  challenges: prevent digital cross talk, pixel size, C_D (for large electrode design)

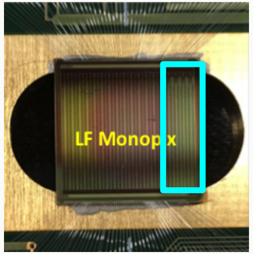
ASYNCHRONOUS READOUT SCHEMES

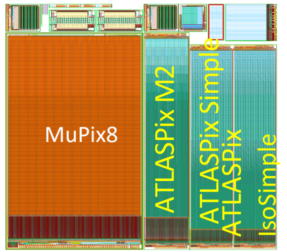
DMAPS with asynchronous matrix => time stamping at periphery

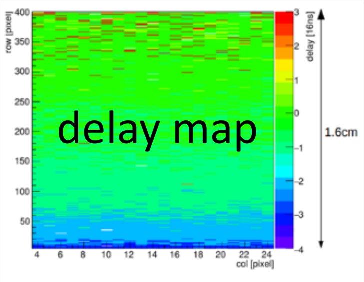
=> Hits transferred to periphery immediately => calls for massive parallelism

A) One to one connection



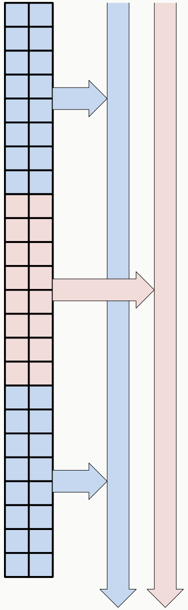


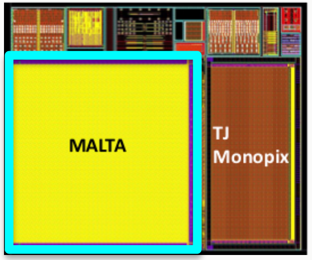




400 lines in two metal layers; larger periphery

B) Shared bus by pixel groups





- Two high speed buses w/ short pulses (~1ns)
- Complicated balancing for multibit data to arrive simultaneously at bottom
- GHz synchronization needed

- Challenge: avoid data collisions

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DEVELOPMENT LINES

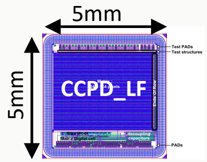
LARGE FF

REALISED IN LFOUNDRY 150 NM

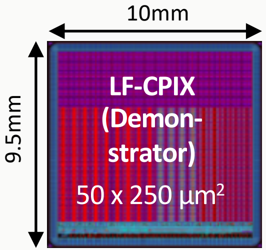
SMALL FF

REALISED IN TOWERJAZZ 180 NM

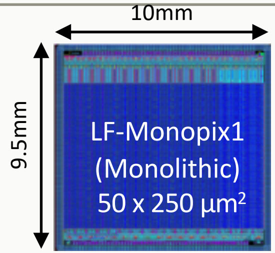
DEVELOPMENT LINES



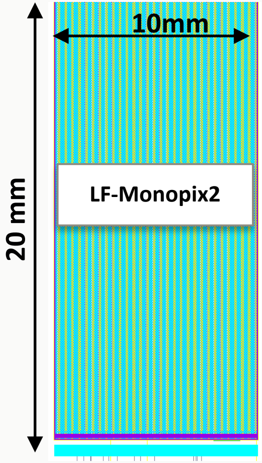
CCPD_LF
- *Subm. **Sep. 2014***
- *Fast R/O coupled to FE-I4*



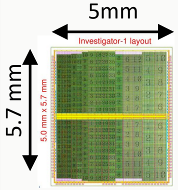
LF-CPIX (DEMO)
- *Subm. **Mar. 2016***
- *Fast R/O coupled to FE-I4*



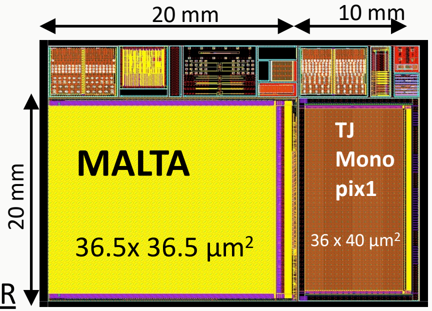
LF-Monopix1
- *Subm. **Aug. 2016***
- *Fast column drain R/O*



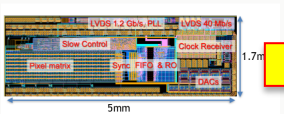
LF-Monopix2
- *subm. **Oct. 2019***
- *50 x 150 μm² pixels*
- *Full height matrix*
- *Fast column drain R/O*



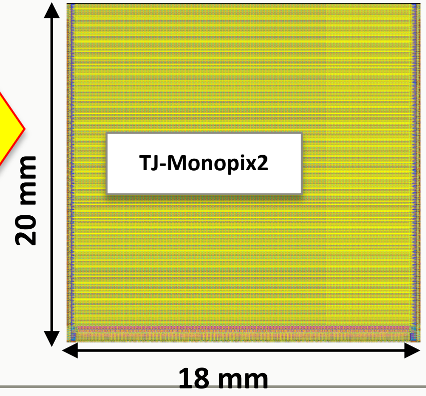
INVESTIGATOR
- ***2016***
- 8 x 8 pixel submatrices



MALTA (asynchronous) & TJ-Monopix1 (column drain)
- subm. **2018**
- large matrices
- fast asynchr & col. drain R/O



miniMALTA
- subm. **2018**
- measures for rad. hardness



TJ-Monopix2
- *subm. **Oct. 2019***
- *33 x 33 μm² pixels*
- *Full height matrix*
- *Fast column drain R/O*

RESULTS ON LARGE FF

LFOUNDRY 150 NM DESIGNS

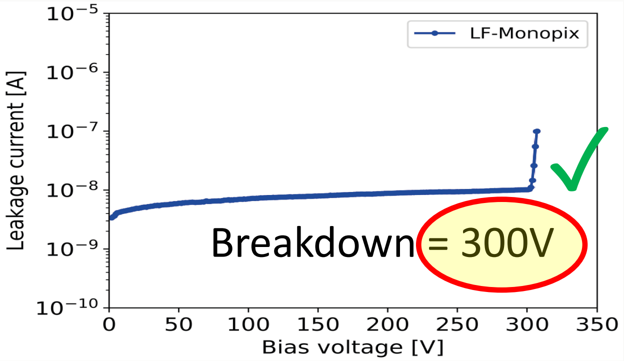
LFA150:

- LFoundry **150 nm** process (deep N-well/P-well)
- **Quadrupel** well
- 7 metal layers
- Resistivity **> 2 kΩ·cm**
- Small implant customization possible
- Backside processing
- Voltages > **350 V**

SENSOR IRRADIATION PERFORMANCE

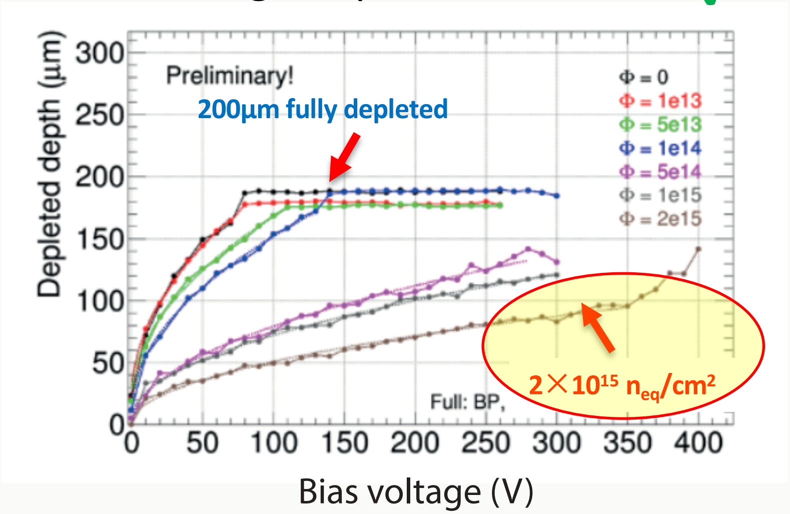
- Large depletion volume after radiation proven in various prototypes

❑ LF-MonoPix



T. Hirono et al., DOI: 10.1016/j.nima.2016.01.088
P. Rymaszewski et al., DOI: 10.1088/1748-0221/11/02/C02045
D.-L. Pohl, et al., DOI: 10.1088/1748-0221/12/06/P06020

❑ large depletion volume ✓

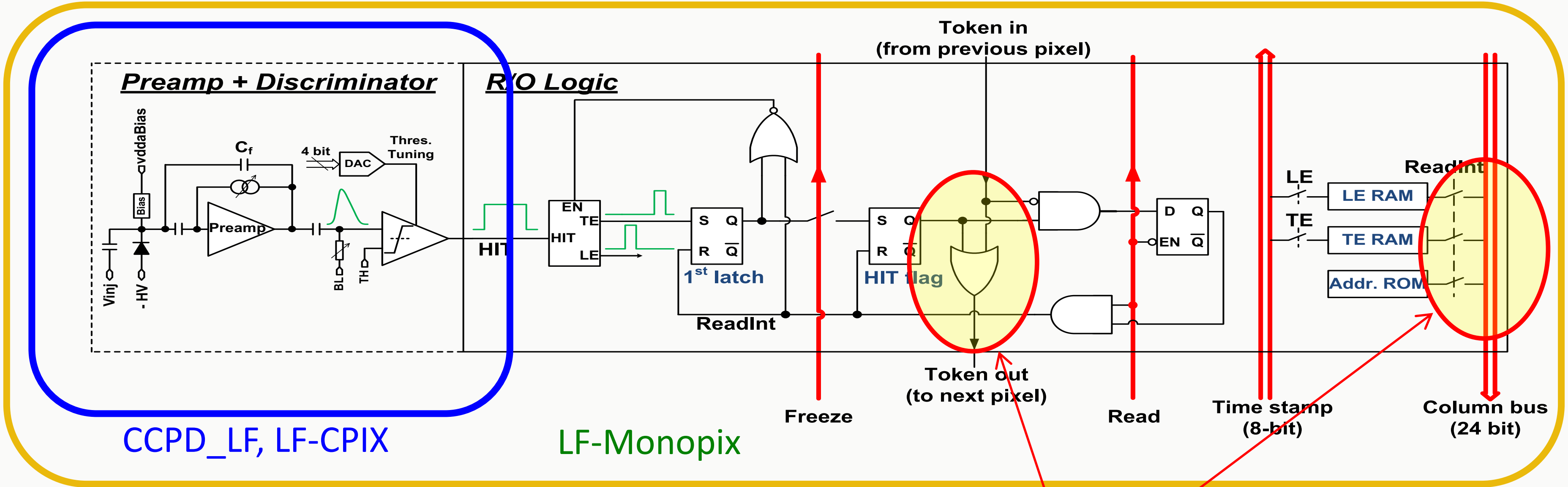


I.Mandić, et al., DOI: 10.1016/j.nima.2018.06.062

Full depletion voltage @ 100 µm:

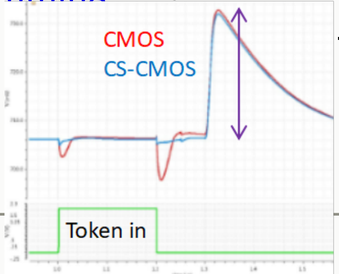
unirradiated	V_{dep} = **7 V**,
irradiated	V_{dep} = **130 V**

PIXEL DESIGN AND CROSS TALK MITIGATION



- Charge sensitive amplifier
- In-pixel 4-bit DAC for threshold trimming
- Hit register (1-bit counter)
- 8-bit time stamp @ 40 MHz
  - *Time, charge of signal*

Output of CSA



- Full-custom dig. circuit
  - *Minimized area* **=>** *for less C_d*
  - *Low noise circuit design for critical dig. blocks*

eg. current steering logic, Source follower readout of SRAMs

mitigation works ✓

RADIATION HARDNESS (TID & NIEL)

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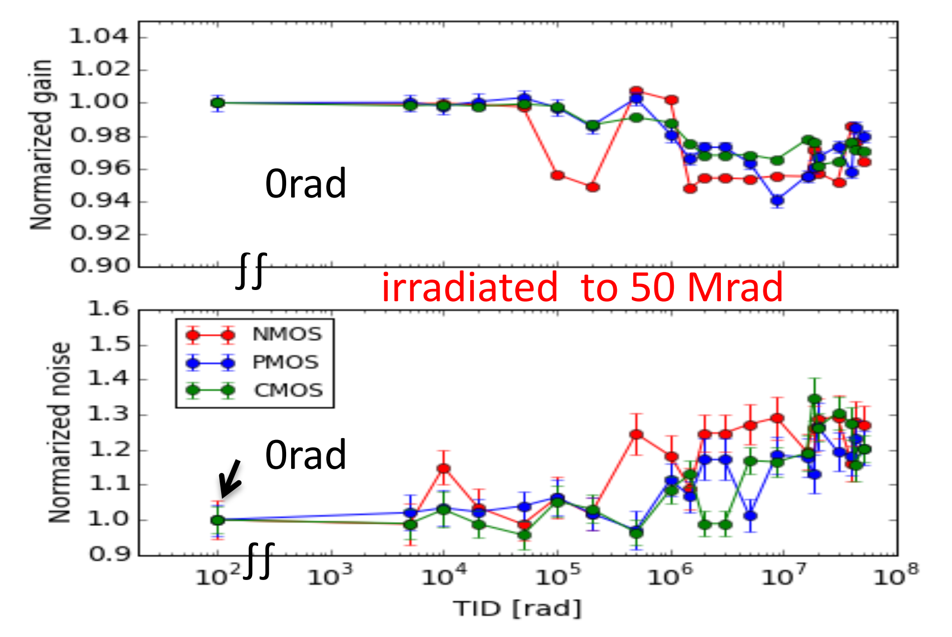
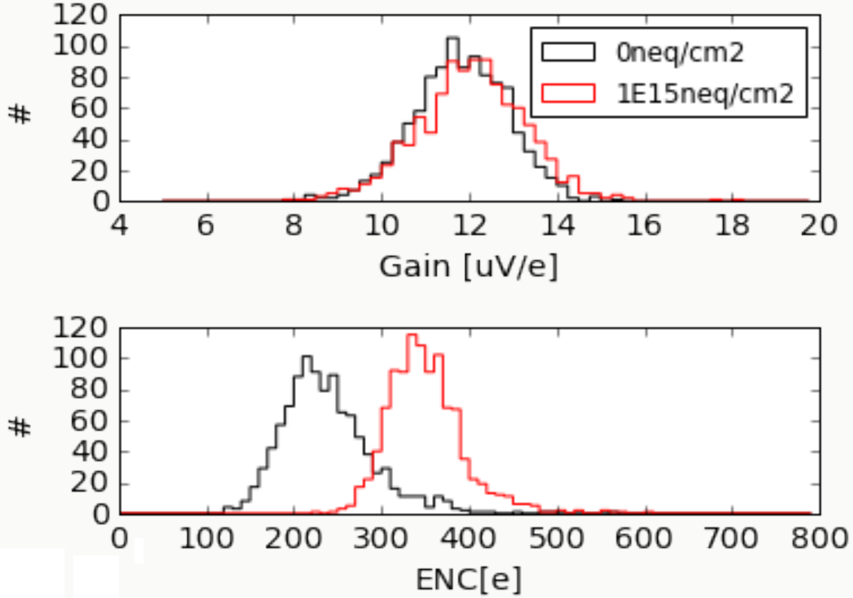
TID

NIEL

e.g. gain and noise





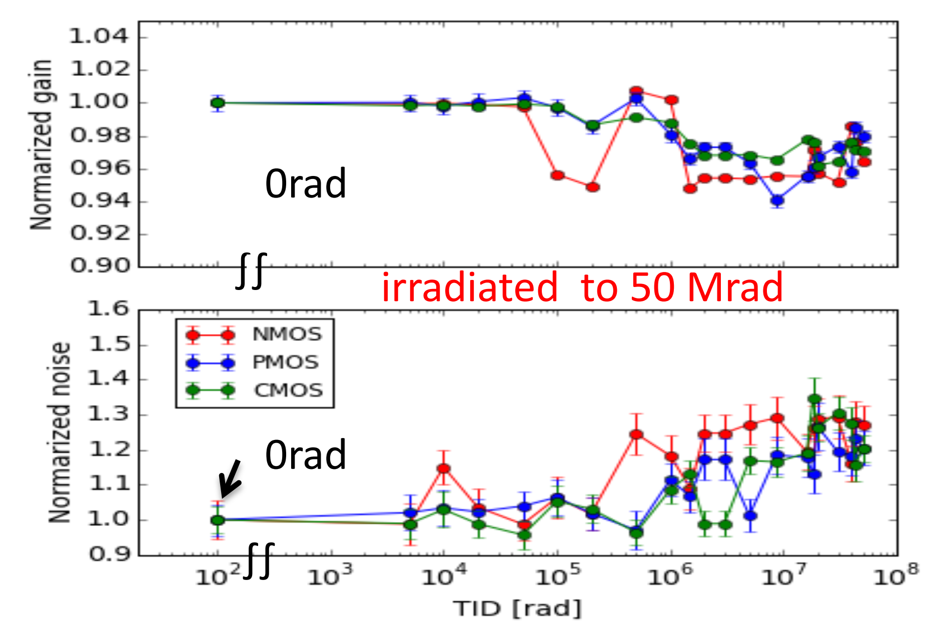
Breakdown voltage is larger than 200V

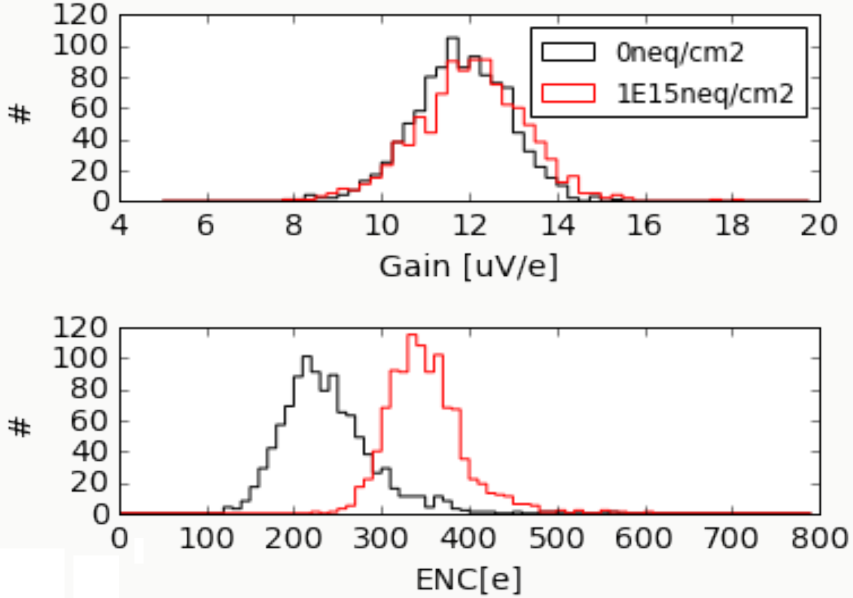
T. Hirono, et al., DOI: 10.1016/j.nima.2018.10.059

RADIATION HARDNESS (TID & NIEL)

TID ✓ NIEL ✓

e.g. gain and noise





Breakdown voltage is larger than 200V

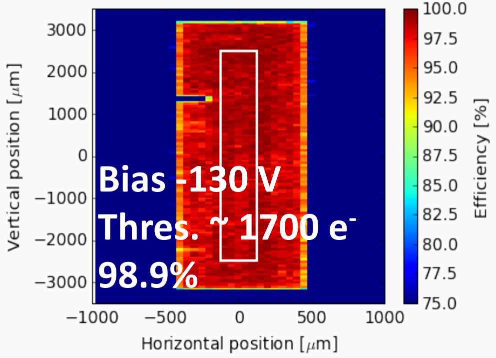
T. Hirono, et al., DOI: 10.1016/j.nima.2018.10.059

RESULTS – LF-MONOPIX

- High bias voltage > 200 V => large depletion + high field
- High and uniform efficiency even after irradiation @ very low noise occ. < 10^{-8}/25ns/pixel
- Promising timing characteristics (still improvable by changed biasing + thinning)

overall eff

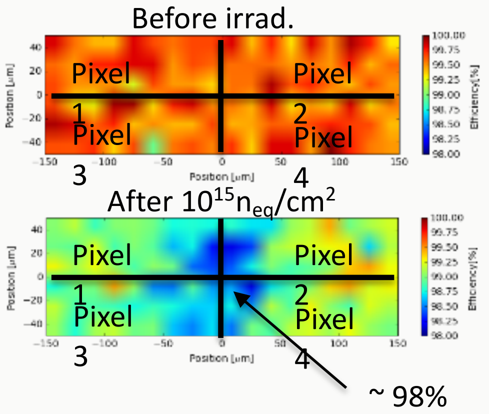
After $10^{15} n_{eq}/cm^2$ (neutron)



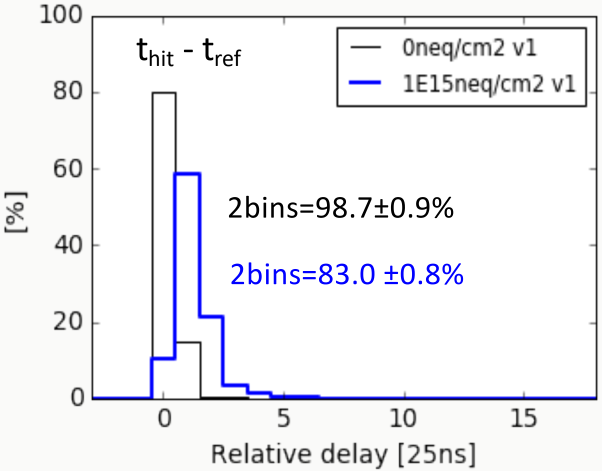
@ Noise occ. < 10^{-8}, thr~1700e-

T. Hirono, et. al, DOI: 10.1016/j.nima.2018.10.059

in-pixel eff



timing



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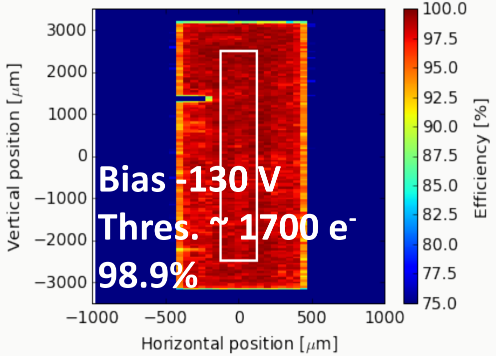

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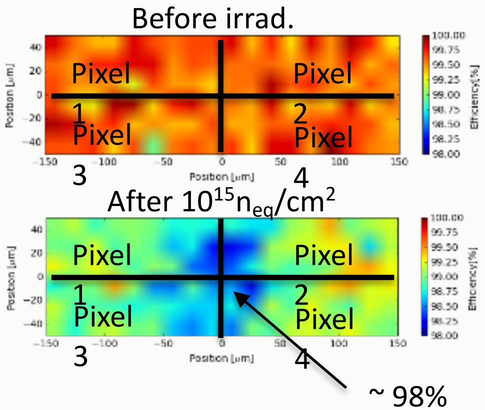
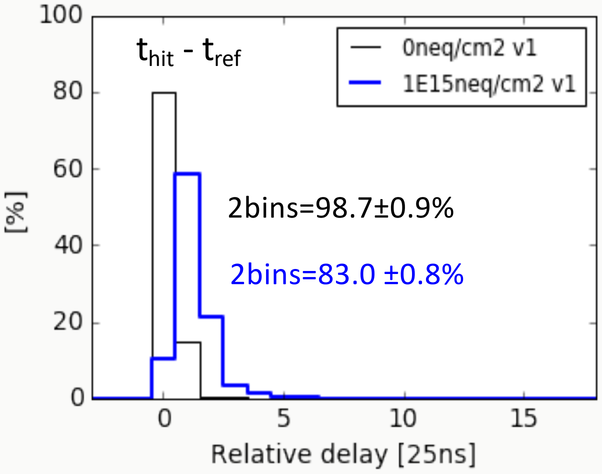
T. Hirono, et. al, DOI: 10.1016/j.nima.2018.10.059

in-pixel eff ✓



timing



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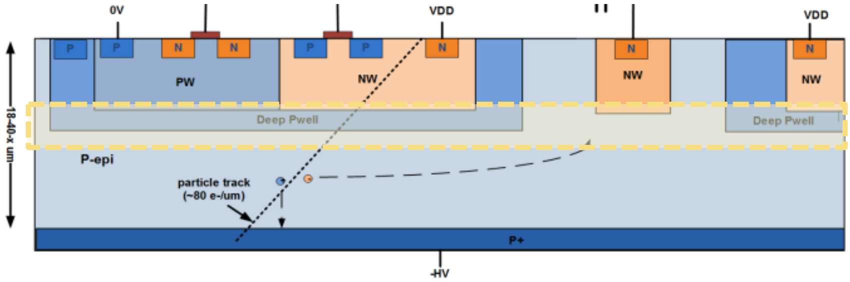
RESULTS ON SMALL FF

TOWERJAZZ 180 NM DESIGNS

TJ – MALTA & MONOPIX



- **TowerJazz** 180 nm CMOS CIS
- Deep Pwell allows full CMOS in pixel
- Gate oxide 3 nm good for TID
- Thickness: 18 – 40 µm
- High resistivity: 1 – 8 k Ohm-cm
- Reverse substrate bias
- **Modified process** to improve lateral depletion
- Derived from ALICE development (CERN)

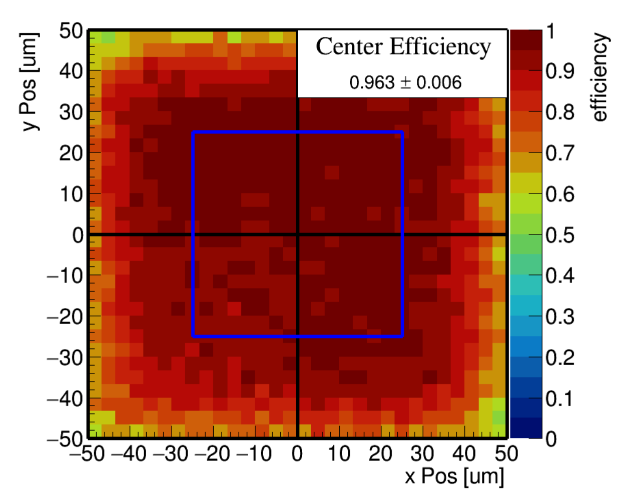
Design: CERN (MALTA), Bonn (MONOPIX)

SMALL ELECTRODE AND RADIATION TOLERANCE

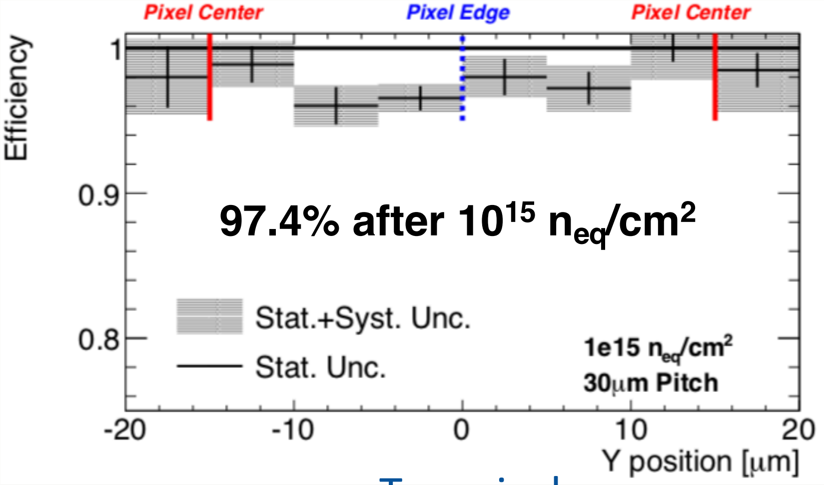
"Investigator" chip to investigate modified technology

H. Pernegger et al., JINST 12 (2017) no.06, P06008

50x50 µm pixel pitch,
3µm electrode,
40µm opening



30x30µm pixel pitch,
3µm electrode
9µm opening

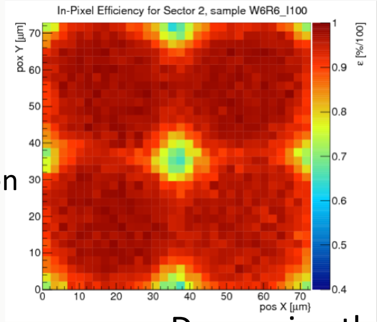


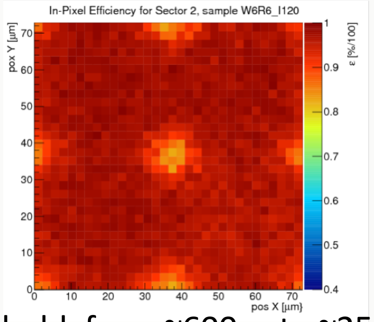
Two pixels

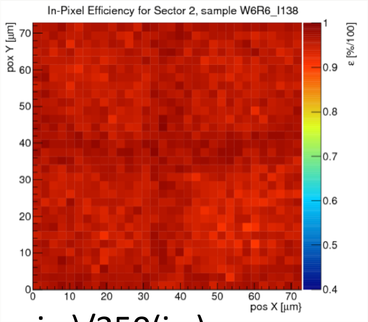
RESULTS – MALTA & TJ-MONOPIX

- Low corner efficiency, especially after irradiation

MALTA
Before irradiation

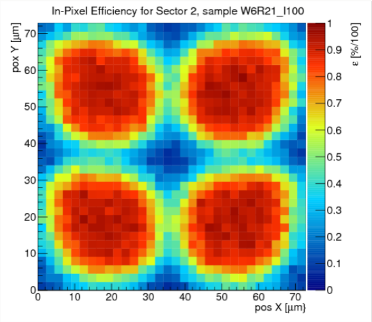


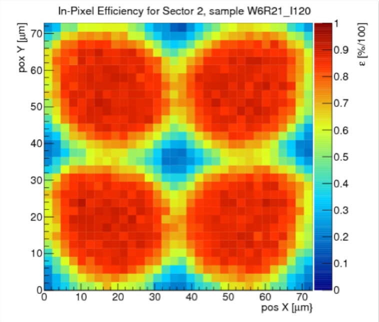




Decreasing threshold, from ~600 e^- to ~250(unirr)/350(irr) e^-

MALTA
Irradiated
5 x10^{14} n_{eq}/cm^2

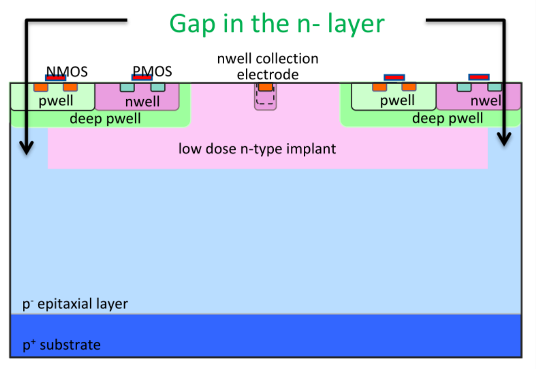


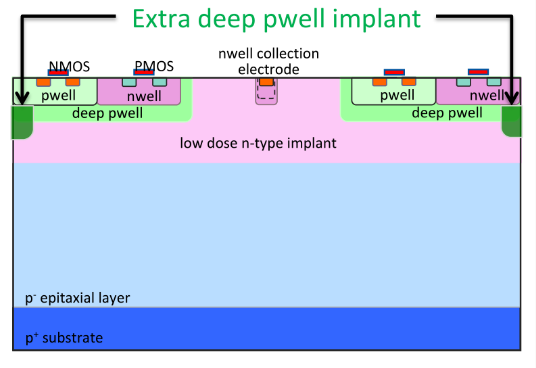


Couldn't reach lower threshold

A. Sharma, et al., Vertex 2018

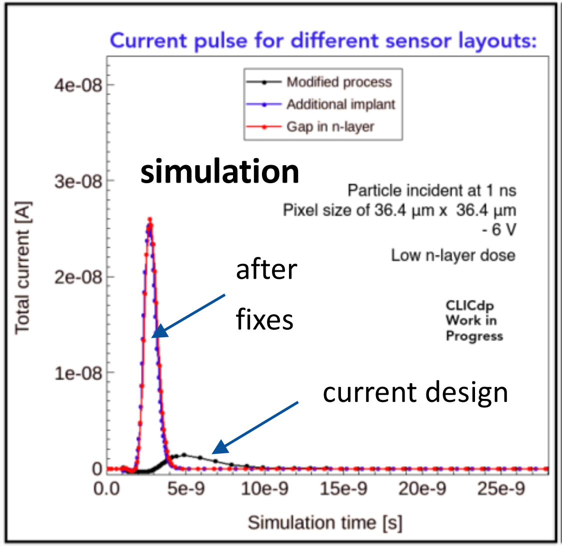
TO IMPROVE CHARGE COLLECTION AFTER IRRADIATION

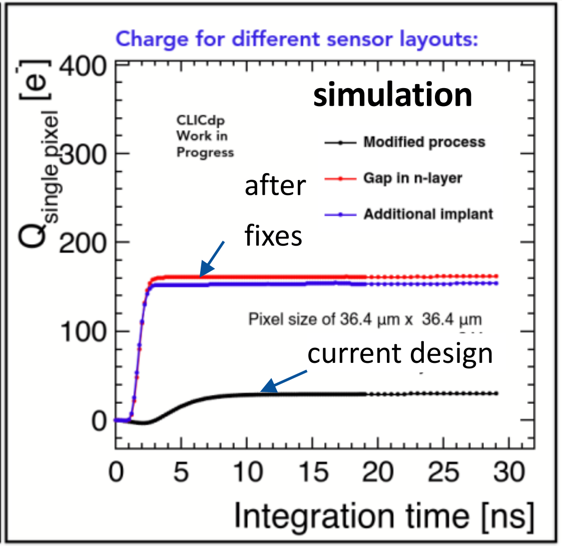




T. Kugathasan et al., VERTEX 2018

TCAD sim. after irrad. ($10^{15} n_{eq}/cm^2$) M. Munker, JINST 14 C05013 (2019)

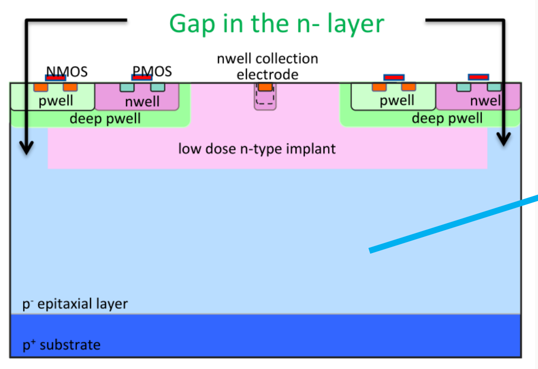


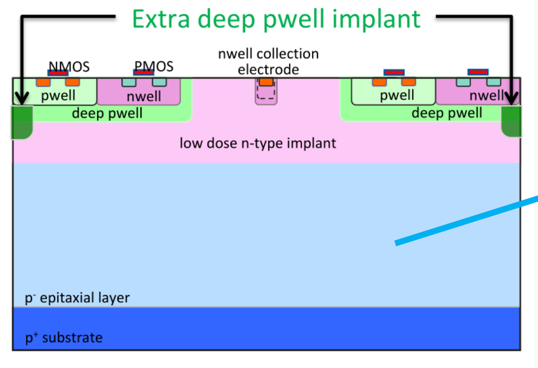


Note: simulation is for "worst case" = particle impinging at pixel corner

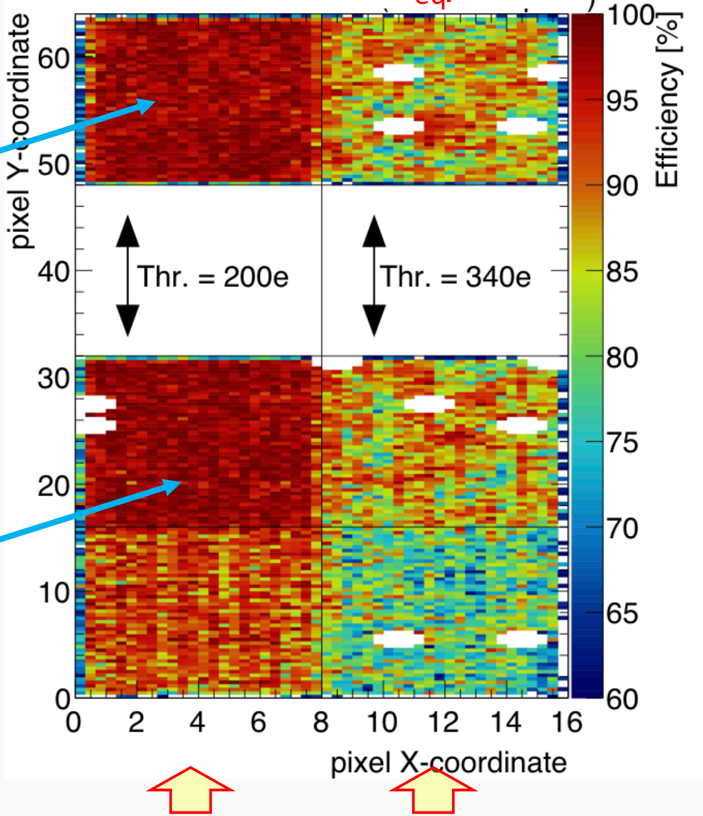
- Simulation shows significantly improved charge collection
- additional measures: better signal to noise/threshold by enlarged transistors with higher gain and lower noise

FIXES TO IMPROVE EFFICIENCY AFTER IRRADIATION





after $1 \times 10^{15}\ n_{eq}/cm^2$



efficiency **> 98%**

with

1. improved Q coll.

plus

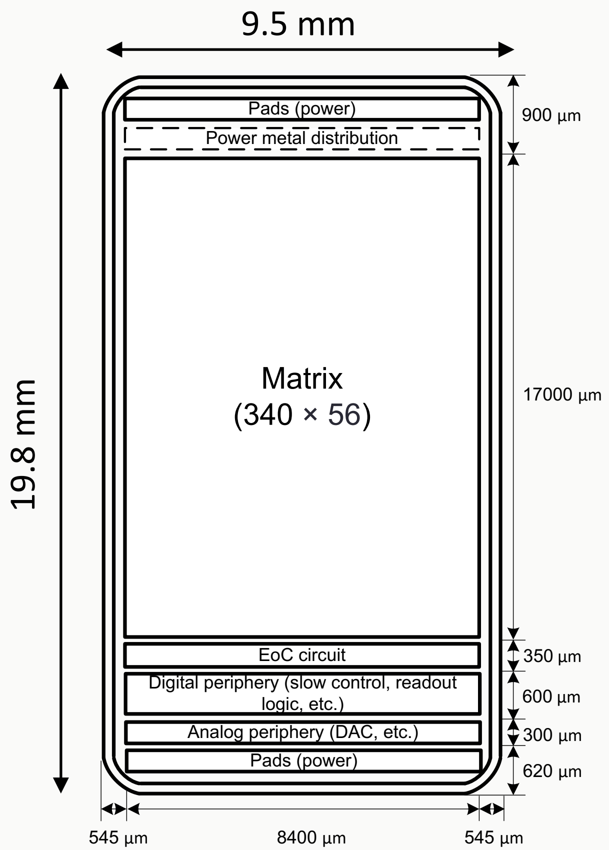
2. improved frontend

enlarged transistors previous size

2019 GENERATION

LF MONOPIX2
TJ MONOPIX2

LFOUNDRY MONOPIX2



	LF-Monopix1	LF-Monopix2
Pixel size	50 × 250 µm²	50 × 150 µm²
Cd	~ 400 fF	~ 300 fF
Analog power/pixel (CSA + Discri.)	15 µA + 5 µA = 20 µA	10 µA + 2 µA = 12 µA
Noise	~150 e⁻ - 200 e⁻	100 ~150 e⁻
LE/TE time stamp	8-bit	6-bit
ToT @ 6 ke⁻	---	200 – 250 ns
Max. ToT	---	400 ns
p-p (rms) thres. dispersion	(~ 100 e⁻)	800 e⁻ (80 e⁻)
Min. threshold	1500 e⁻	1000 e⁻
In-time threshold	~ 2000 e⁻	1500 e⁻

*could become 50 x 110 µm

TOWERJAZZ MONOPIX2

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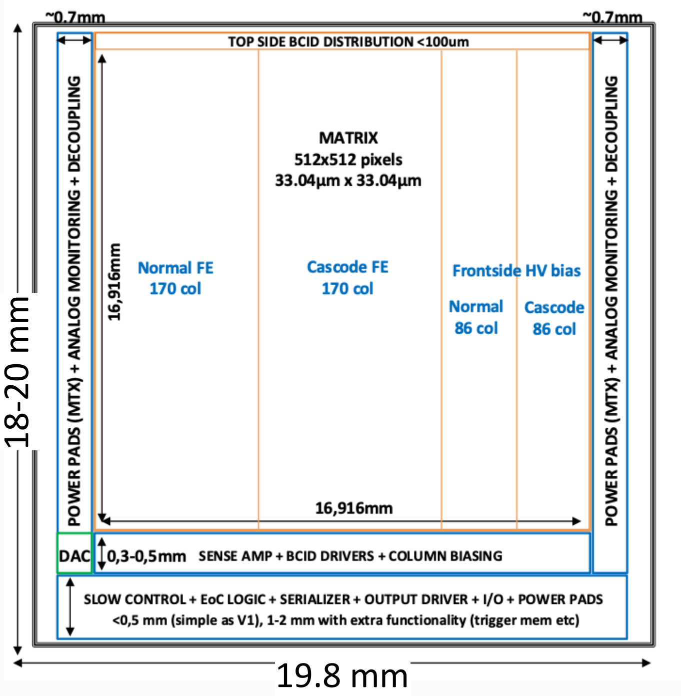

	TJ-Monopix1	TJ-Monopix2
Pixel size	36 × 40 μm²	33.04 × 33.04 μm²
Cd	< 3 fF	< 3 fF
Analog power/pixel (CSA + Discri.)	500 nA + 50 nA (static) = 550 μA	**500 nA + 50 nA (static) = 550 μA**
Noise	~10 e⁻	**< 10e⁻ (improved FE)**
LE/TE time stamp	6-bit	**7-bit**
ToT @ 1 ke⁻	~500ns (depends highly on FE settings)	**1 - 2 us**
Max. ToT	---	~2us (7bit LE)
rms thres. dispersion	~ 30 e⁻ (unirradiated)	**< 20 e⁻ (improved FE + tuning)**
Min. threshold	~ 300 e⁻ (unirradiated)	**< 150 e⁻**
In-time threshold	~ 100 e⁻ overdrive → ~400e⁻	**250 - 300 e⁻**

- **Numbers given in red = target values**

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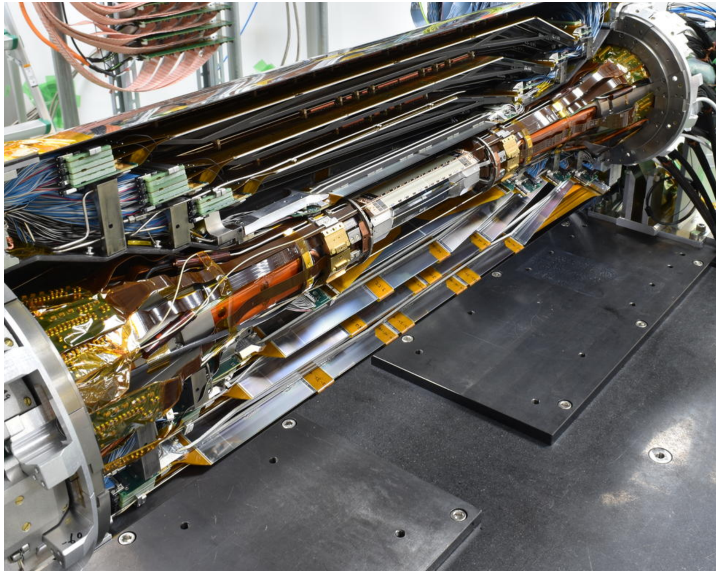
PROPOSE

DMAPS FOR BELLE II



DMAPS FOR BELLE II

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We believe that a small electrode design is well suited for the Belle II upgrade, promising

- optimal pixel size for Belle II (~35 x 35 μm^2)
- low mass modules (~0.1% X_0)
- low power (~0.2 W/cm^2 compared to 1.3 -> 2.5 W/cm^2 for PXD)
- meets TID and NIEL radiation requirements
- time stamping resolution is not a problem (< 50 ns)
- zero suppressed data R/O and high hit and trigger rate capabilities
- triggered output less by 100 ns / 20 µs = 1/200 plus factor 3 from pixel size ratio
- can be built at reasonable cost and fast fabrication turn arounds
- and even has a vendor in sight that may last with HEP for some time

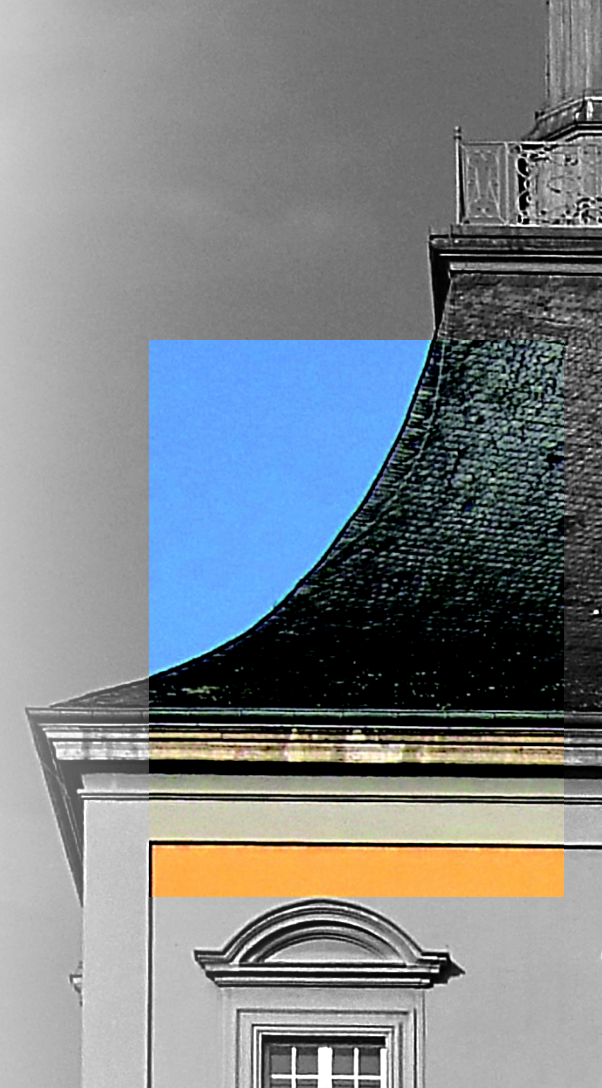
	power (W/cm^2)	x/X_0 (%)	frame time (µs)	trigger rate capability (kHz)	output/mod. (Mbits/s)
PXD -> extrapol.	1.3 -> 2.5	0.21-> 0.1	20 -> 2	30 -> 150	(4->9)×16000
ATLAS outer layer	0.2	0.1	0.025 -> 0.1	4000	4×32 / 1×128

CONCLUSIONS

- Depleted CMOS pixels (DMAPS) combining HV and HR have matured to radhard monolithic pixel devices with high rate capability.

- They can be fabricated
  - fast
  - at comparatively low cost
  - with large throughput
  - and thin

- They are thus well suited for the Belle II Upgrade, especially small pixel, low capacitance designs (small FF)



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