EMBEDDING MICROFLUIDICS INTO MICROELECTRONICS

Alessandro Mapelli

BELLE II VXD OPEN WORKSHOP
8-10 JULY 2019
• **Silicon microchannel cooling plates**
  • NA62 GTK
  • LHCb VELO upgrade

• **Buried channels technology (BCT)**
  • CMOS-compatible BCTs
  • Embedding microchannels into MALTA
  • Transferring BCTs to aerospace
SILICON MICROCHANNEL COOLING PLATES

LHCb VELO LS2 UPGRADE
presented tomorrow by Jan Buytaert

A-A

bonded wafers stack

COLD FLUID IN

wafers with etched microchannels

cover wafer

WARM FLUID OUT

NA62 GIGATRACKER
MICROFABRICATION OF THE GTK COOLING PLATES

- Collaborative effort between CERN groups (ALICE, LHCb, NA62 and EP-DT) and external partners (CSEM, EPFL, TMEC).
- Design by CERN EP-DT
- Prototypes fabricated by CERN EP-DT at EPFL-CMi on 4” wafers
- Pre-production series by IceMOS on 6” wafers
- Three batches fabricated at CEA-Leti on 8” wafers
- Fourth batch is under fabrication for the post-LS2 GTK modules.
**MICROFLUIDIC SYSTEM INTEGRATION**

**Assembly steps:**
- Machining of KOVAR connectors;
- Brazing of connectors to capillaries (1);
- Bending of the capillaries;
- Brazing the other end of the capillaries to the manifolds (2);
- NiAu plating of the connectors;
- Soldering of the connectors to the silicon cooling plate (3);

**QA/QC:**
- After each joining step the He leak rate is measured. (Acceptance leak rate: $10 \times 10^{-10}$ mbar l⁻¹ s⁻¹).
- Pressure testing of the cooling plate at $1.43 \times P_{op}$
NA62 GigaTracker

- Read-out board
- Vacuum flange and feedthrough
- Microfluidic connectors
- Cooling plate
- Hybrid (not shown)
- Manifolds (1/8” to 1/16”)
- 1/16” SS capillaries
- 1/8” SS capillaries

1/8” SS capillaries
NA62 GigaTracker

- Microfluidic connectors
- Cooling plate
- Read-out board
- Vacuum flange and feedthrough
- Hybrid

ALESSANDRO MAPELLI

BELLE II VXVD OPEN WORKSHOP
8-10 July 2019
microfabrication of the VELO cooling plates

Cooling plate

500 µm thick

Microchannels
120 x 200 µm (~260 mm long)
Adiabatic heat changing the CO2 vapor quality (ratio of gas and liquid)

Plasma dicing by DRIE
Deep Reactive Ion Etching

Chang Kun Kang et al 2008 J. Micromech. Microeng. 18 075007
LHCb VELO Upgrade

Pixel sensors
Cooling plate
Read-out circuits
Microfluidic connector
CO\textsubscript{2} capillaries

INVAR connector

NA62

LHCb

21mm

3.6mm
EMBEDDING MICROCHANNELS

• Low-temperature wafer bonding processes.
• Etch the channels into the device and seal them without wafer bonding.
Silicon buried channels for pixel detector cooling

M. Boscardin, P. Conci, M. Crivellari, S. Ronchin, S. Bettarini, F. Bosi

1. ANISOTROPIC ETCHING OF TRENCHES

2. ISOTROPIC ETCHING OF CHANNELS

3. SEALING TRENCHES

Fig. 1. Process sections for longitudinal and transverse channels.

CMOS-COMPATIBLE THREE DIMENSIONAL BURIED CHANNEL TECHNOLOGY (3DBCT)

Phillip Zellner, Liam Renaghan, and Masoud Aghah
VT MEMS Lab, Virginia Polytechnic Institute and State University, Blacksburg, Virginia, USA

Transducers 2009, Denver, CO, USA, June 21-25, 2009

Figure 1: Process flow for 3D buried channels. (Top) Mask layout (1-3) Sealable channels (4) Gradually varying depth design (5) Unsealable mask window for access holes in oxide layer (6) Non-symmetric channels
BURIED CHANNELS TECHNOLOGY (BCT)

ANISOTROPIC ETCHING OF TRENCHES (DRIE)

PASSIVATION

DIRECTIONAL ETCHING OF PASSIVATION

ISOTROPIC ETCHING OF CHANNELS

STRIPPING OF PASSIVATION

SEALING

UNDER ETCHING OF PASSIVATION

POLY-SI
- Closed at the top by poly-Si
- Sharp closing angle

POLY-SI + ETCHED + OXIDATION
- Closed at the bottom by oxide

POLY-SI + OXIDATION
- Closed at the top by poly-Si
- Closed at the bottom by oxide
PRESSURE RESISTANCE

EDMS doc no CERN-0000191313

• **Standard samples** used for the QA/QC of the LHCb and NA62 cooling plates as well as for the investigation of **new fabrication techniques** (bonded wafers, buried channels, 3D-printed devices in plastics, ceramics,...).
BCTs on the backside of MALTA

Riccardo CALLEGARI & Clémentine LIPP

CMOS-compatible post-processing of single dies.

![Diagram showing the process flow for BCTs on the backside of MALTA](image)
MALTA with BCTs

- Single lithography process for microchannels and inlets.
- Maskless lithography on backside of single dies.

FOOTPRINT ~ 20 x 20 mm
PROOF OF PRINCIPLE WITH 3D-PRINTED CONNECTOR

Pressure resistance: ~110 bars
Leak tightness: ~$10^{-8}$ mbar x l /s
PERFORMANCE OF MALTA WITH BCTs

Roberto CARDELLA

**55Fe source scan**
- Peaks fit comparable
- Distance of the peaks within the gain dispersion of MALTA

**Collection Efficiency**
- Readout issue reduced the efficiency of ALL detectors to ~70%
- Comparable efficiency for the different ROIs
glueing a 3D-printed connector on a wire-bonded MALTA with BCTs
TECHNO. TRANSFER TO AEROSPACE

- Innovative Mechanically Pumped loop for Active Antennae
- EU-funded project (H2020) for the development of a novel thermal management system for active antennas in telecommunication satellites.
- CERN was invited to participate by the consortium to bring their expertise on silicon microfluidic evaporators and interfaces to hydraulics and electronics.
- This project will allow CERN to further develop and investigate the Buried Channels Technology for future HEP detectors and upgrades.
CONCLUSIONS & OUTLOOK

• Microfabrication processes developed at CERN
  • to fabricate silicon cooling plates by DRIE and wafer bonding;
  • to embed microchannels on the backside of monolithic pixel detectors.

• Prototypes are fabricated in the class 100 (ISO5) MEMS cleanrooms of the Center for MicroNanotechnology at EPFL.

• Cooling plates for NA62 and LHCb are manufactured at CEA-Leti.

• The first results obtained with MALTA with BCTs do not show any performance degradation.

• Further tests will be performed with MALTA in the coming days.

• An optimised connector for BCTs will be designed and studied in the coming months within the IMPACTA consortium.
BACKUP
SILICON MICROCHANNEL COOLING PLATES

- No CTE mismatch
- Active and distributed cooling
  - Better temperature uniformity across sensor
- Low and uniform material budget
- Radiation resistance
- Great potential for integration
  - Same microfabrication techniques as sensors and microelectronics.
- Thermal Figure of Merit

\[
TFM = \frac{T_{\text{sensor}} - T_{\text{fluid}}}{\text{power density}}
\]

**Fig. 6**

<table>
<thead>
<tr>
<th>Flow [g/s]</th>
<th>TFM</th>
<th>Tsat [°C]</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>~12</td>
<td>~25</td>
</tr>
<tr>
<td>5</td>
<td>~20</td>
<td>~10</td>
</tr>
<tr>
<td>10</td>
<td>~20</td>
<td>~0</td>
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</tbody>
</table>

CO₂ boiling Thermal Figure of Merit (TFM) at constant flow rate 0.3 g/s and various Tsat

Désirée Hellenschmidt, Poster 78, VCI2019

Alessandro Mapelli
NA62 GTK and LHCb VELO Upgrade

<table>
<thead>
<tr>
<th>NA62</th>
<th>LHCb</th>
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<tbody>
<tr>
<td># of modules</td>
<td>3</td>
</tr>
<tr>
<td>distance between modules</td>
<td>~10 m</td>
</tr>
<tr>
<td>sensors</td>
<td>hybrid pixel</td>
</tr>
<tr>
<td>sensor size</td>
<td>60 x 38 mm</td>
</tr>
<tr>
<td>sensors/module</td>
<td>1</td>
</tr>
<tr>
<td>power dissipation (average)</td>
<td>~2 W/cm²</td>
</tr>
<tr>
<td>coolant</td>
<td>liquid C₆F₁₄</td>
</tr>
<tr>
<td>cooling plate thickness</td>
<td>~200 µm</td>
</tr>
<tr>
<td>operating temp. on sensor</td>
<td>-10°C</td>
</tr>
<tr>
<td>max. operating pressure</td>
<td>~10 bars</td>
</tr>
<tr>
<td>safety pressure</td>
<td>~20 bars</td>
</tr>
<tr>
<td>operation in vacuum</td>
<td>primary vacuum of NA62</td>
</tr>
<tr>
<td>distance to beam</td>
<td>in the beam axis</td>
</tr>
</tbody>
</table>

3D schematic drawing of the GTK module

Silicon microchannel cooling plate

Support and alignment structure

Cooling plate

Sensor, silicon pixels (30 x 60 mm)

Silicon microchannel cooling plate

Micro channels 200 µm x 120 µm

Cooling In/outlets

GigaTracker*Module

(12 x 20 mm), heat production ca. 3.2W per chip (2 W/cm²)

Cooling*plate*

Readout*chip*

Sensor,*silicon*pixels

(30 x 60 mm)

Support*and*alignement*structure

Beam*direc=on*
"in-house" microfabrication processes

Process-flow developed at CERN for the first microchannel cooling plates

- pre-etching of through holes
- etching of through holes & microchannels
- anodic bonding of glass cover
- gluing of PEEK connectors


First demonstration of 2-phase CO2 circulation in silicon microchannels

- Power dissipation
  - Digital Power 58 W
  - Analog Power 10 W
- Liquid CuF2
  - 7g/s
  - -10°C at inlet

2 independent networks of 76 microchannels of the hybrid detector
SILICON DIRECT WAFER BONDING

No intermediate layer such as eutectic metals or adhesives for the bonding

Hydrophilic bonding

Hydrophobic bonding

T_{\text{anneal}} = 1050^\circ C
P_{\text{max}} \sim 400 \text{ bars}
delamination + rupture

T_{\text{anneal}} = 1050^\circ C
P_{\text{max}} \sim 700 \text{ bars}
rupture without delamination
**INTEGRATING MICROCHANNELS ON PIXEL DETECTORS**

**“LOW TEMPERATURE” WAFER BONDING**
CEA-Leti, EPFL, G-Ray

- Jacopo BRONUZZI, PhD EPFL, 2018

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<thead>
<tr>
<th>COOLING PLATE</th>
<th>CMOS WAFER</th>
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</thead>
<tbody>
<tr>
<td><img src="image1" alt="COOLING PLATE Diagram" /></td>
<td><img src="image2" alt="CMOS WAFER Diagram" /></td>
</tr>
</tbody>
</table>

- Channels - Anisotropic Etch
- Channels - Anisotropic Etch
- Wafer Bonding
- Wafer Bonding

**BURIED CHANNELS**
EPFL, FBK
Clémentine LIPP, MSc EPFL, 2017

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<tr>
<td><img src="image3" alt="COOLING PLATE Diagram" /></td>
<td><img src="image4" alt="CMOS WAFER Diagram" /></td>
</tr>
</tbody>
</table>

- Trenches - Anisotropic Etch
- Trenches - Anisotropic Etch
- Channels - Isotropic Etch
- Channels - Isotropic Etch
- Trench Filling
- Trench Filling

- Tests ongoing with blank wafers
- **Embed microchannels** on the backside of CMOS wafers, tests later this year.