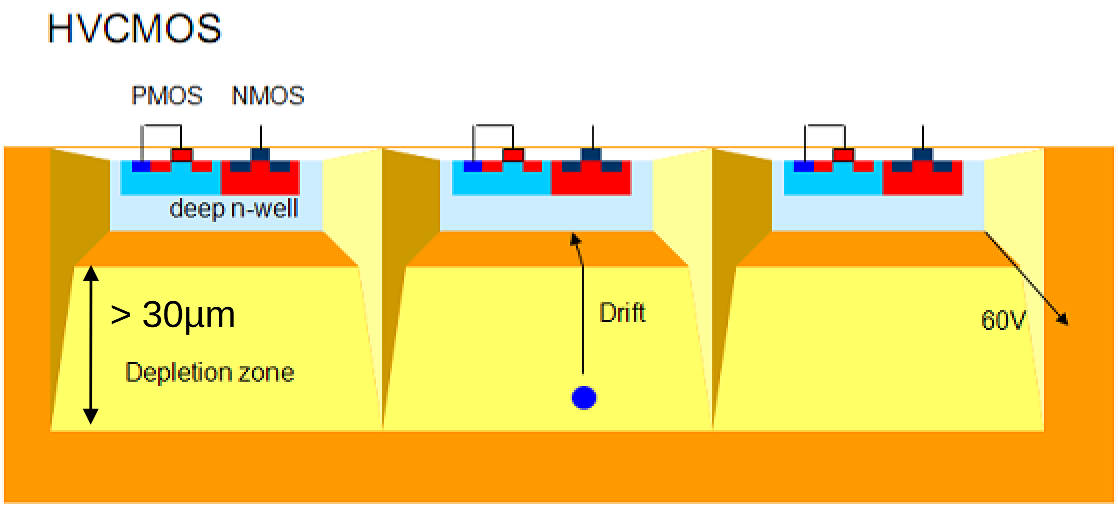
HV-CMOS Option for VXD Upgrade

Ivan Perić (KIT), Felix Ehrler (KIT), Thomas Fritzsch (IZM), Piotr Mackowiak (IZM)

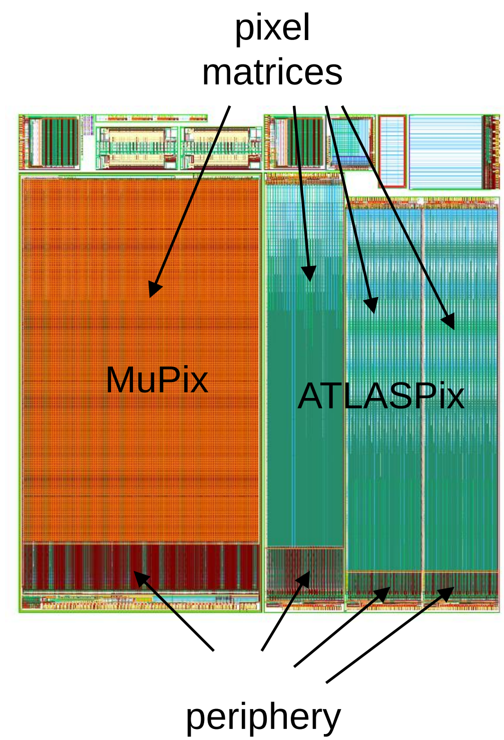
Introduction to HV-CMOS

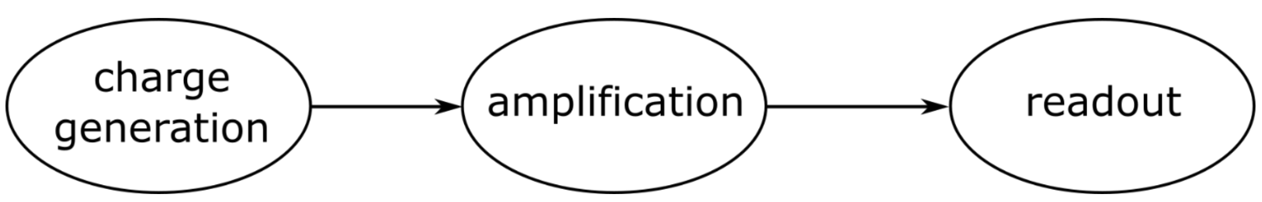
- HV-CMOS sensors are implemented in standard CMOS technologies
  - Cheap when compared to DEPFET or Hybrid
  - Very good availability
- n-in-p sensor
- Charge collection by drift is fast
- Very good signal to noise ratio
  - High voltage (-50 … -200 V) -> high resistivity substrate -> strong signals (e.g. > 5000 e/MIP)
- Very high radiation tolerance because of short drift path and large electrode
  - Intrinsic
  - Smart design
  - TID: 100 MRad
  - $1.5 \cdot 10e15$ neq/cm²



HV-CMOS in a Nutshell

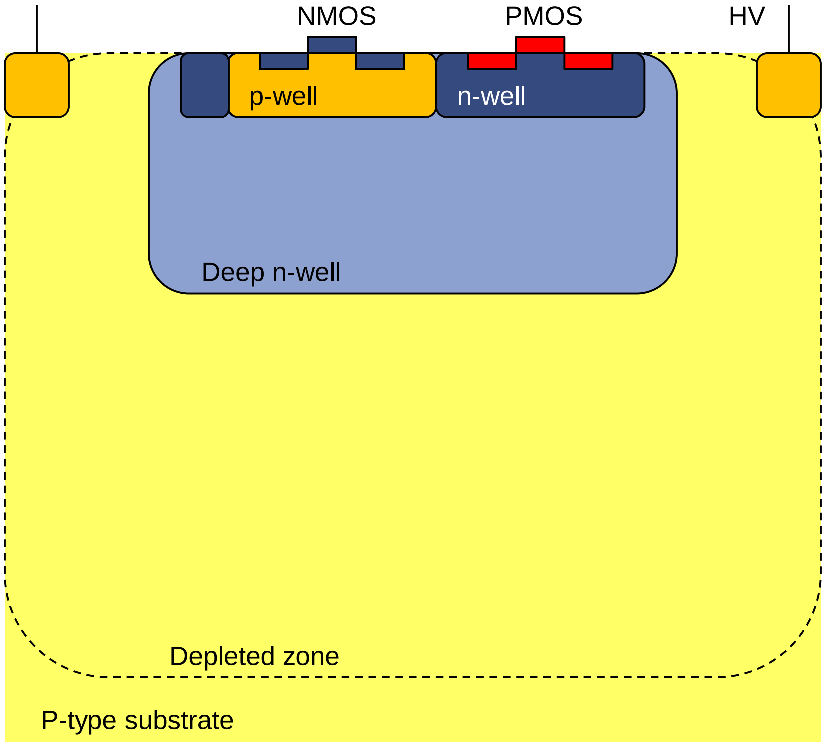
- Readout electronics and sensor on the same die: Monolithic Active Pixel Sensor (MAPS)
  - No dedicated readout chip, no ball bonding, low material budget
  - In-pixel charge amplification and in-pixel readout components
- HV-CMOS wafers can be thinned
  - Standard thickness is around 700µm
  - Thinning down to 70 µm and less is possible
- High resistive substrate is possible
  - E.g. 20 Ωcm …1k Ωcm
- Good time resolution
  - Fast amplifier
  - Smart digitization

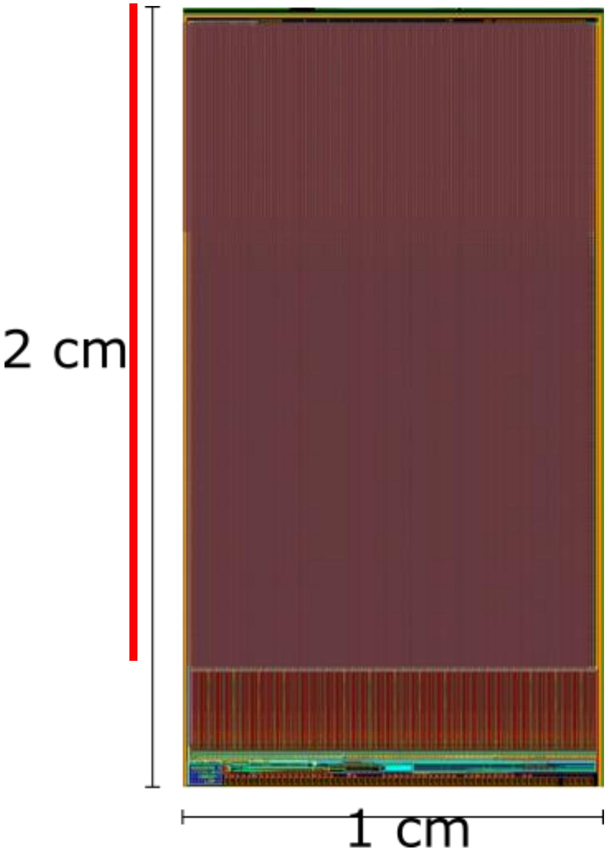




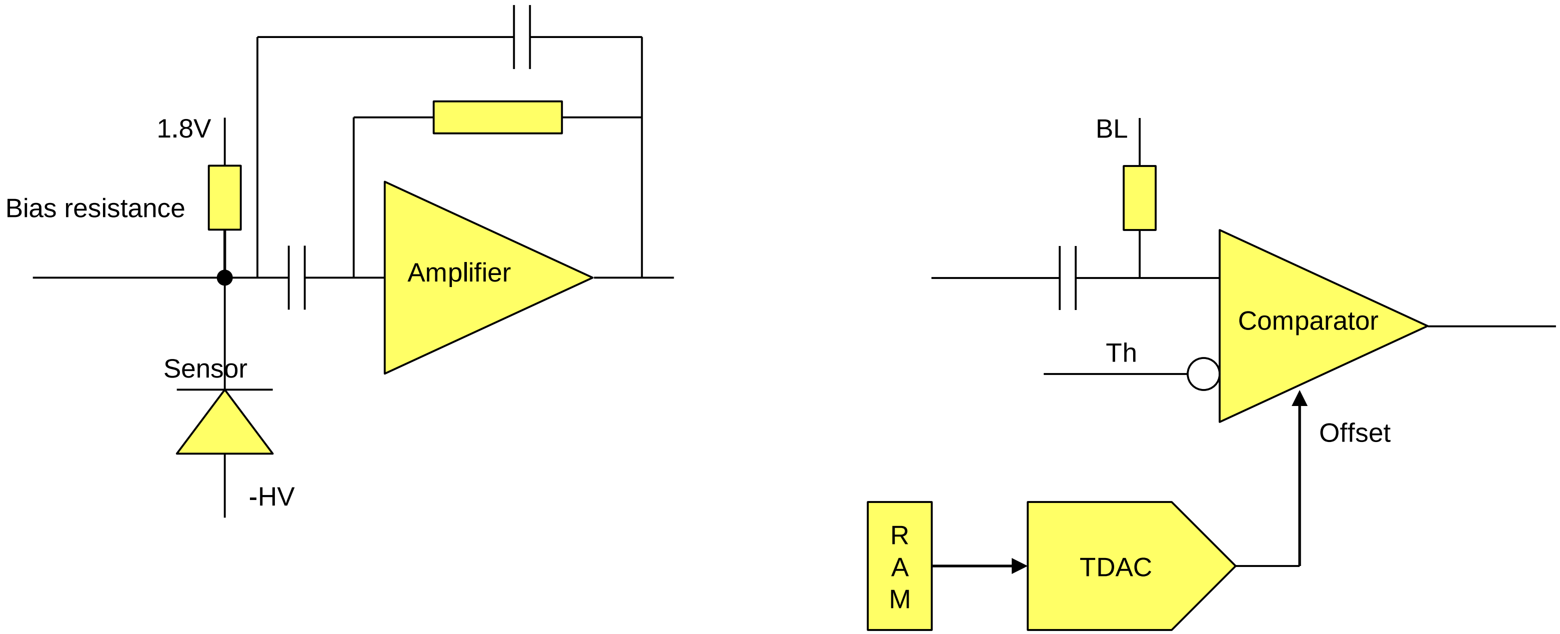
In-Pixel Components of a HV-CMOS Chip

- Pixels are based on floating electronics structure – pixel electronics is placed into a deep n-well
- Deep-n-well fulfils two tasks:
  - Local substrate for electronics (isolated from p-substrate)
  - Charge collecting electrode.
- The p-substrate region below the deep n-well is depleted by setting substrate to negative HV.
  - Typical depletion: 30 – 60µm for 80 to 200 Ωcm resistivity.
  - Minimum Ionizing Particle (MIP) signals are typically >5000e for 200 Ωcm substrate
- HV is connected to the front side
  - No backside bonding





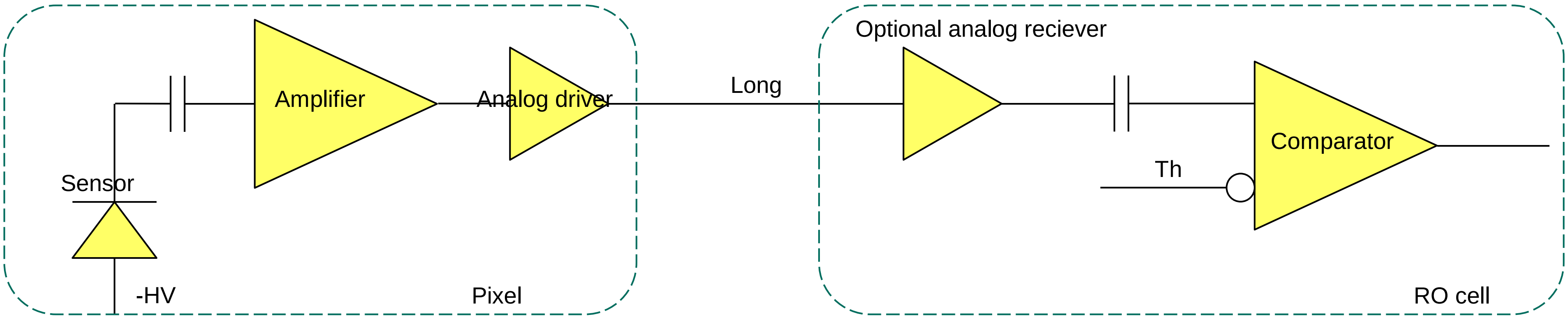
- Comparator is AC coupled to amplifier, it contains threshold tune circuit



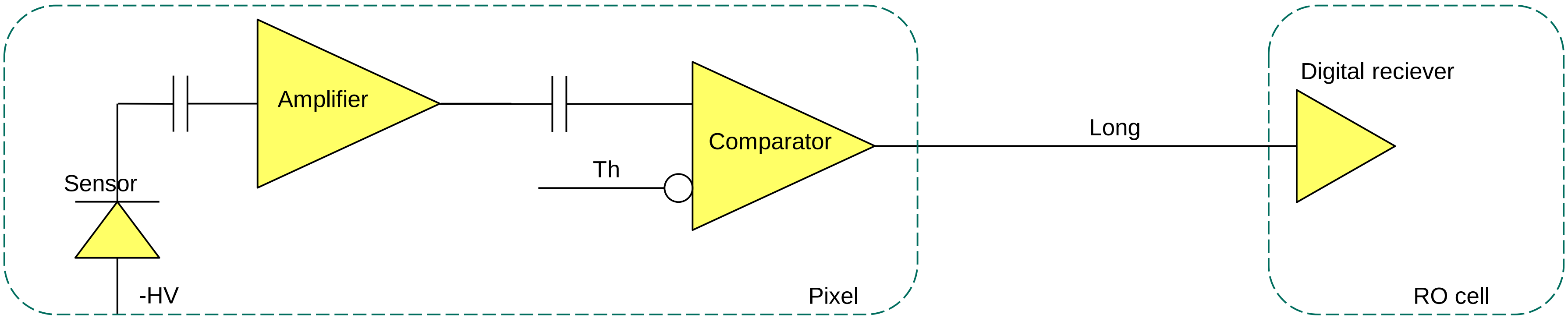
Position of the comparator

- Difference between MuPix and ATLASPix designs:
- MuPix: Comparator is placed at the periphery. The analog signal is transmitted via long lines from CSA to the remote comparator. There is additional analog driver in the pixel
- ATLASPix: Comparator is placed in the pixel

MuPix

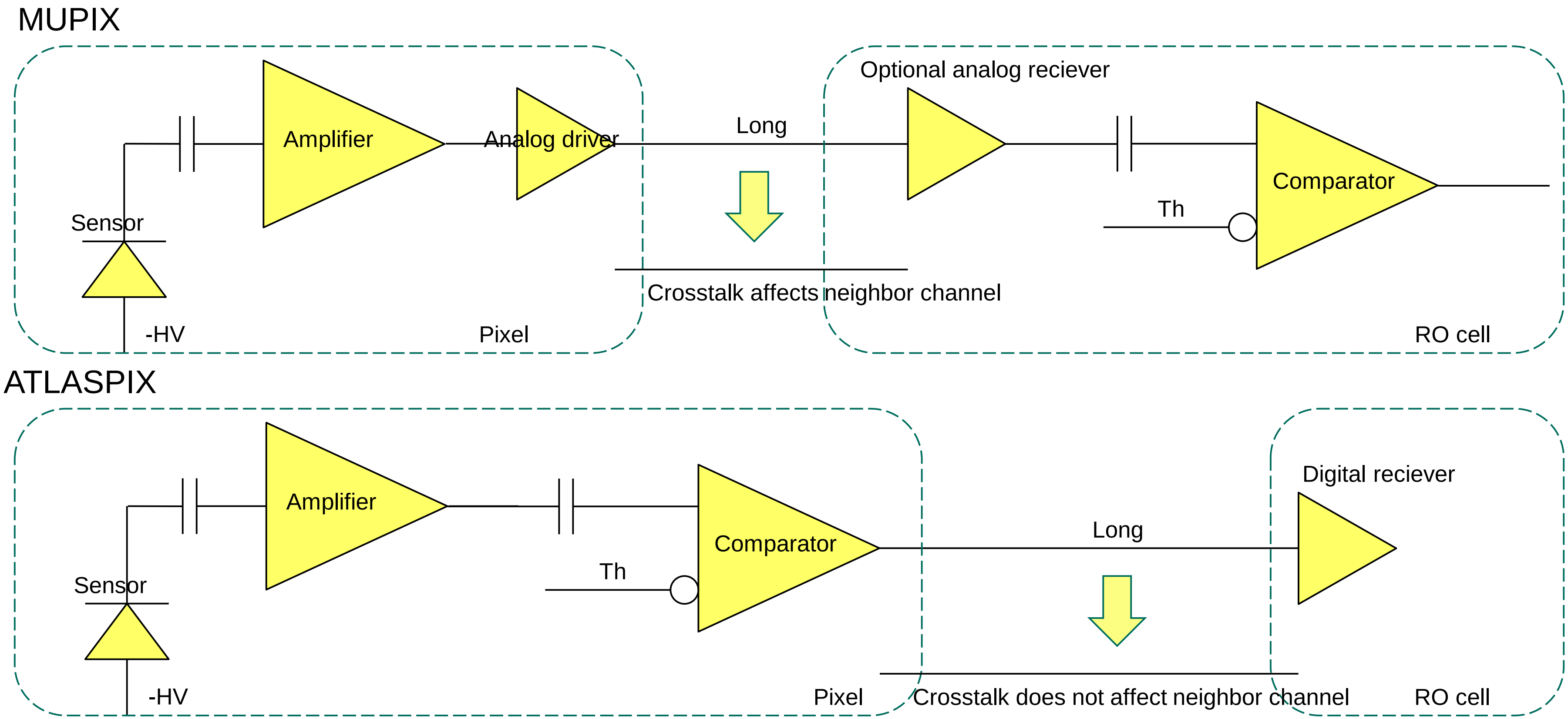


ATLASPix

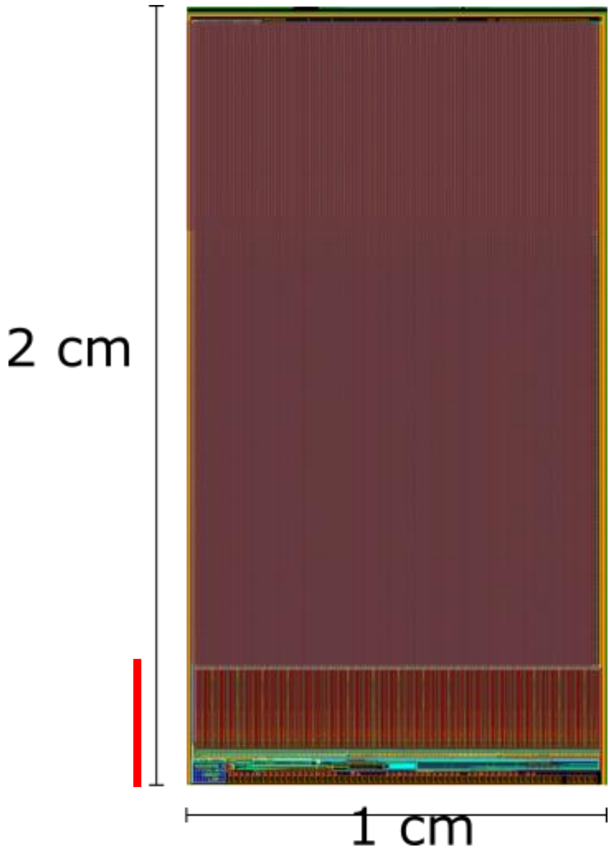


Position of the comparator

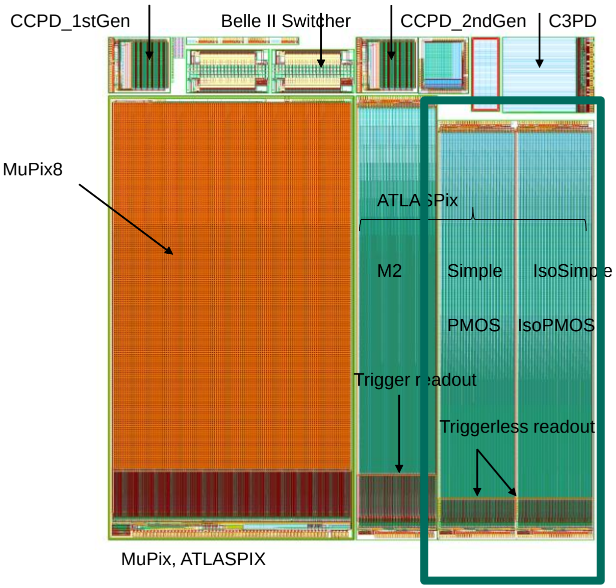
- Removing of comparator from pixel simplifies the pixel electronics → reduces detector capacitance and, in theory, improves time resolution of the system since rise time is shorter for equal noise. The disadvantage is large periphery and line to line crosstalk since analog signals are transmitted. Current drivers and clever routing tackle this issue.
- Placing of comparator in pixel leads to larger detector capacitance but it makes periphery smaller and eliminates crosstalk (because digital receiver has a high threshold)



- Data processing in periphery
  - No clock distribution over matrix → no noise spreading
  - A large number of connections is needed between each pixel and its readout cell
- Data collection
  - Pixel address
  - Time stamp
- Buffer structures
  - E.g. wait for trigger
- Data is only generated when actually a hit has occured
  - Instrinsic Zero-Suppression
- Additional information possible
  - Time over threshold
  - Analog signal height
  - Secondary time stamp
  - …
- All information is combined into a data package and prepared for readout
  - Hit grouping → data load reduction
  - Triggered readout → noise reduction
- Encoding (e.g. 8b/10b or 64b/66b)

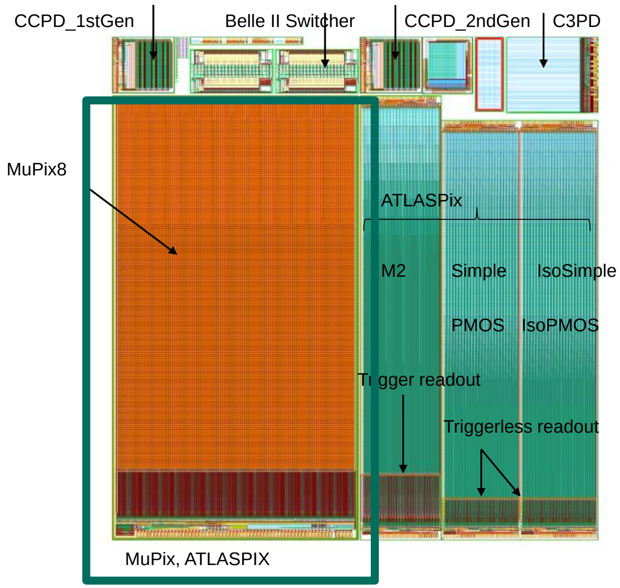


- Pixel matrix: 25 x 400 pixels of 130 x 40 µm² size
- Power consumption 300mW/cm²
- RO cells (hit buffers) that receive pixel signals and perform time measurement
  - (storing of 10-bit time stamp for time-measurement (T_{min} 12.5 ns) and 6 bit timestamp for ToT measurement)
- Readout control unit (RCU) that reads the hits from buffers, formats them (8b10b conversion is used) and sends via one serial link at up to 1.6Gbps
- Hit data word: 32/40 bits before/after 8b10b conversion
- A PLL is used to produce internal fast clock from a reference input clock. In the case of transmission of 1.6gbps, reference clock is 160MHz
- Shift register (SR) for configuration



MuPix, ATLASPIX

- Pixel matrix: 128 x 200 pixels of 80 x 81 µm² size.
- Power consumption 250mW/cm^2
- Pixels contain charge sensitive amplifier and voltage/current mode driver
- Every pixel has a RO cell at the periphery
- RO cell contains two comparators, tune DAC, RAM and digital circuits like ATLASpixSimple
- Readout control unit with 3 channels (RCU), PLL

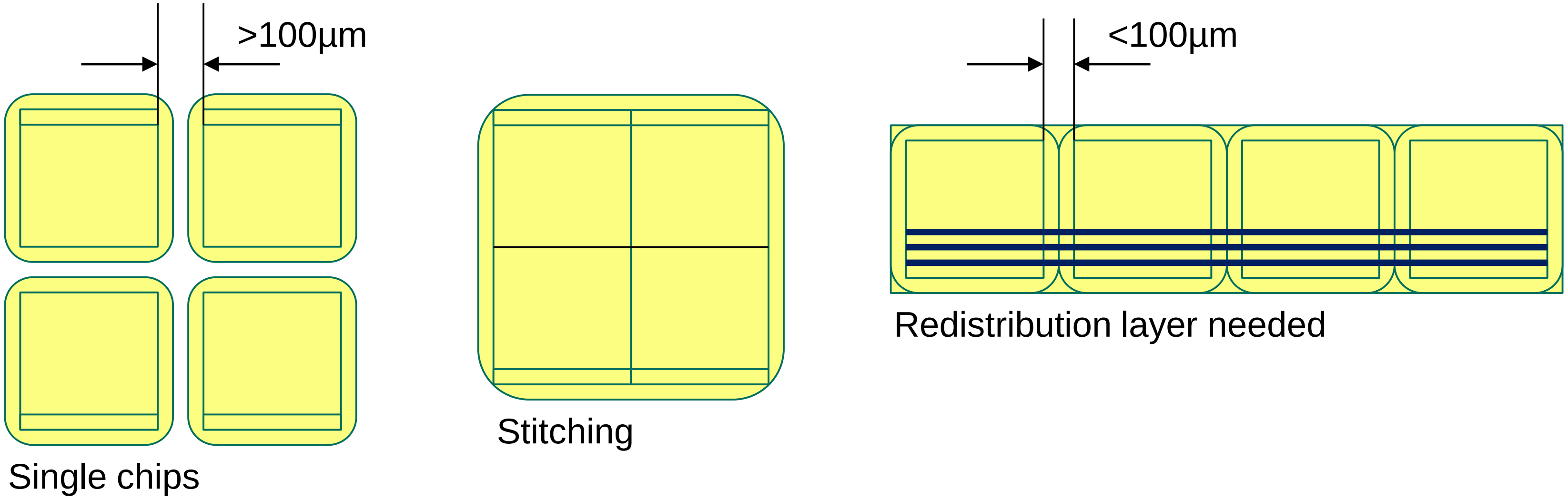


Introduction to HV-CMOS – Summary

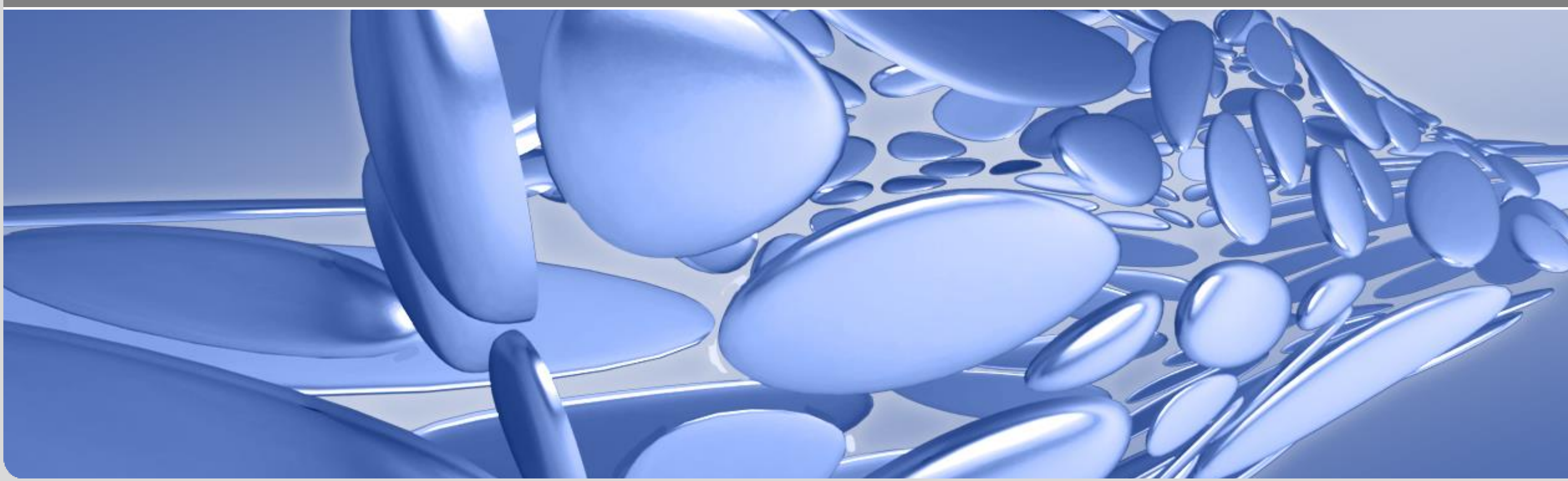
- HV-CMOS is a **standard process**: Cheap
- Electronics on sensor (MAPS): Possibility to have **data processing** on sensor chip
- Thinning: **Reduced material budget**
- Large depletion volume = **strong signals:** high voltage and high resistivity substrate
- **Radiation tolerance**
- Good **time resolution**
- HV is connected to front side

- One limitation:
  - CMOS sensors are produced by stepper, this means that the chip size is in principle limited to projection size of 2 x 2 cm².
  - Larger chips are possible by reticle stitching,
  - or by post processing: adding a redistribution layer (possible at IZM)
  - Some foundries like LFoundry, TSI, XFAB, TJ offer stitching
  - Some not: like AMS, IHP

- Each chip is 2 x 2 cm²
- Double line = bondpads and periphery
- Square with rounded corners = gap ~100 µm



Development and Projects of KIT ADL



- We develop HVCMOS for **Mu3e** experiment, **CLIC** and **ATLAS**
- Some other experiments would use similar designs: **Compass** and **P2**
- For these applications we have made two large area prototypes MuPix and ATLASPix. The process has been modified by using high resistivity substrate.
- CMOS sensor for Belle VXD could be based on one oft he existing designs
- Almost all our designs have pixels containint continuously running charge sensitive amps.
- Similar to DEPFET, but all amps always active → faster but higher power consumption

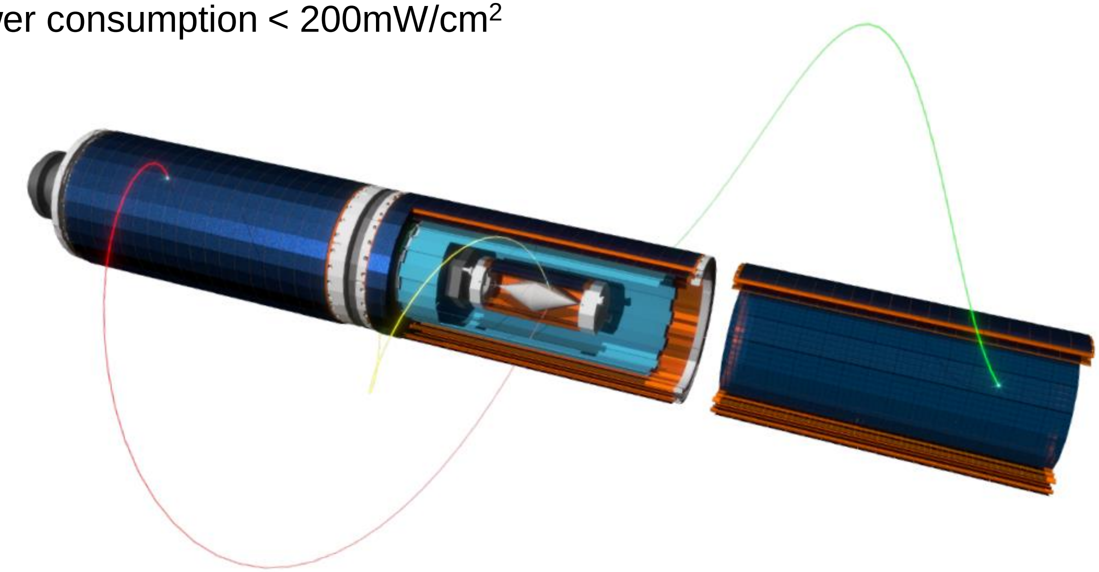
- Mu3e pixel detector should have extremely little material (0.1% radiation length per tracking layer).
- Only thin Al-Kapton flex provide stability (‘Origami’)
- Sensors thinned to 50µm
- Sensors chips: 2 x 2 cm^2
- Chips have inactive region for readout on one side, bonded by single point tape automated bonding (SPTAB) to the Al-Kapton flex

General specifications:

- Momentum resolution 0.5 Mev/c (low momentum particles < 53 MeV/c), vertex resolution ~ 200µm
- Particle flux: 10^9 muon decays / s → 1.5M hits/s/cm^2 (like 0.04 hits/BC/cm^2), all hits are readout, no trigger
- Radiation tolerance ~ NA

Chip specifications:

- Pixel size 80 x 81μm^2
- Cooling with thinned helium → power consumption < 200mW/cm^2



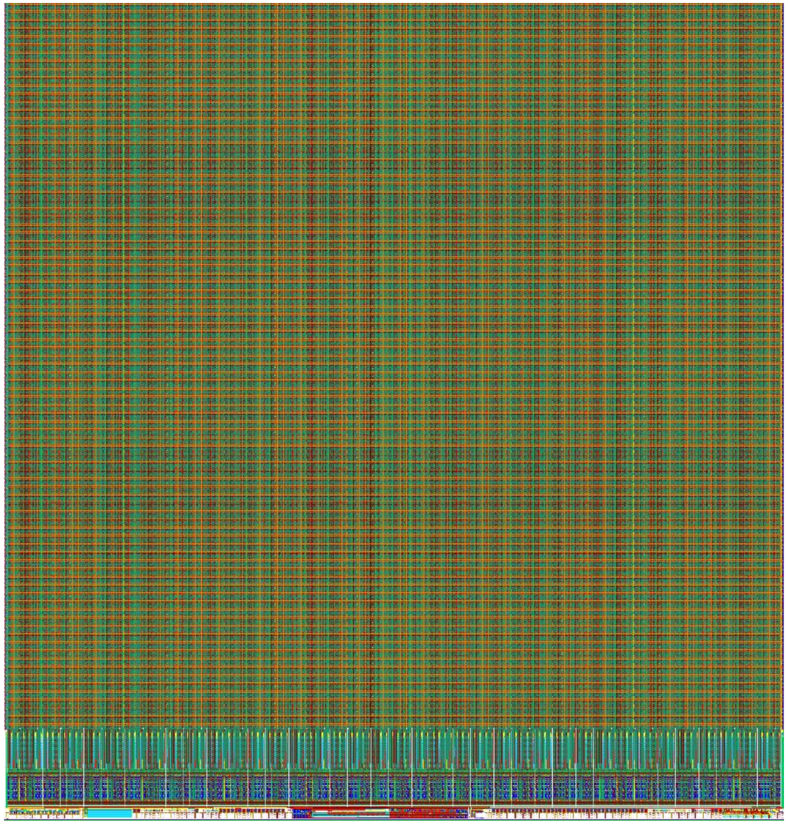
ATLASPix: Example of a production design

ATLASPix3

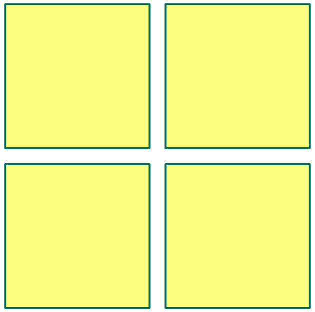
- HVCMOS sensor for quad module
- Implemented in TSI 180nm HVCMOS technology, licensed IBM/AMS H18 process
- Features and data interface similar to RD53
- Supports triggered readout with trigger latency up to 25µs
- Serial powering

Interface:

- Input CMD line (used for clock generation, L1 triggering with trigger tag, configuring and readback of configuration), like RD53
- Output: Aurora 64b66b, 1.28Gb/s, hit words 32bits, End-of-Event words
- Supports serial powering (only one power supply needed)
- Size: 20.2mm x 21mm
- Submitted in April 2019
- Expected soon

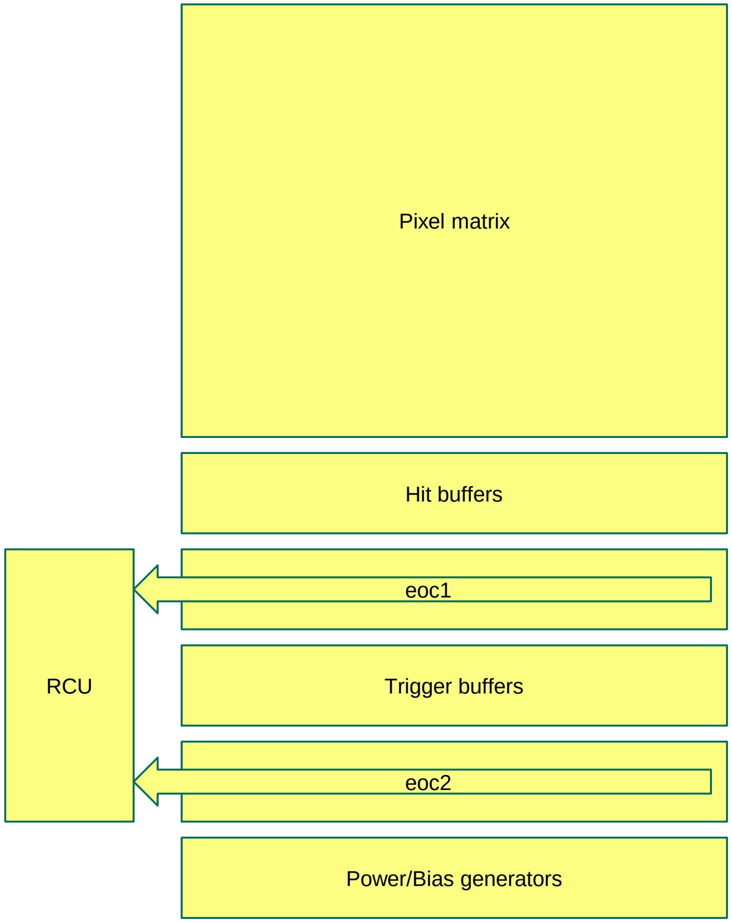


Layout of ATLASPix3



Square quadmodule

- Chip architecture is shown here: it contains pixel matrix, hit buffers, trigger buffers, digital block (readout control unit), power and bias voltage generators, Output data format is compatible with FEI3

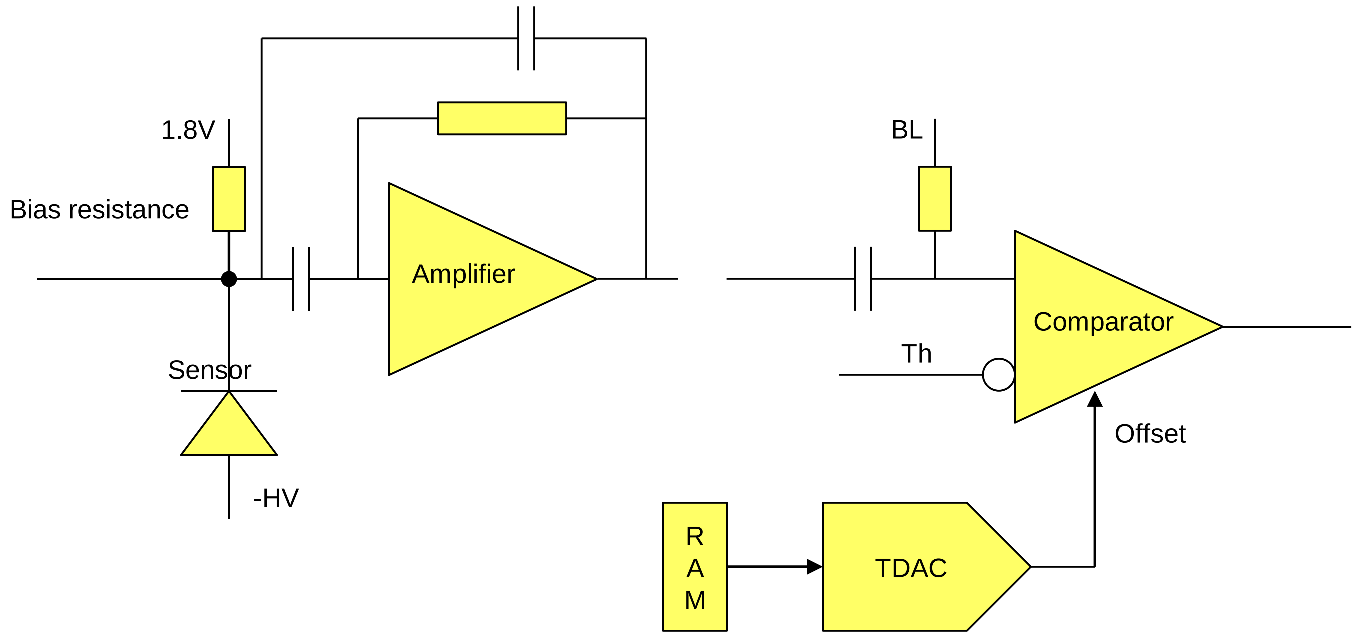


Pixel size (x, y): 150 x 50 μm^2
Matrix size: 132 x 372 pixels

Time stamp: 10 bits
ToT time stamp: 7 bits TS
Frequency: 80MHz (untriggered), 40MHz (triggered)

Hit word:
9 bit row address
8 bit column address
10 time stamp
7 bit ToT
= 34 bits

- Pixels contain continuously running charge sensitive amps.
- This could be compared to DEPFET. In DEPFET, there is also a simple amplifier per pixel. However, only one row is active at a time. In ATLASPIX, the amplifier is always active, it is connected to comparator. This means that the pixel can immediately detect a hit and record a time stamp with short delay after hit
- Advantage of this concept is fast timing (6 ns sigma), disadvantage higher power consumption.
- We have about 200mW/cm^2 for ATLASPix3.
- However, power consumption depends on time consumption. This means ATLASPIX has time resolution of 25ns and 200mW. The chip can be also done to have 100ns time resolution and 100mW consumption that is similar to DEPFET.

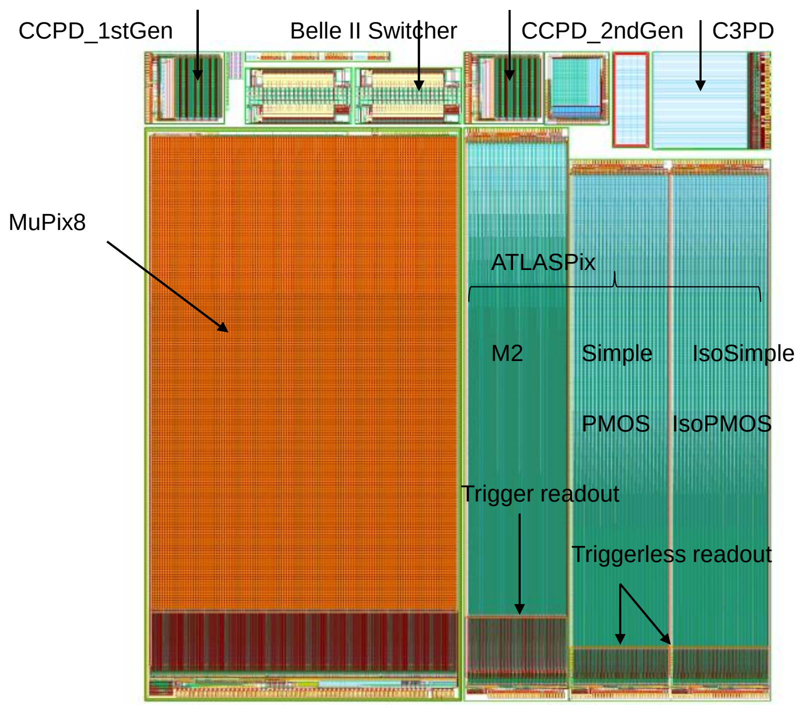


ATLASPix3 Summary

- ATLASPix3 has the following properties:
- Chip size: 20.2 x 21 mm^2
- Active area size: 20.0 x 18.6 mm^2
- Periphery height: 2.3 mm
- Pixel size: 150 x 50 μm^2
- Radiation tolerance 100 Mrad and 1 x 10^{15} neq/cm^2
- Readout: triggered (untriggered can be optionally used for testing)
- Analog information: yes (7 bits)
- Time resolution (~ 5ns required, present status 6ns)
- Trigger: up to 4MHz with latency 25µs, trigger window 25ns
- TSI process
- Serial powering
- Output data rate: about 0.5 - 1 hit / 25ns / $4cm^2$ (after trigger) – one serial link/chip at 1.28gbps
- Typical particle rate: about 1-2 / cm^2 / 25ns or 40 10^6 / cm^2 / s
- By reduction of trigger latency (25µs → 5µs) the same design can cope with by factor 5 higher particle rate, further improvement is possible by increasing buffer depth

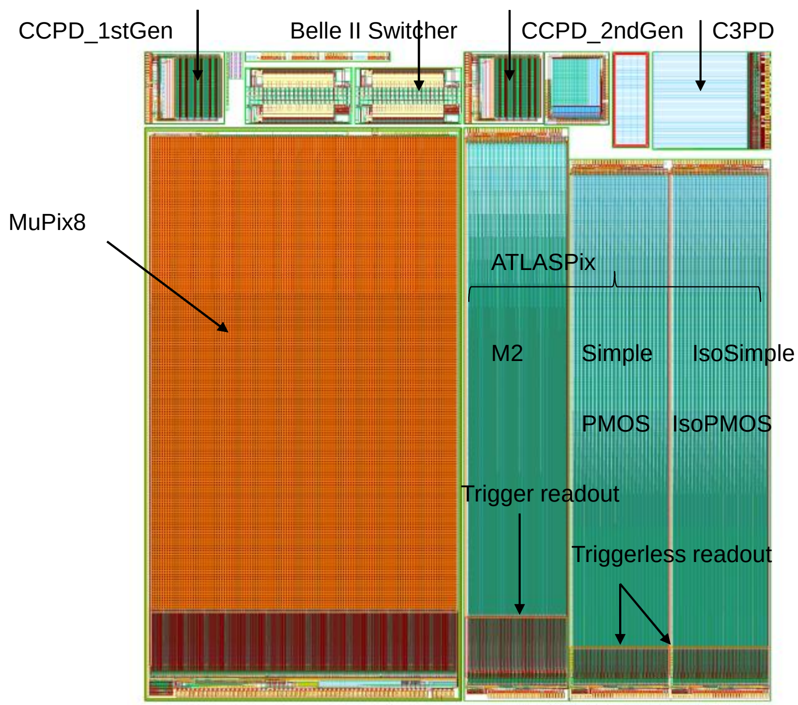
Measurement Results

- Shown the results obtained with MuPix8 and ATLASPix1

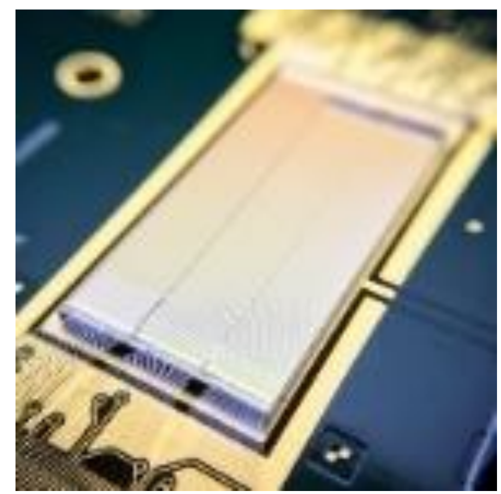


MuPix, ATLASPIX

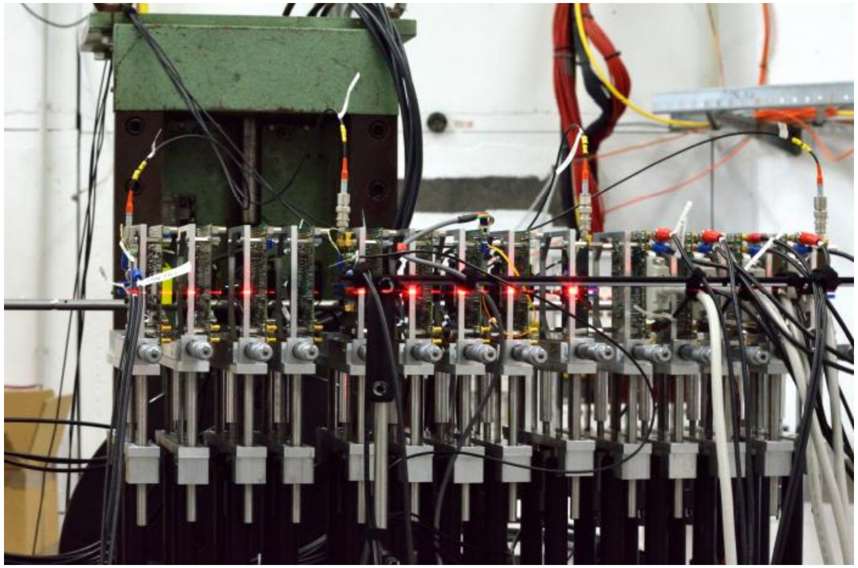
- Two large area prototypes MuPix8 and ATLASPix1
- MuPix8: Area 1cm x 2cm, Pixel matrix: 128 x 200 pixels of 80µm x 81µm size, two matrix types
- ATLASPix1: two variants: M2 – triggered readout, Simple – untriggered readout (here two flavours "normal" and with isolated PMOS option)
- Example: Simple "normal": Pixel matrix: 25 x 400 pixels of 130µm x 40µm size
- Submitted within engineering run. Producer AMS. Technology is 180nm HVCMOS, process HV 7sf (H18), variant aH18
- Process has been modified using high resistivity substrate



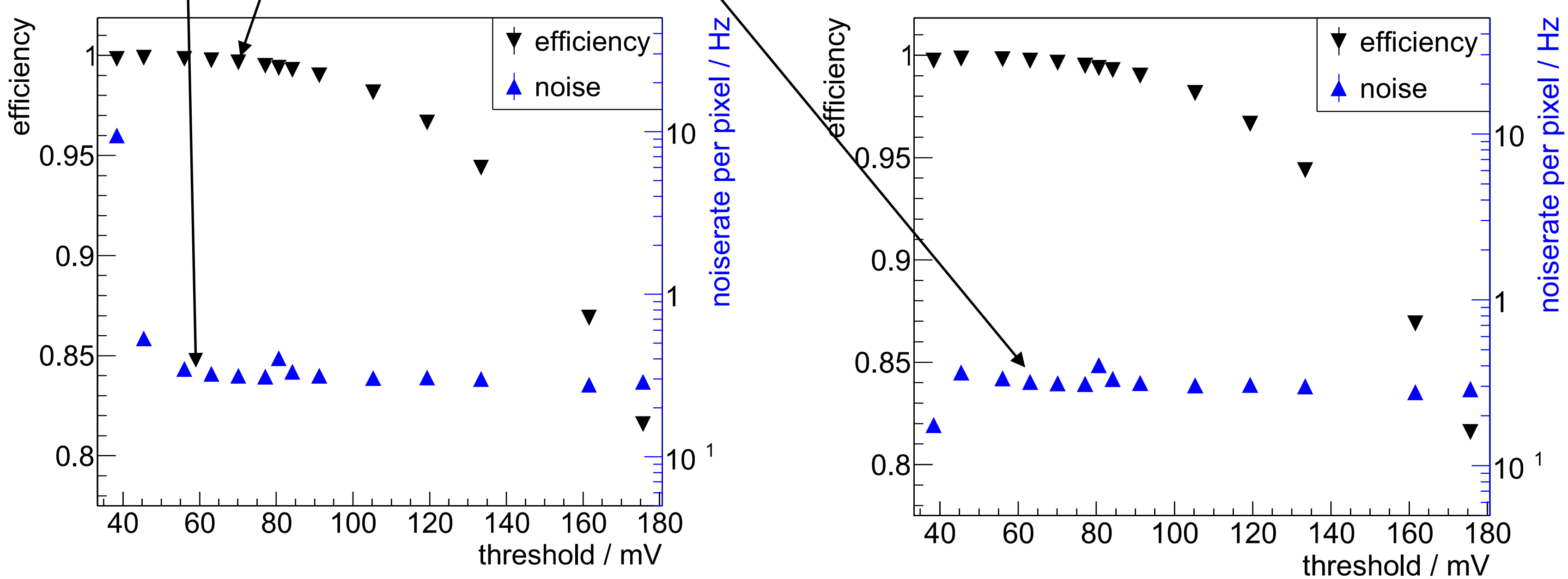
MuPix, ATLASPIX



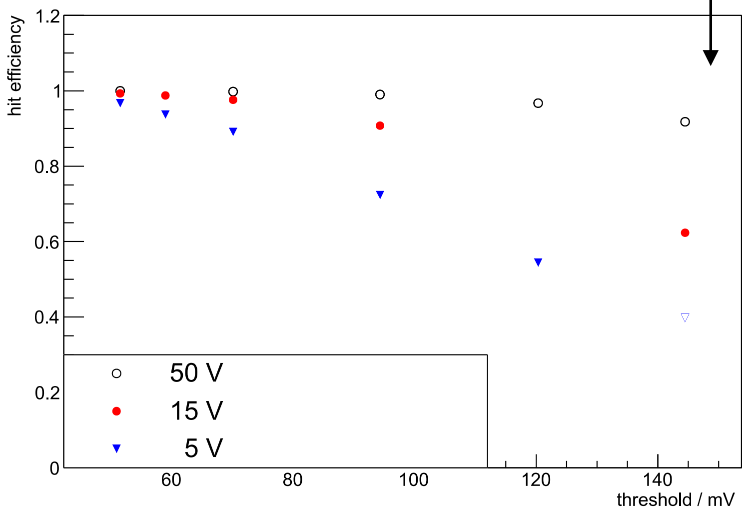
- The efficiency has been measured in beam using MuPix telescope (developed in Heidelberg)
- Uses 4-8 layers of MuPix chip, one is device under test (DUT)
- Measurements have been performed at DESY, MAMI and PSI

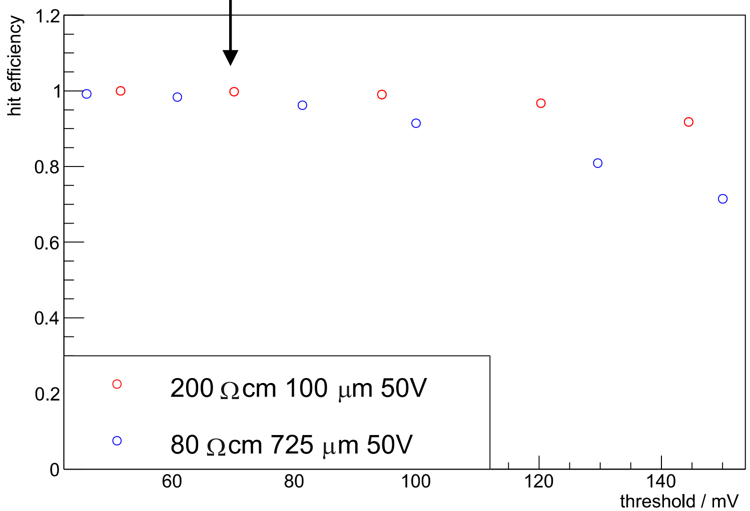


- The detector is highly efficient in detection of minimum ionizing charged particles
- The noise is low
- There is a large plateau with high efficiency and low noise.
- Masking of pixels improves noise further

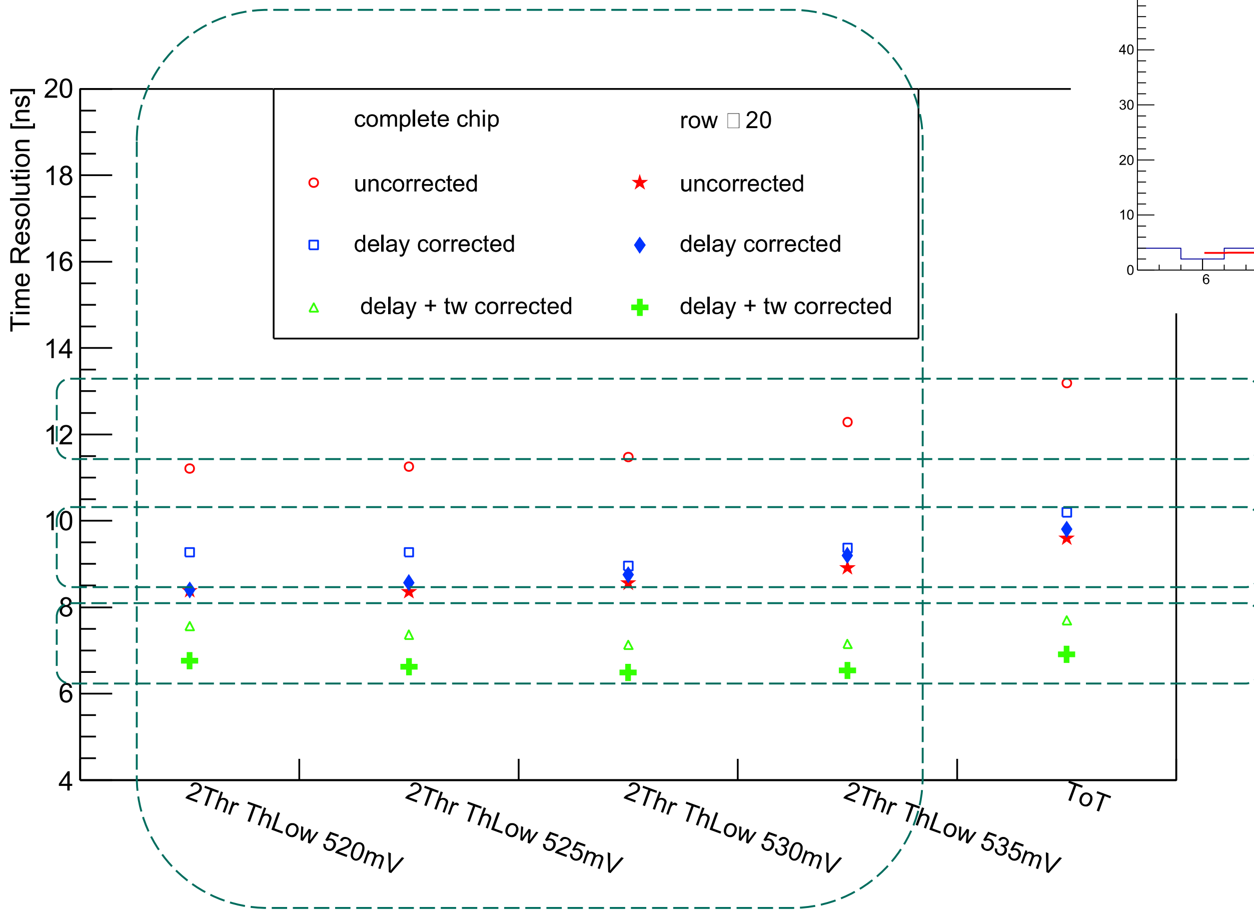


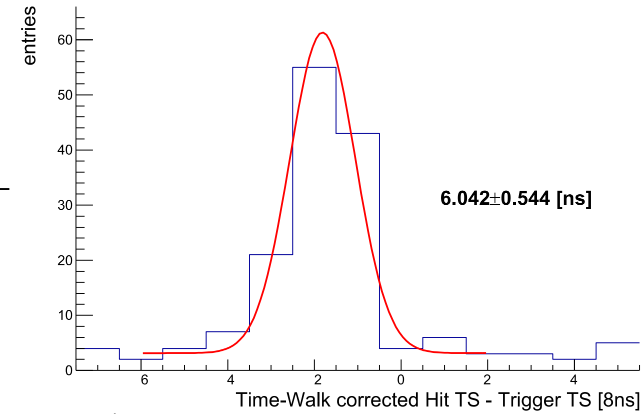
- The efficiency improves with high voltage bias (HV) and with substrate resistivity



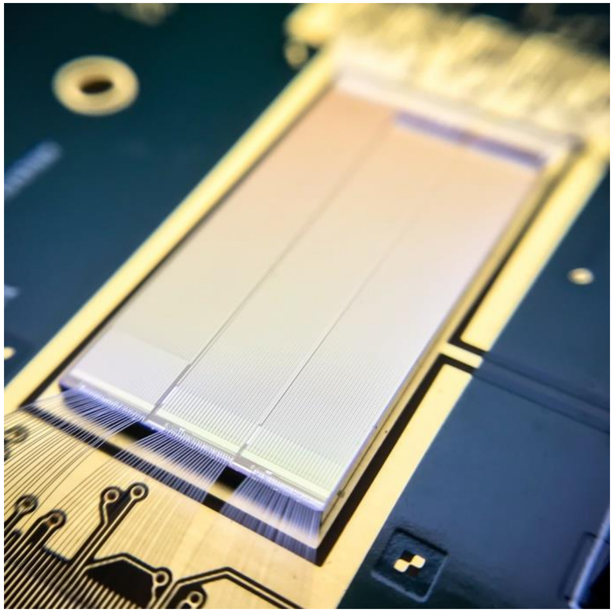


- Using linear correction obtained from the plot time resolution can be improved to ~ 6ns RMS





- ATLASPix1



Summary of Efficiencies after Irradiation

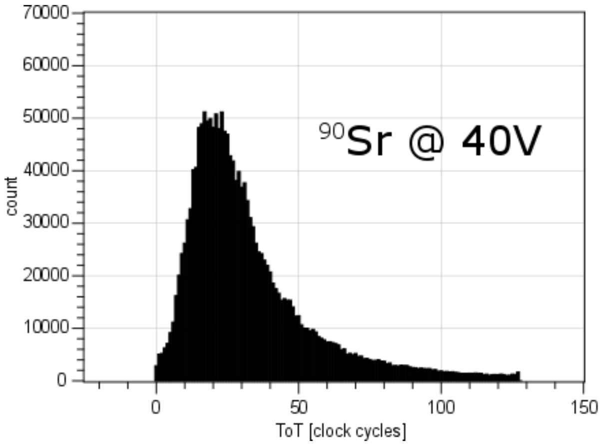
- no tuning of pixels; ≤ 81/10000 pixel masked

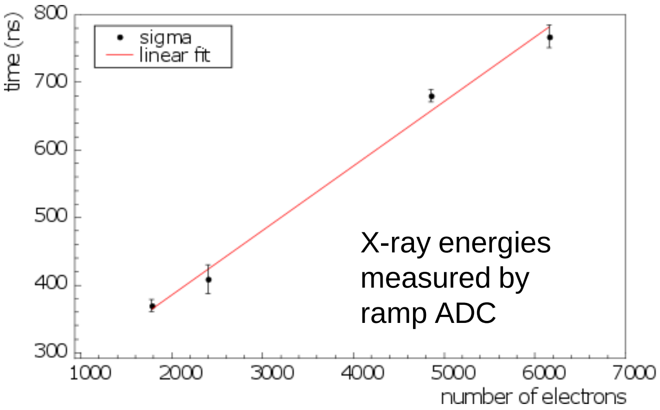
Efficiency$_{40\ Hz}$	sub-strate	thick-ness	bias voltage (#masked pixel)			
fluence (neq/cm²)	(Ω cm)	(μm)	60 V	70/75 V	80/85 V	90/95 V
n 2e15	80	62	98.5% (81)	98.4% (81)	98.6% (81)	
n 1e15	80	62	99.3% (38)		99.5% (38)	99.5% (39)
n 5e14	80	62	99.5% (19)			
n 2e15	200	100	96.5% (55)		98.7% (60)	98.7% (55)
n 1e15	200	100/725	98.7% (18)	99.4%	99.5%	99.4%
n 5e14	200	100	99.2% (14)			
p 5e14 (50 MRad)	200	100	≥ 99.6% (9)	≥ 99.7% (9)	≥ 99.9% (9)	
p 1e14 (10 MRad biased)	200	725	≥ 99.7%			

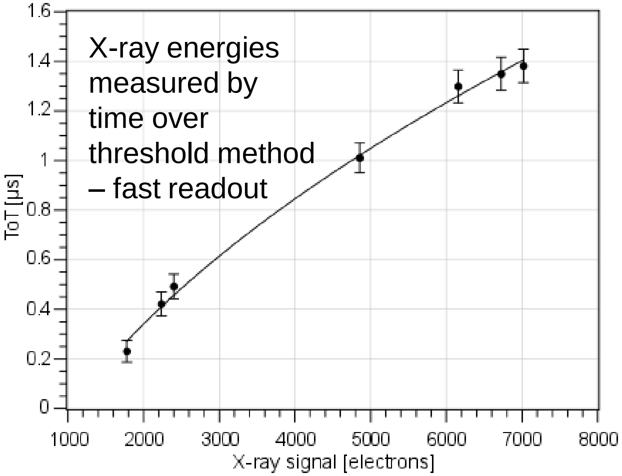
≥ means that the 40 Hz/pixel noise limit was not reached

- MuPix8


C247
C179
C196
C157
C297
C235
C243

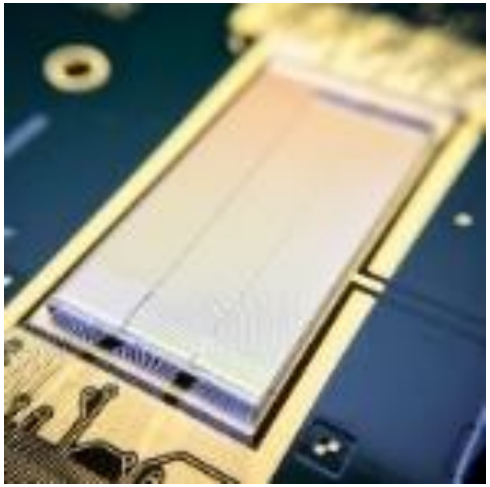

70000
60000
50000
40000
30000
20000
10000
0
count
0
50
100
150
ToT [clock cycles]
90Sr @ 40V


800
700
600
500
400
300
time (ns)
sigma
linear fit
1000
2000
3000
4000
5000
6000
7000
number of electrons
X-ray energies
measured by
ramp ADC


1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
ToT [µs]
1000
2000
3000
4000
5000
6000
7000
8000
X-ray signal [electrons]
X-ray energies
measured by
time over
threshold method
– fast readout

Summary of measurement results

- ATLASPix and MuPix are large area designs (MuPix 1cm x 2cm) work well
- The chips are implemented in HVCMOS process, high resistivity wafer has been used
- The sensors have readout circuits on chip
- Efficiency in beam > 99% for charged ionizing particles.
- Best time resolution achieved with MuPix8 is 6 ns RMS
- We are currently working on the large ATLASPIX3 (submitted) and MUPIX10 (submission thisfall) designs



Module concept for Belle II

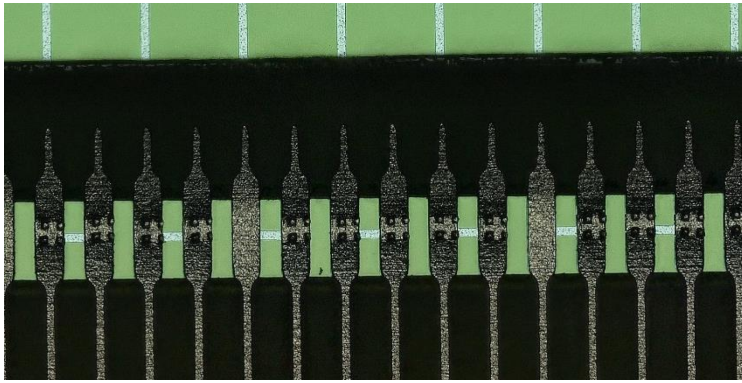
- For ATLAS and Mu3e different module concepts are used than in VXD.
- ATLAS is based on quad modules, in case of Mu3e we plan to glue the chips on Kapton flex with aluminum lines. Stability is assured by folding (0.1% radiation length).

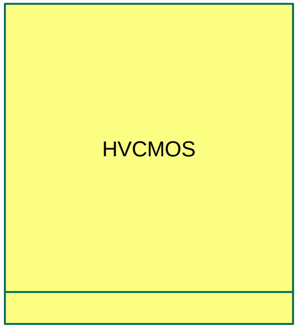
- Here we proposed a structure that is similar to what we have now. We could make multi-reticle CMOS modules. Several reticles form one module. One module is cut in one piece from wafer.
- We need to reduce power consumption
- We need to be compatible to the existing structures

Possible HV-CMOS Module for Belle II PXD

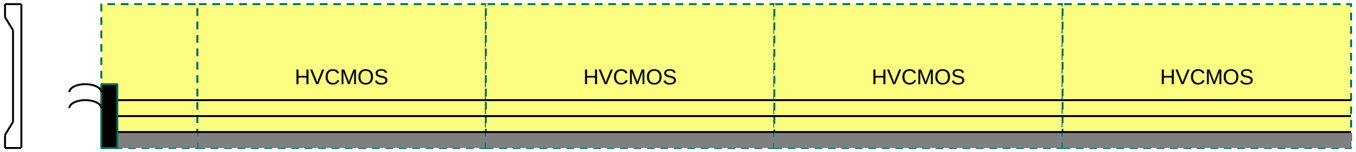
- Module for Belle II can be based on ATLAS design
- Belle II module could consist of 4 - 5 reticles with, each ca. 2 cm x 1 cm size
- Matrix height would be half of ATLAS' matrix → easier design, smaller periphery
- Pixel size ~ 50µm x 50µm → does not necessarily increase power consumption (smaller p-well = smaller detector capacitance)
- Comparator in periphery → lower power consumption
- Slower timestamp: 50ns instead of 25 ns → lower power consumption
- To avoid wire bonding of all chips , we can do additional power and signal lines after CMOS processing (redistribution layer). This can be done at IZM. Cost is about 20k for 10 wafers (enough for PXD)

Tabonding at KIT





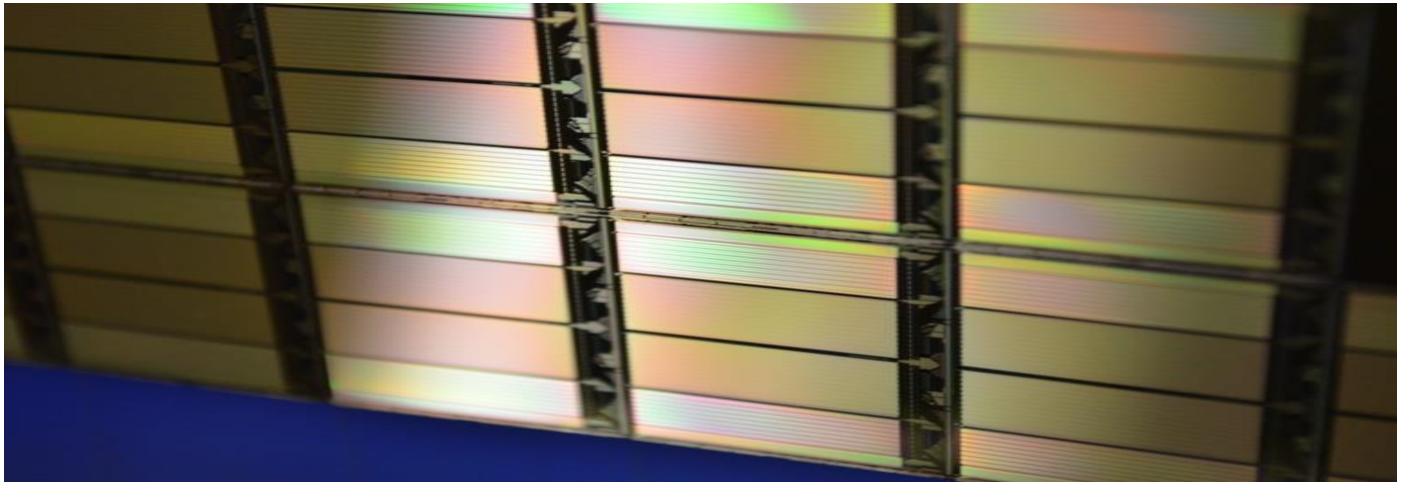
Possible configuration for PXD

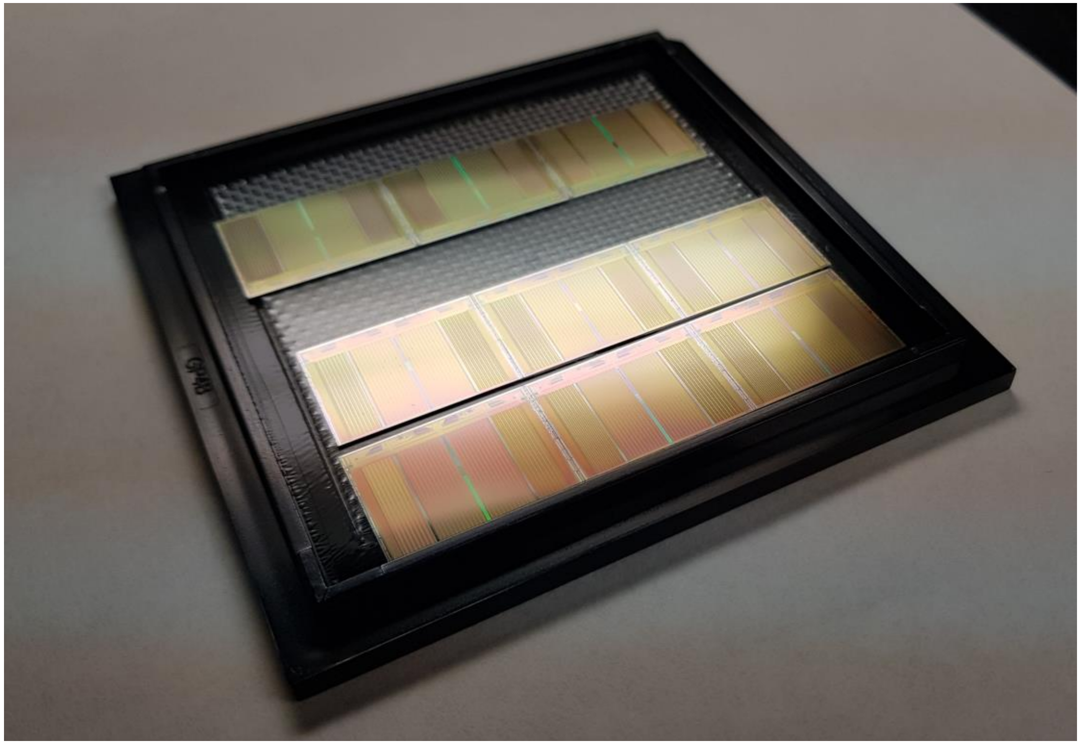


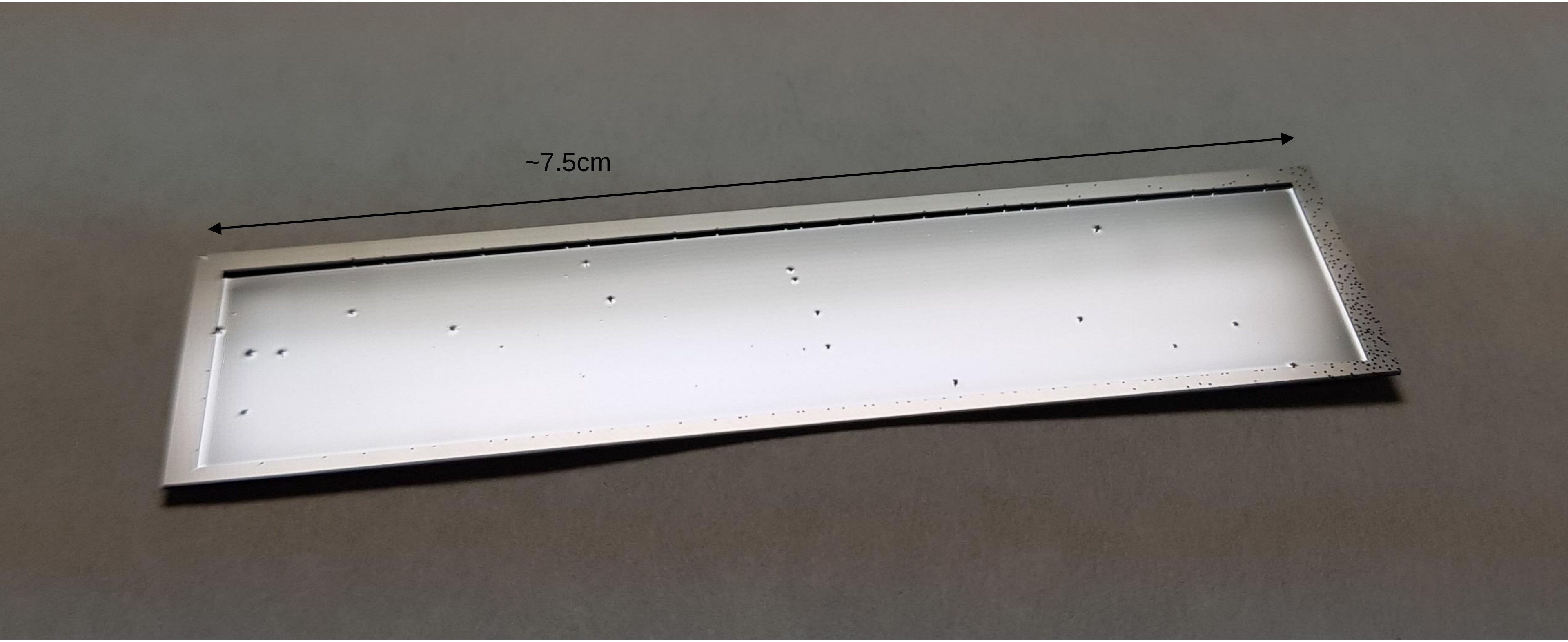
First Steps towards a HV-CMOS Module for Belle II

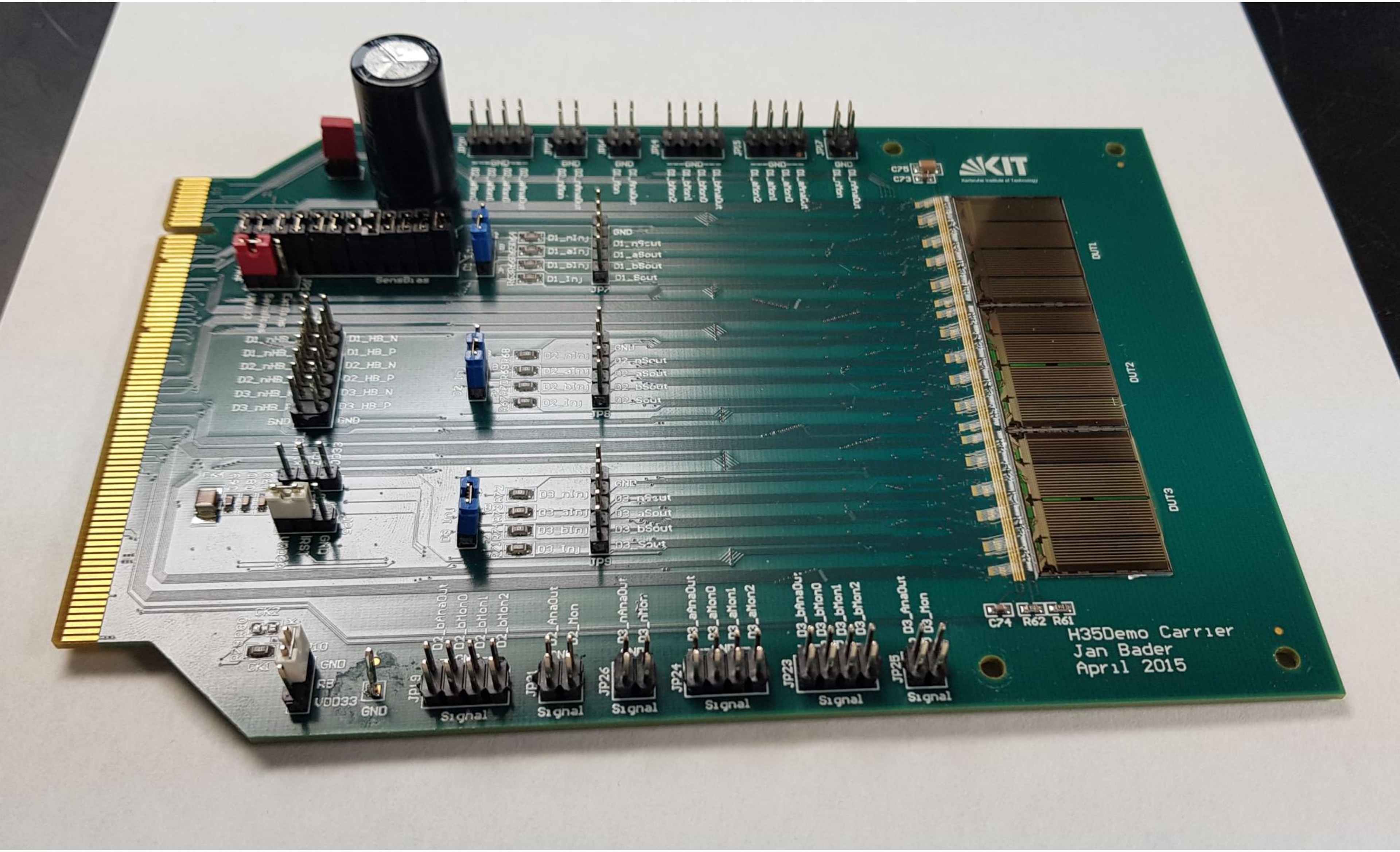
- A nice feature of DEPFET module is that it has a thick frame and thin active region. This assures mechanical stability together with low material budget
- The question is: Can it be done on CMOS as well?
- To test this we have sent several wafers to IZM Berlin. We have used an older HV-CMOS design (350nm technology), the H35DEMO. This was the first HV-CMOS engineering run (ATLASPix1 was at this moment in production)
- H35DEMO is a chip of 2.5 x 2 cm², with several matrix types. Similar to ATLASPix we have nice results. However, large 350 nm technology leads to a larger power consumption
- IZM has performed patterning of the backside so that we have an active region of <100 µm thickness and a frame of original thickness
- The modules are mechanically stabile

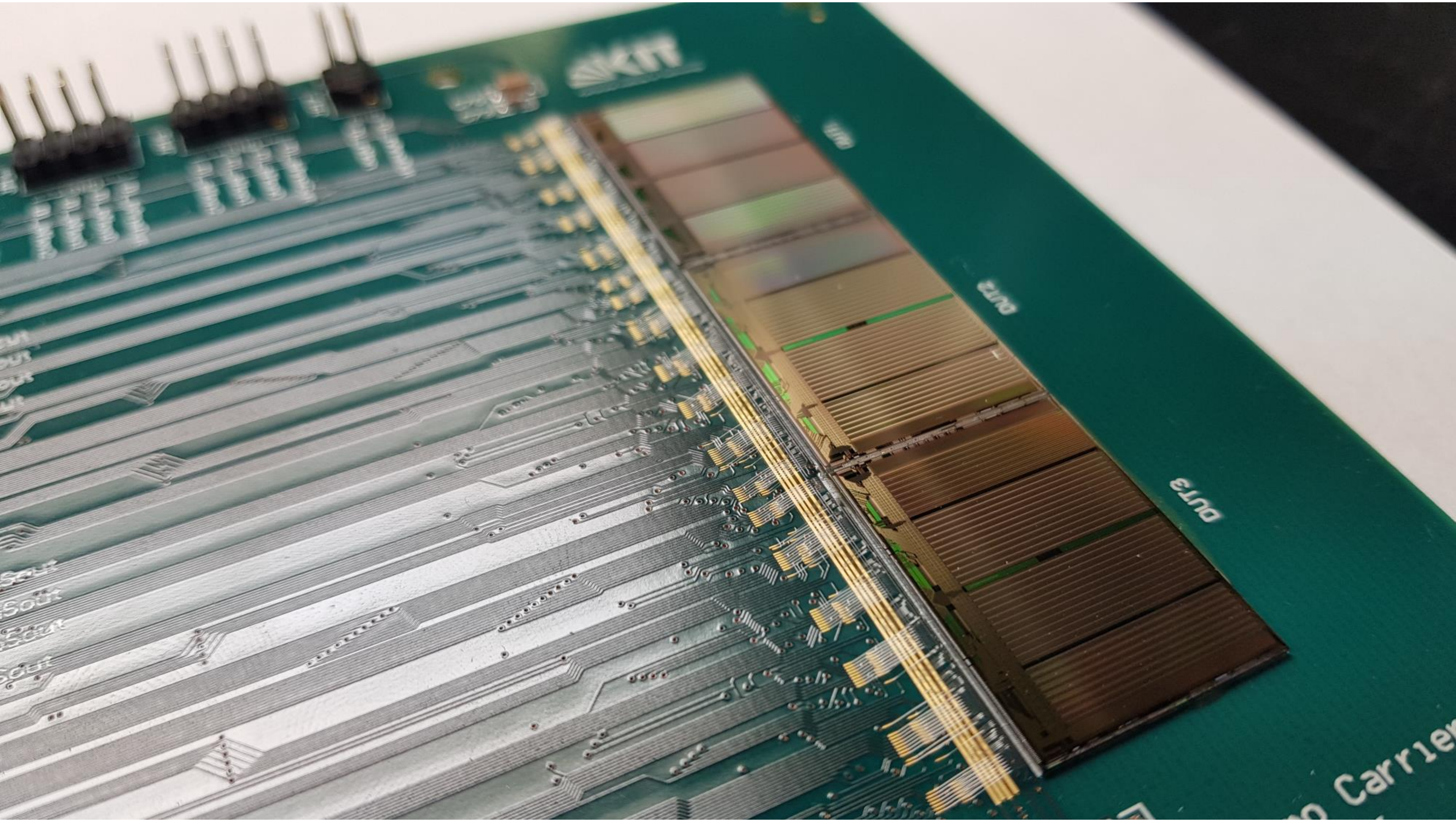
[1] Benoit, M., et al.; Test beam measurement of ams H35 HV-CMOS capacitively coupled pixel sensor prototypes with high-resistivity substrate; Journal of Instrumentation 13(12),P12009; 2018



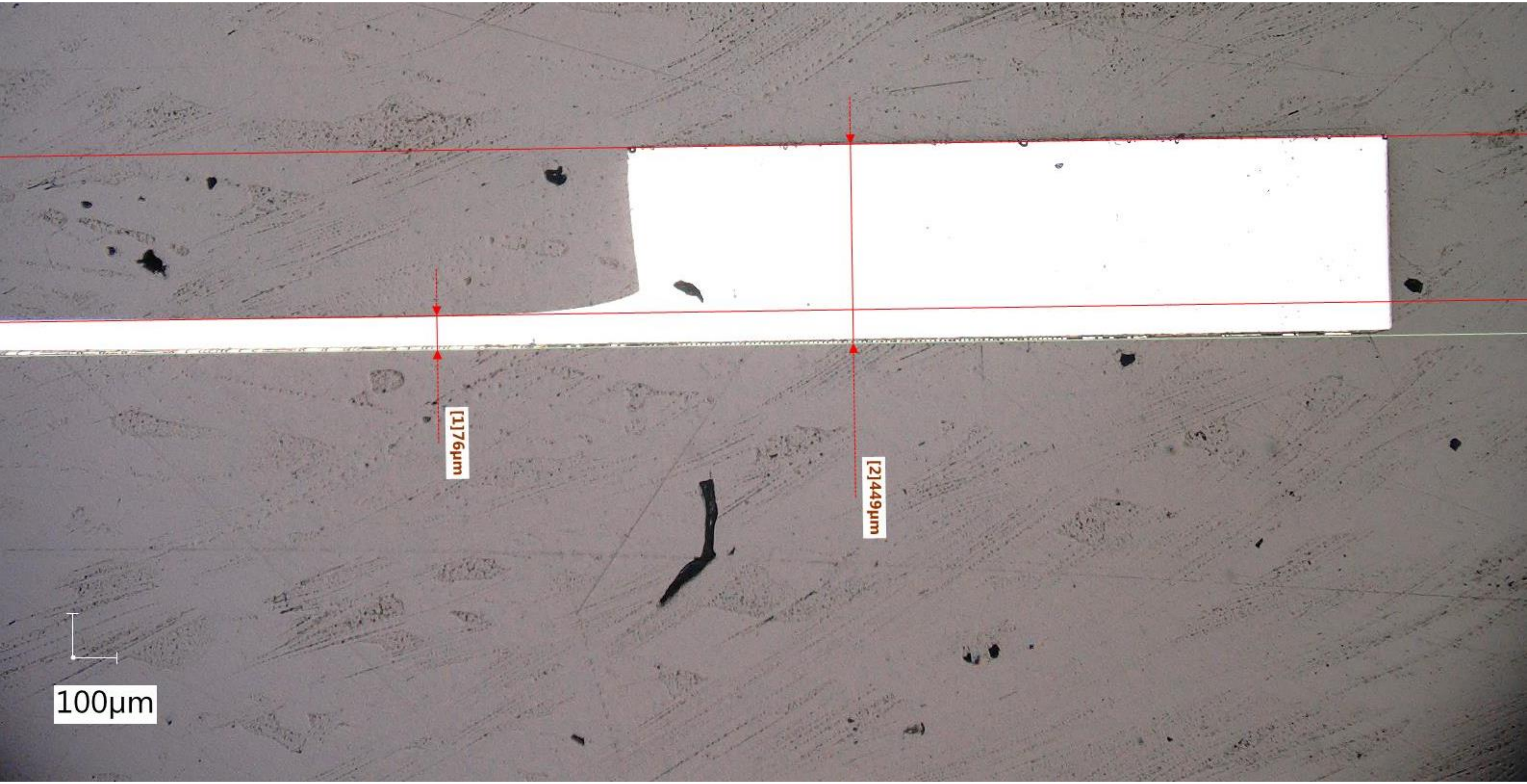


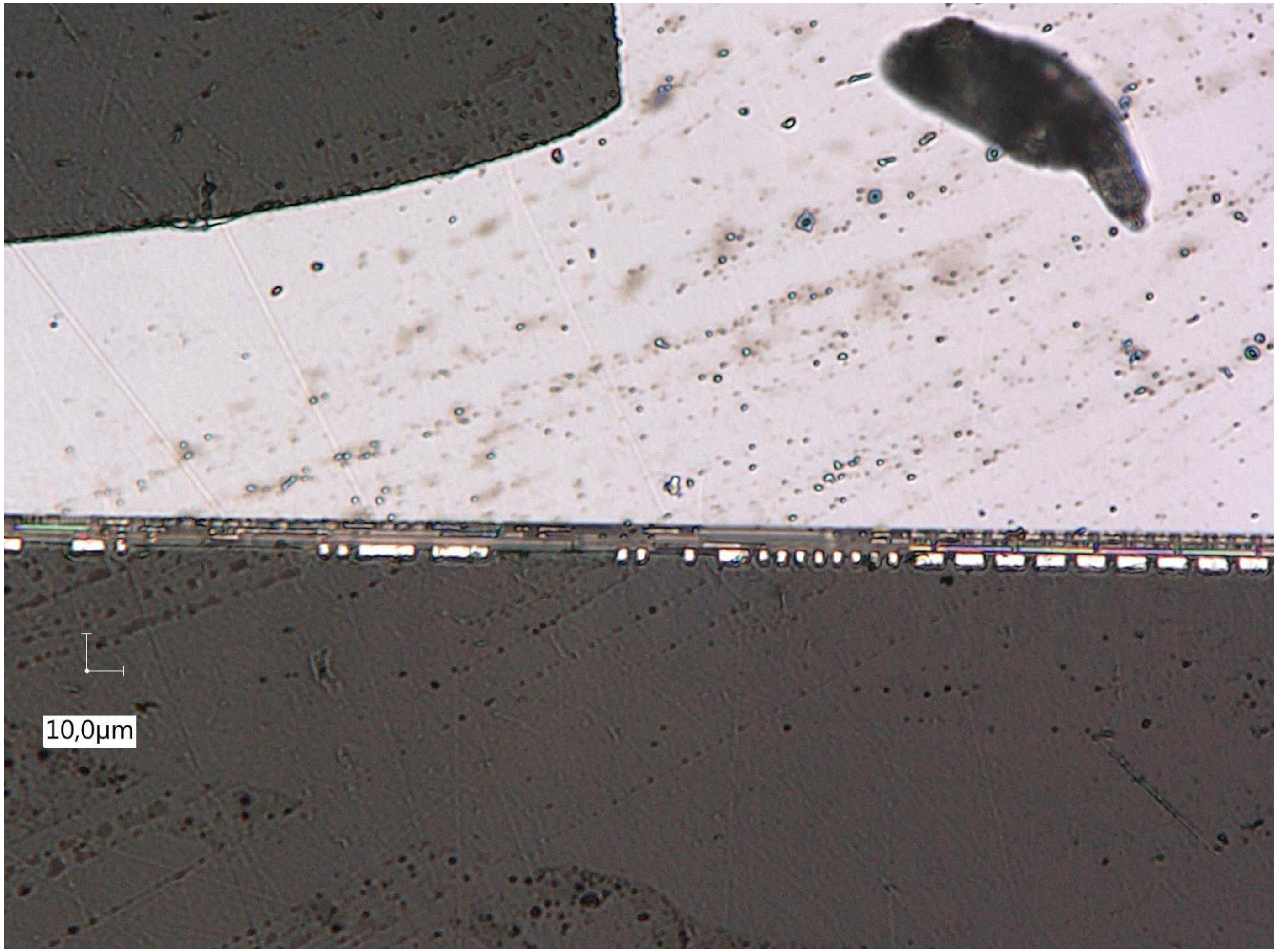

~7.5cm


H35Demo Carrier
Jan Bader
April 2015
KIT
DUT1
DUT2
DUT3
Signal
SensBias

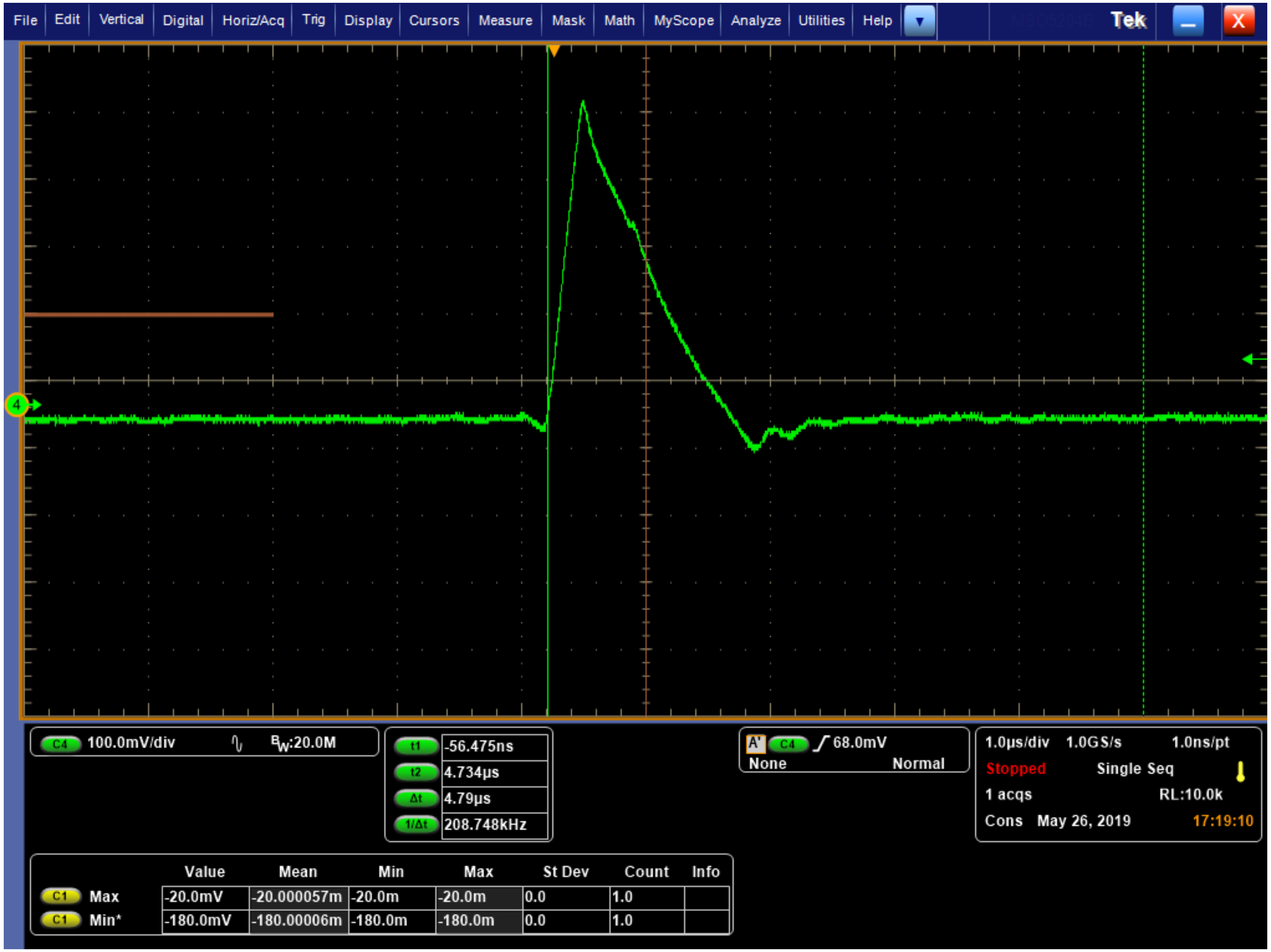

DUT2
DUT3

- The module was cut and the cross section measured
- Thickness in active region is 76 µm



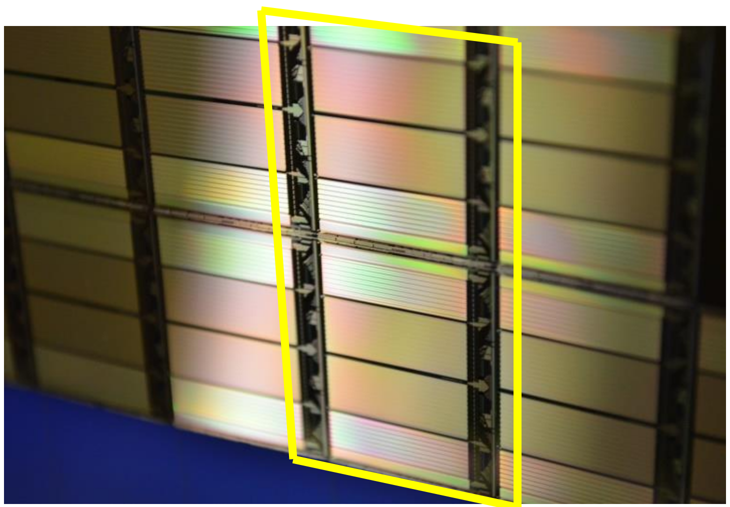

10,0µm

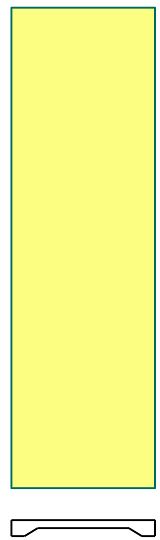
- Matrices can be configured
- We have tested one chip and it seems to work well. We see that it is possible to operate a pixel.



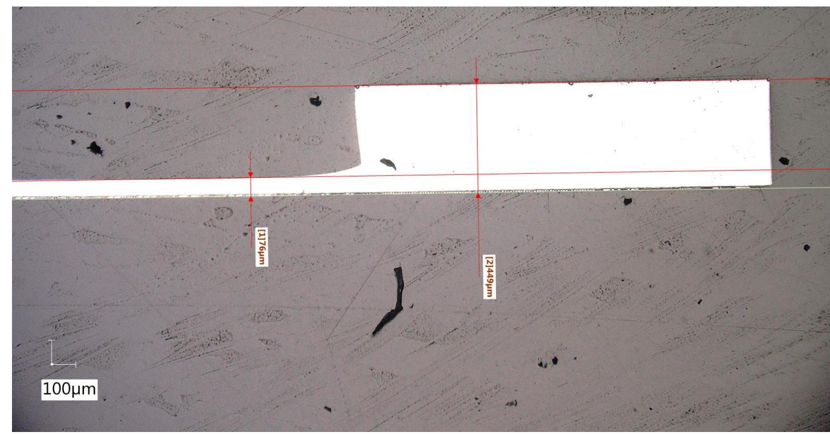
- Thinning and inter-reticle connections can be done at IZM
- First multichip sensor structure with the profile similar to DEPFET produced (only thinning)
- The module would be compatible with present mechanics

HV-CMOS pixel sensor in H35 technology





Thinning at IZM – first try



	Belle II DEPFET	HL - ATLAS layer 4 HVCMOS	Belle II upgrade HVCMOS
Trigger	20kHz (50µs)	Up to 4MHz (0.25µs)	200kHz (5µs) ?
Trigger latency	5µs	25µs	5µs ?
Time resolution	20µs	25ns	100ns
Occupancy	1 hit / cm^2 /25ns	1-2 hit / cm^2 /25ns	10 hits / cm^2 /25ns ?
Readout	Rolling shutter	Zero suppressed	Zero suppressed
Readout rate		$4cm^2$ * 2/25ns * 25ns/250ns = 0.8hits/25ns	$4cm^2$ * 10/25ns 100ns/5µs = 0.8hits/25ns

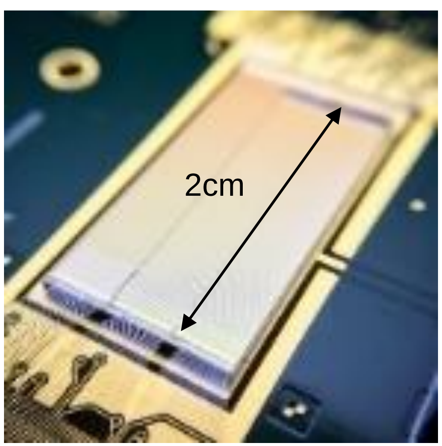
Summary

Summary

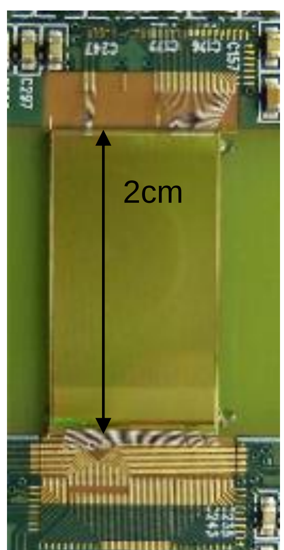
- HV-CMOS will be used for Mu3e experiment and is proposed for Layer 4 of ATLAS
- Mu3e requires production start in 2020 → technology will be ready in time
- Belle II sensor module can be based on the ATLAS and Mu3e sensor designs (similar hit rates)

Present status for ATLAS and Mu3e

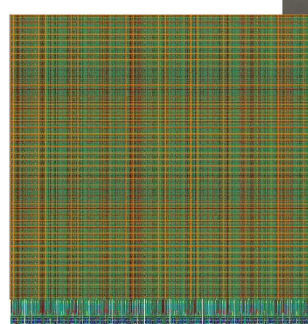
- We have successfully tested reticle-size sensors produced in 180nm HV-CMOS technology
- We have measured > 99% detection efficiency after proton and neutron irradiations
- Time resolution is of the order of RMS = 6ns (zero suppressed readout on pixel level with time measurement, not a rolling shutter)
- Power consumption depends on amplifier on-chip setting and can be ~ 100mW/cm^2 (switchers consume similar power presently)
- Several foundries can produce the sensors: TSI (main option) (TSI has done reticle stitching, engineering runs and wafers not expensive)
- Production of multireticle modules seems to be possible

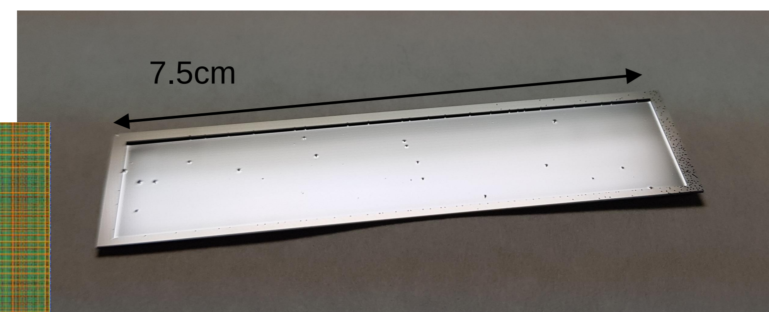


ATLASPix1



MuPix


ATLASPix3



H35DEMO thinned at IZM

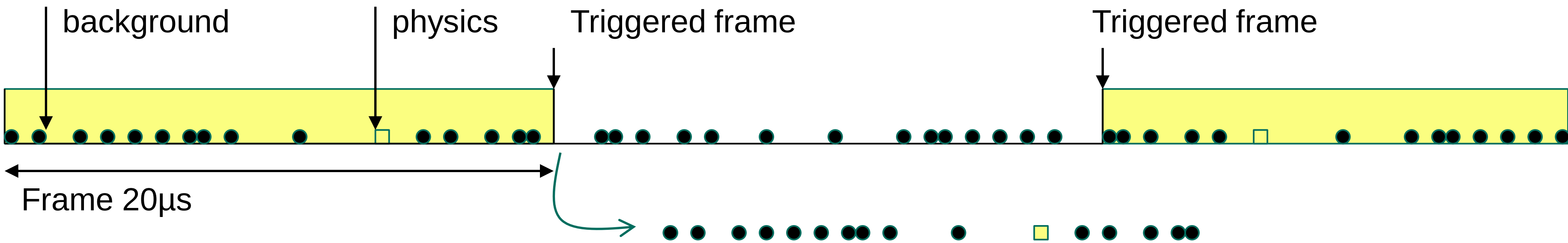
Proposed project plan

- We could submit a design for Belle II end of this year. The chip could have 50µm x 50µm pixel size, the pixel matrix could contain 250 x 400 pixels (1.25 cm x 2 cm). Comparators would be placed on periphery which reduces detector capacitance and power. Three metal layers would be used for routing of analog pixel signals, every layer with pitch of 0.6µm. In this way 250 pixel signals can be routed at 50µm width.
- Energy resolution could be 7 bits.
- Time resolution would be 50ns.
- The power consumption should be about 100mW/cm^2.
- The pixels would be 3x smaller in area than in the case of ATLASPIX. Low power consumption will be achieved by reduction of the detector capacitance by factor three. This can be achieved by the use of smaller pixel electrode and by placing of comparators at the chip periphery that leads to smaller p-well size and capacitance. Further, comparator power can be reduced if the time resolution is relaxed from 25ns (ATLASPIX) to 50ns (Belle II design).
- Crosstalk would be reduced by smart routing of signals, limiting of signal amplitude and by corrections in the digital part.
- After wafers with chips are produced we would send them to IZM, where the redistribution layer and cavities can be done.
- In 2020 we would have multi-reticle modules.
- Design could be used for pixel area and for vertex area.

Thank you!

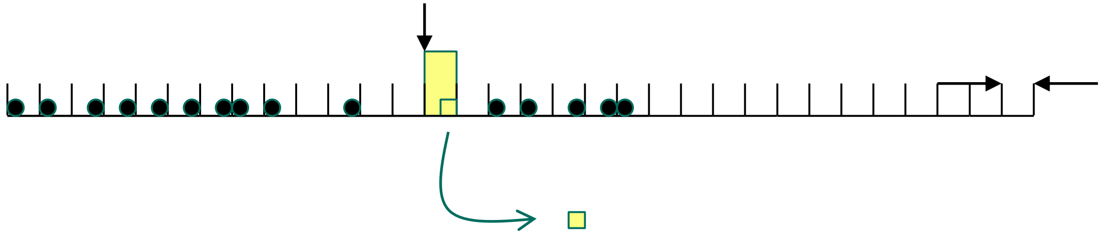
Backup slides

- HVCMOS sensor can cope with increased luminosity
- Slow pions can be detected by measuring amplitude



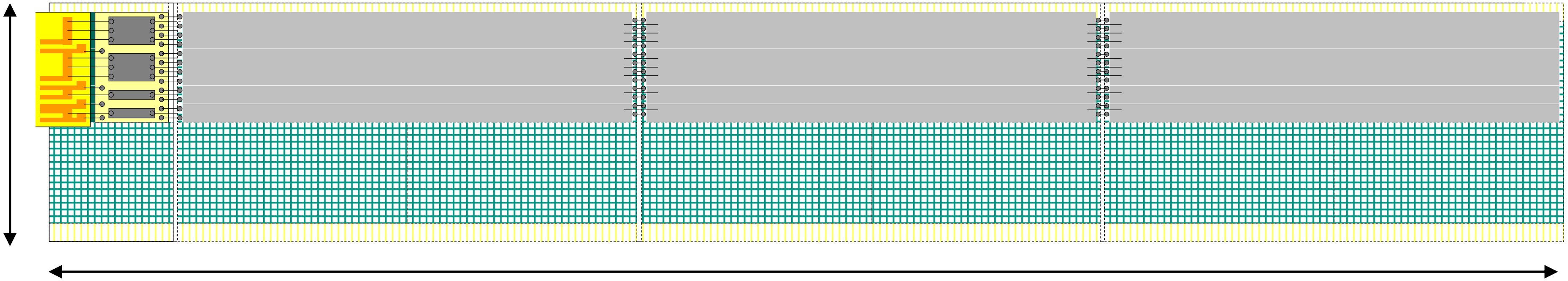
Triggered DEPFET frame: a few % of transmitted hits are relevant for physics, majority are background

Triggered HVCMOS event, nearly only hits relevant for physics are transmitted

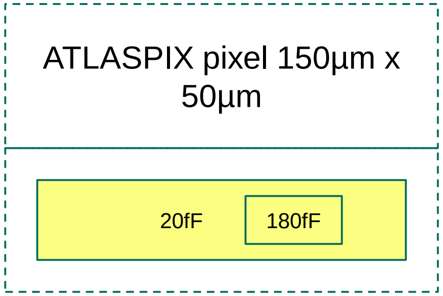


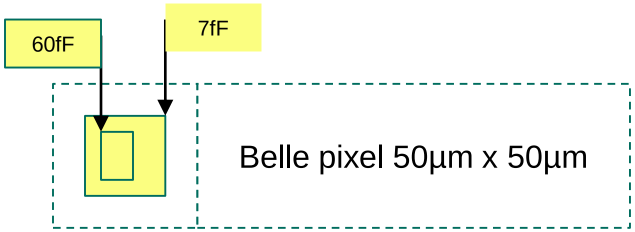
Triggered HVCMOS event, ~ only hits relevant for physics are transmitted

1 cm



Power estimation

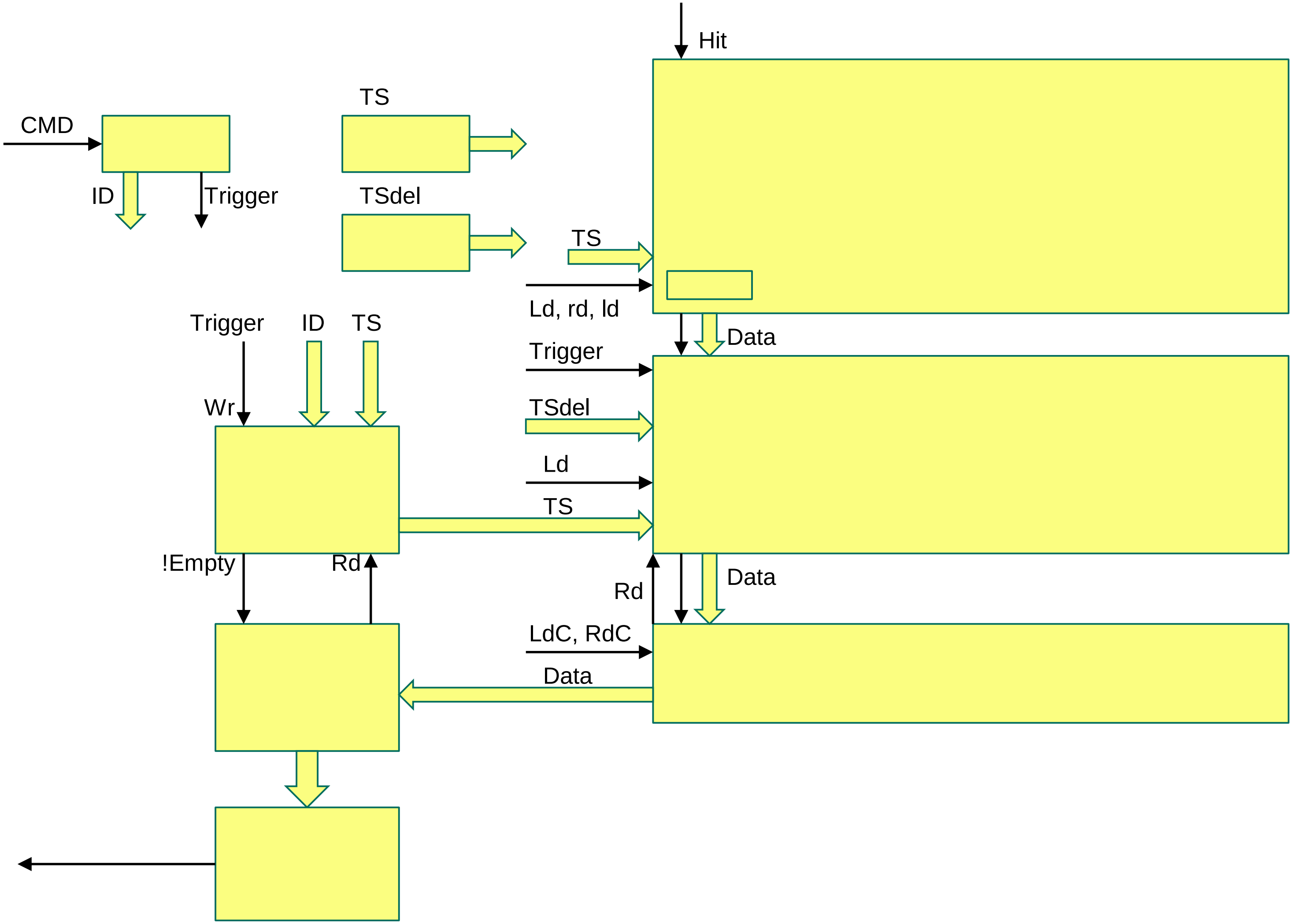


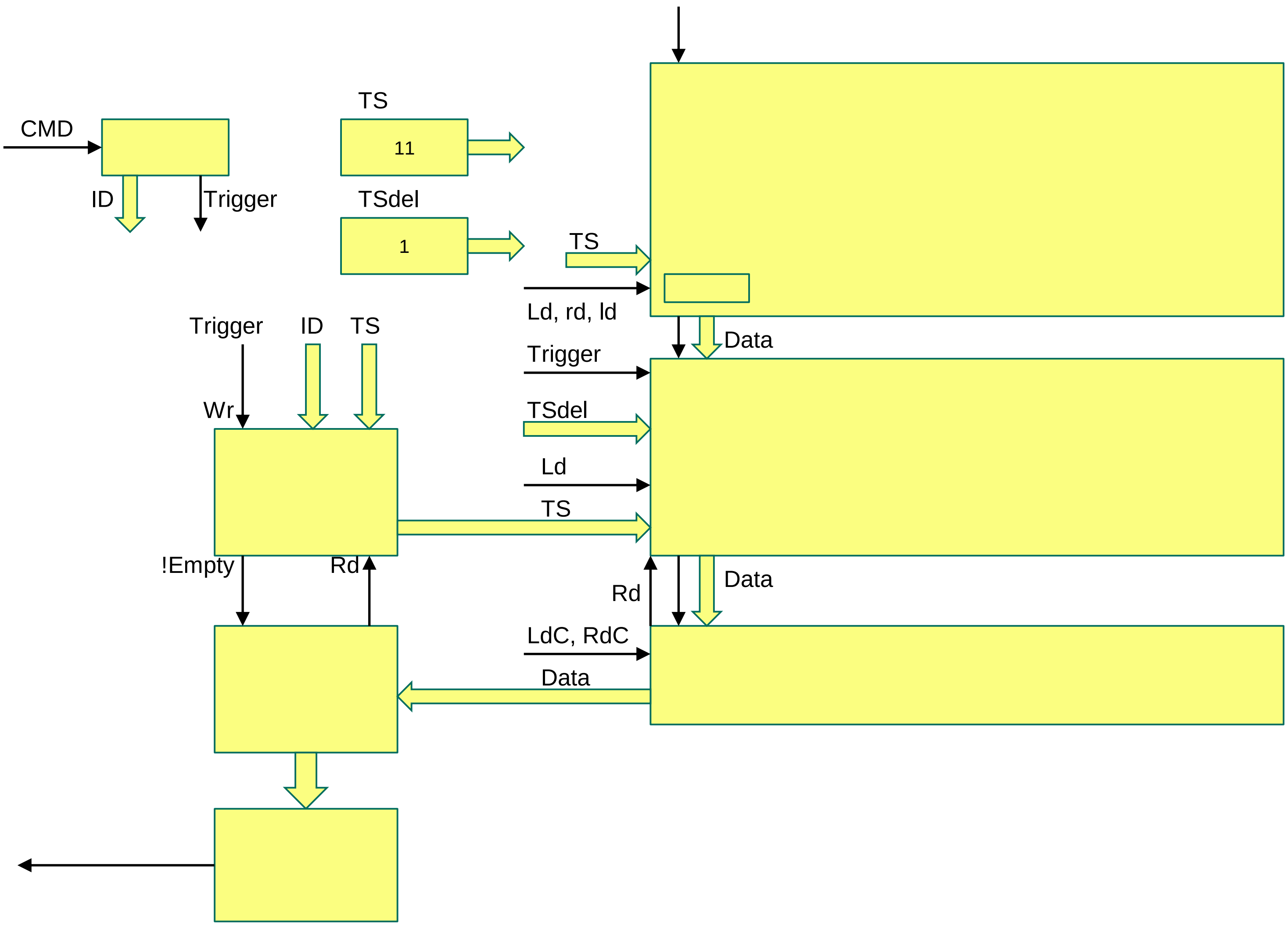


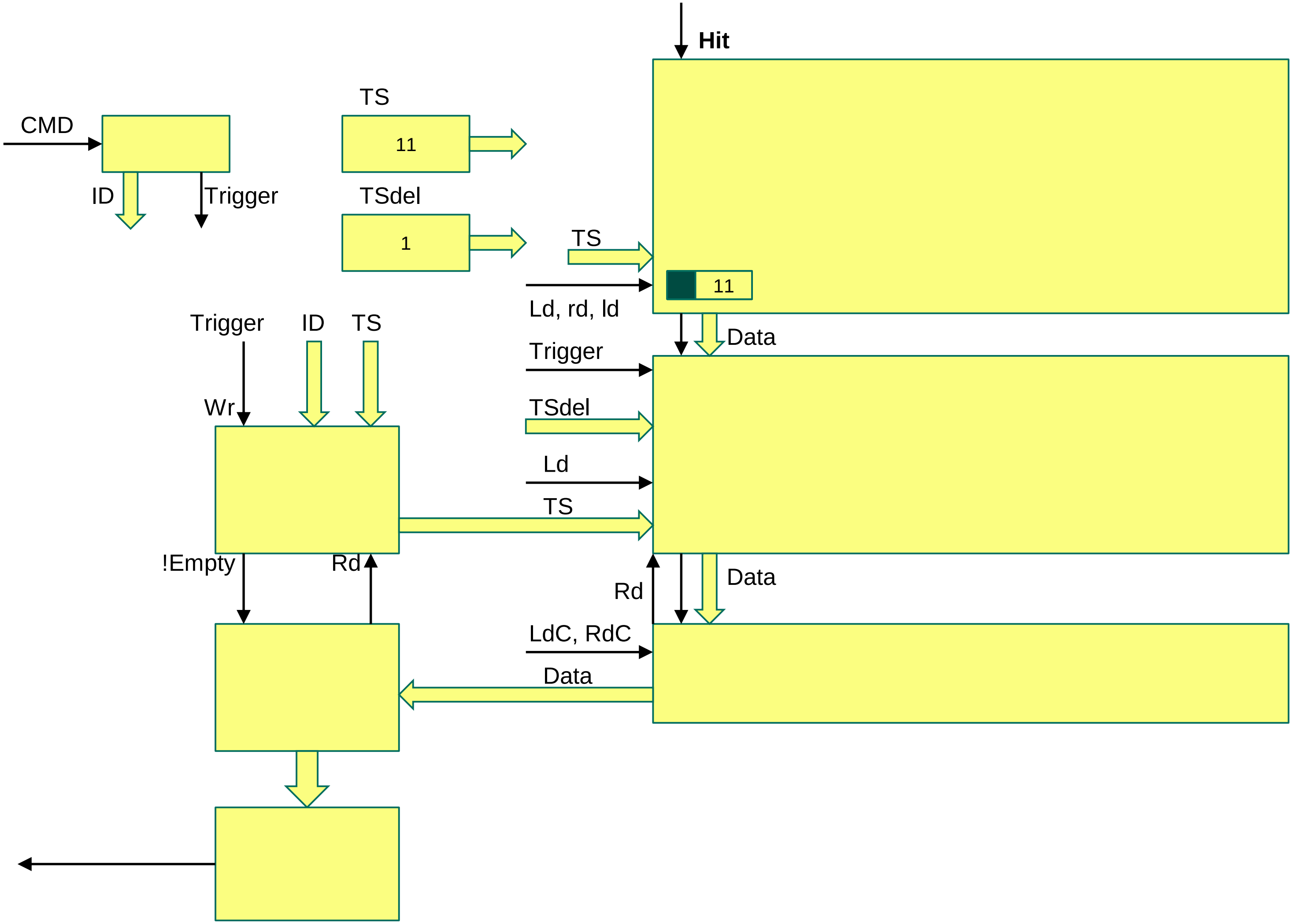
Circuit	ATLASPIX	Belle II	Comment
Amplifier	3.5µA (1.1V)	1.2µA (1.1V)	Amplifier power reduced because of reduced capacitance
Comparator	1.75µA (1.8V)	0.5µA (1.8V)	Comparator power reduced because of reduced time resolution and low power CMOS design
Total		200 x 200 x (1.8V x 0.5µA + 1.1V x 1.2µA) = 80mW/cm^2	

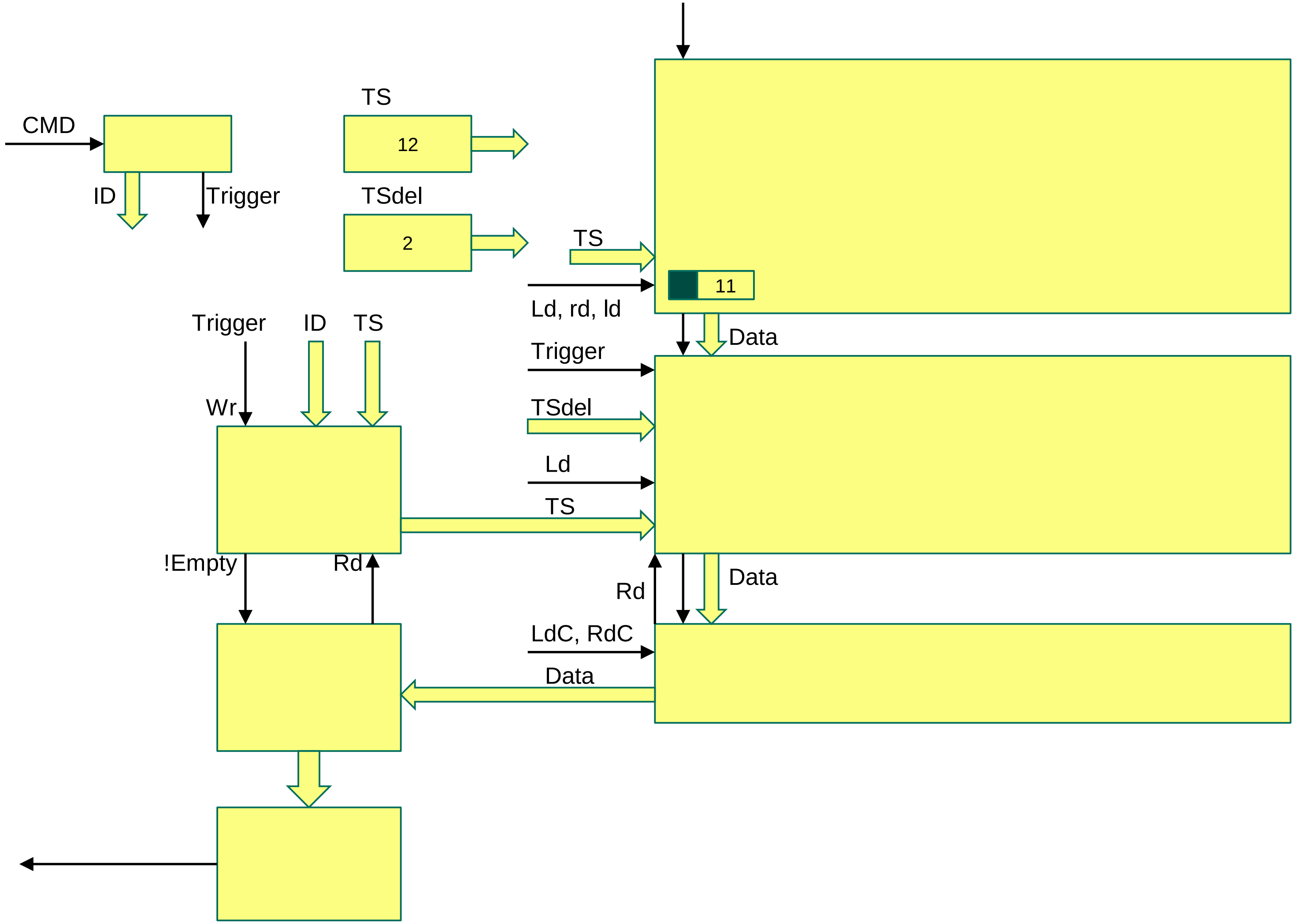
System

- CD system animation (1-level trigger scheme)

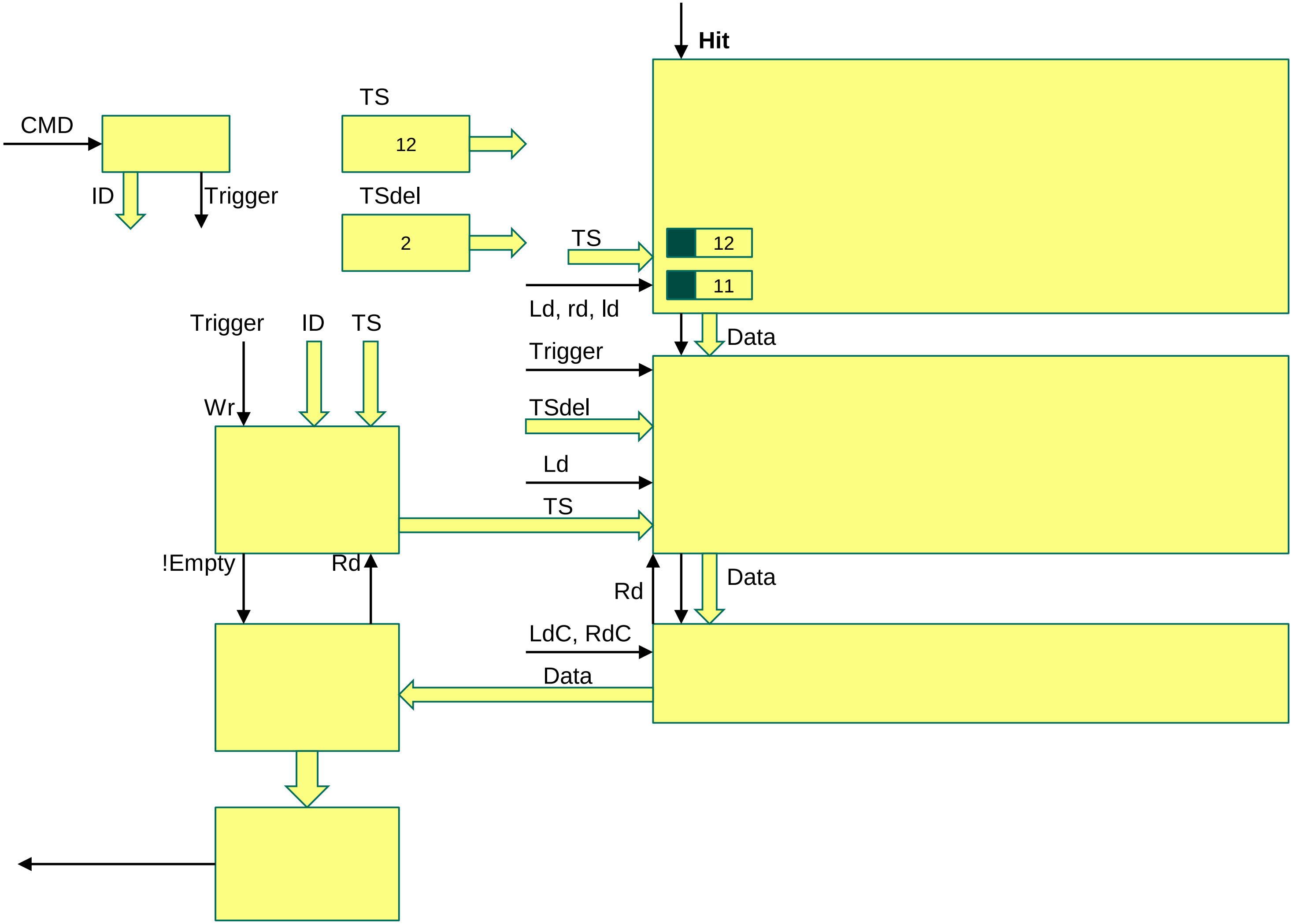

Hit
CMD
TS
ID
Trigger
TSdel
TS
Ld, rd, ld
Data
Trigger
ID
TS
Trigger
Wr
TSdel
Ld
TS
!Empty
Rd
Data
Rd
LdC, RdC
Data


CMD
ID
Trigger
TS
11
TSdel
1
TS
Ld, rd, ld
Data
Trigger
TSdel
Ld
TS
Trigger
ID
TS
Wr
!Empty
Rd
Rd
Data
LdC, RdC
Data

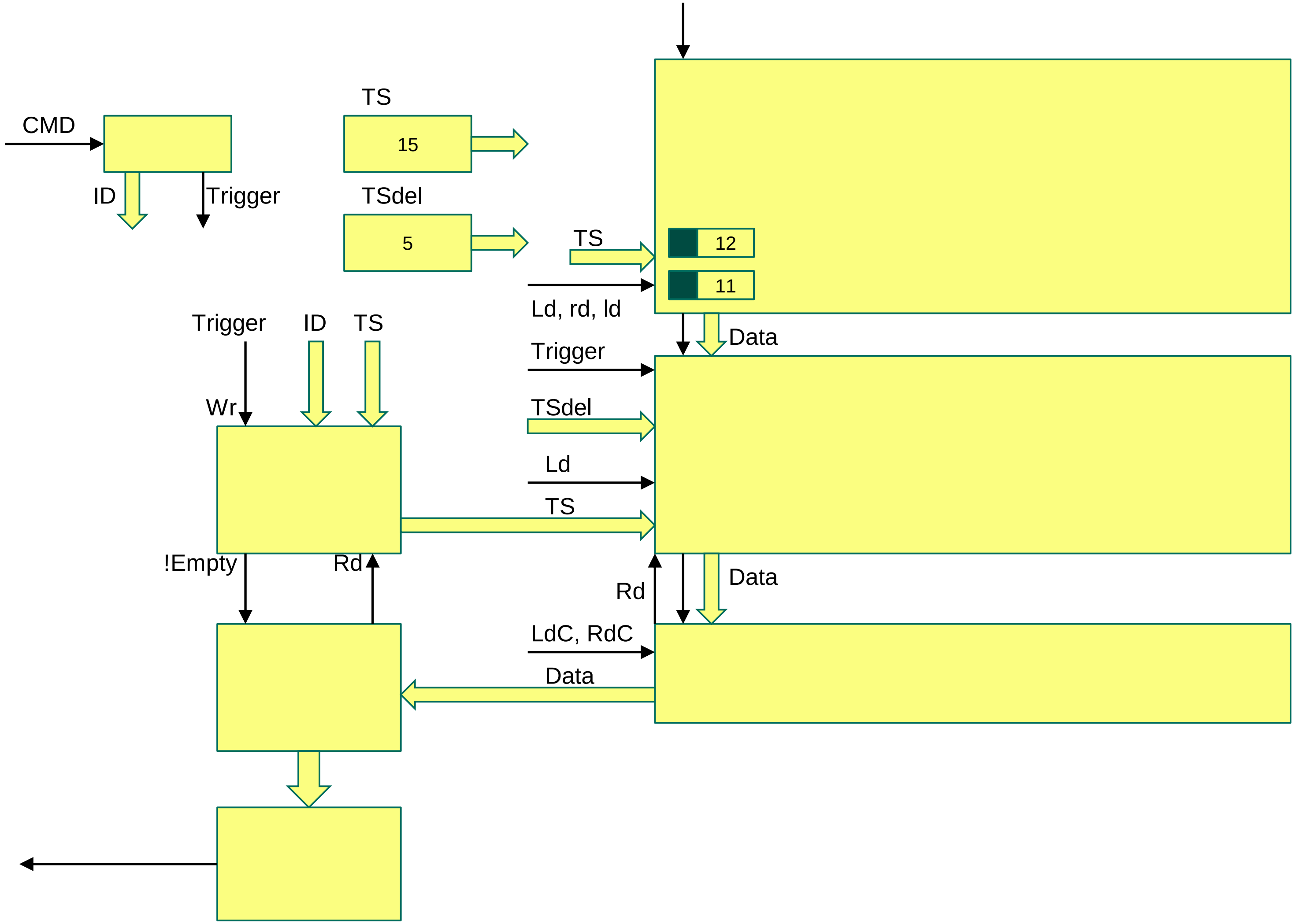

Hit
CMD
TS
11
ID
Trigger
TSdel
1
TS
11
Ld, rd, ld
Data
Trigger
ID
TS
Trigger
Wr
TSdel
Ld
TS
!Empty
Rd
Data
Rd
LdC, RdC
Data

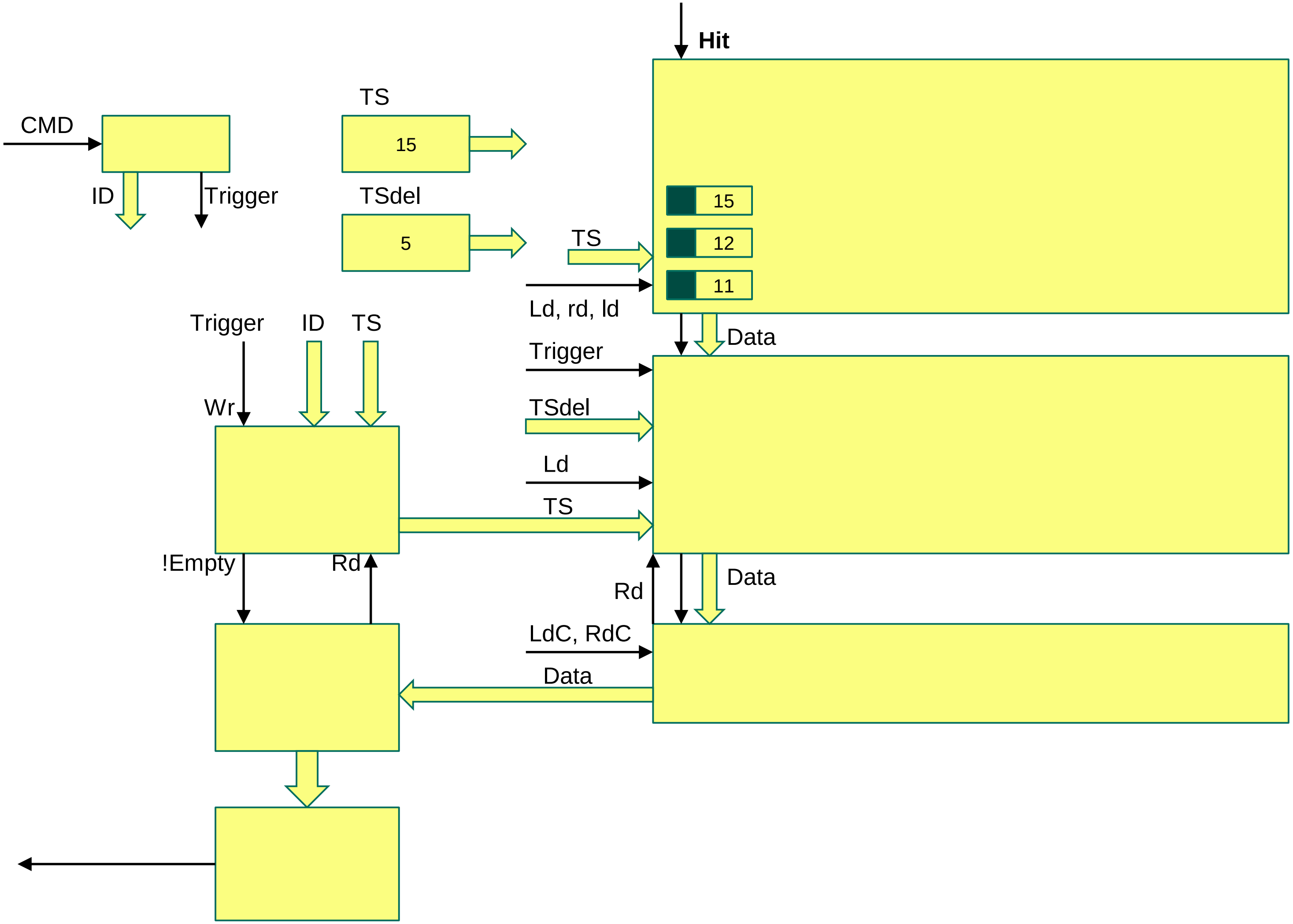

CMD
ID
Trigger
TS
12
TSdel
2
TS
11
Ld, rd, ld
Data
Trigger
ID
TS
Wr
Trigger
TSdel
Ld
TS
!Empty
Rd
Rd
Data
LdC, RdC
Data

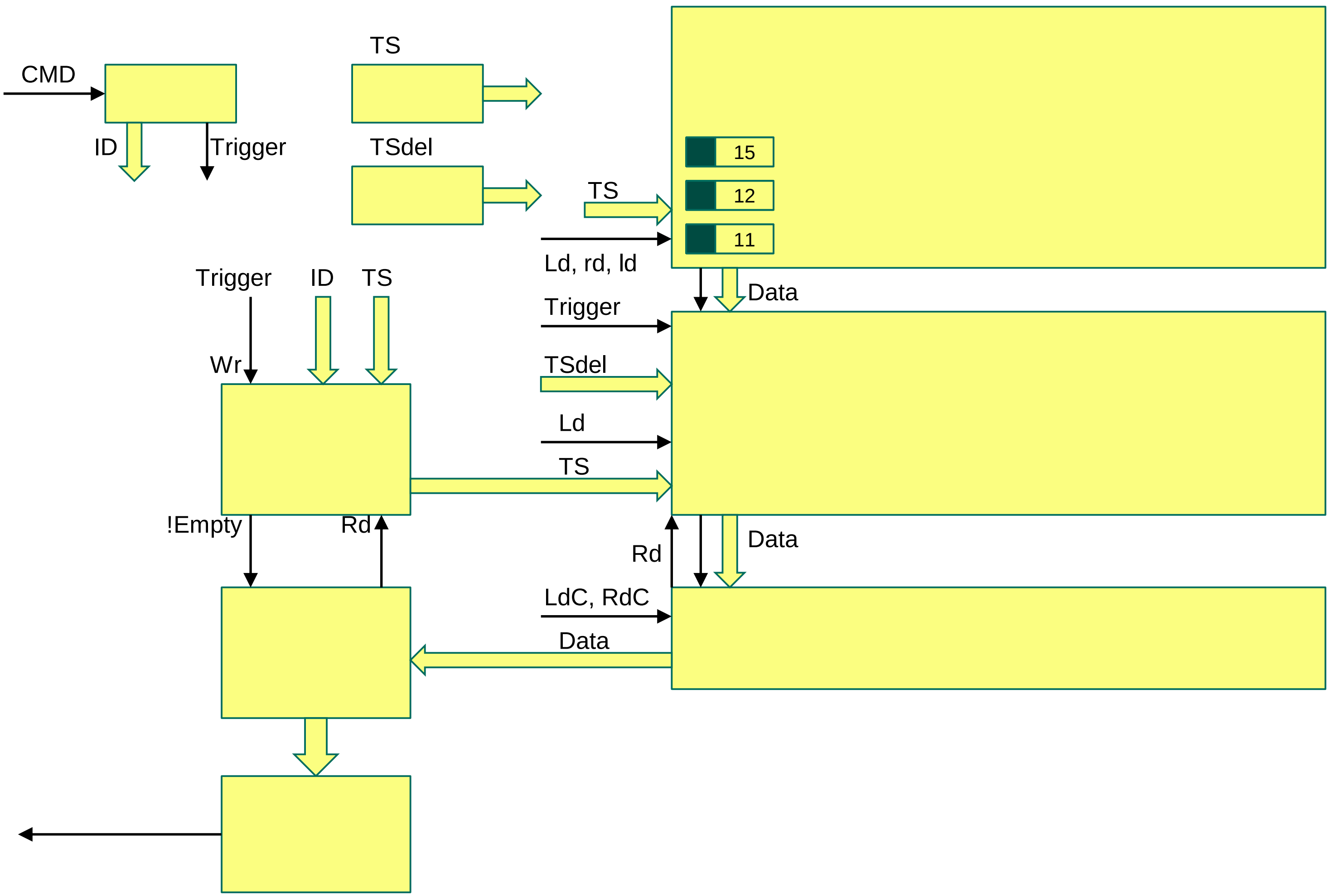
System

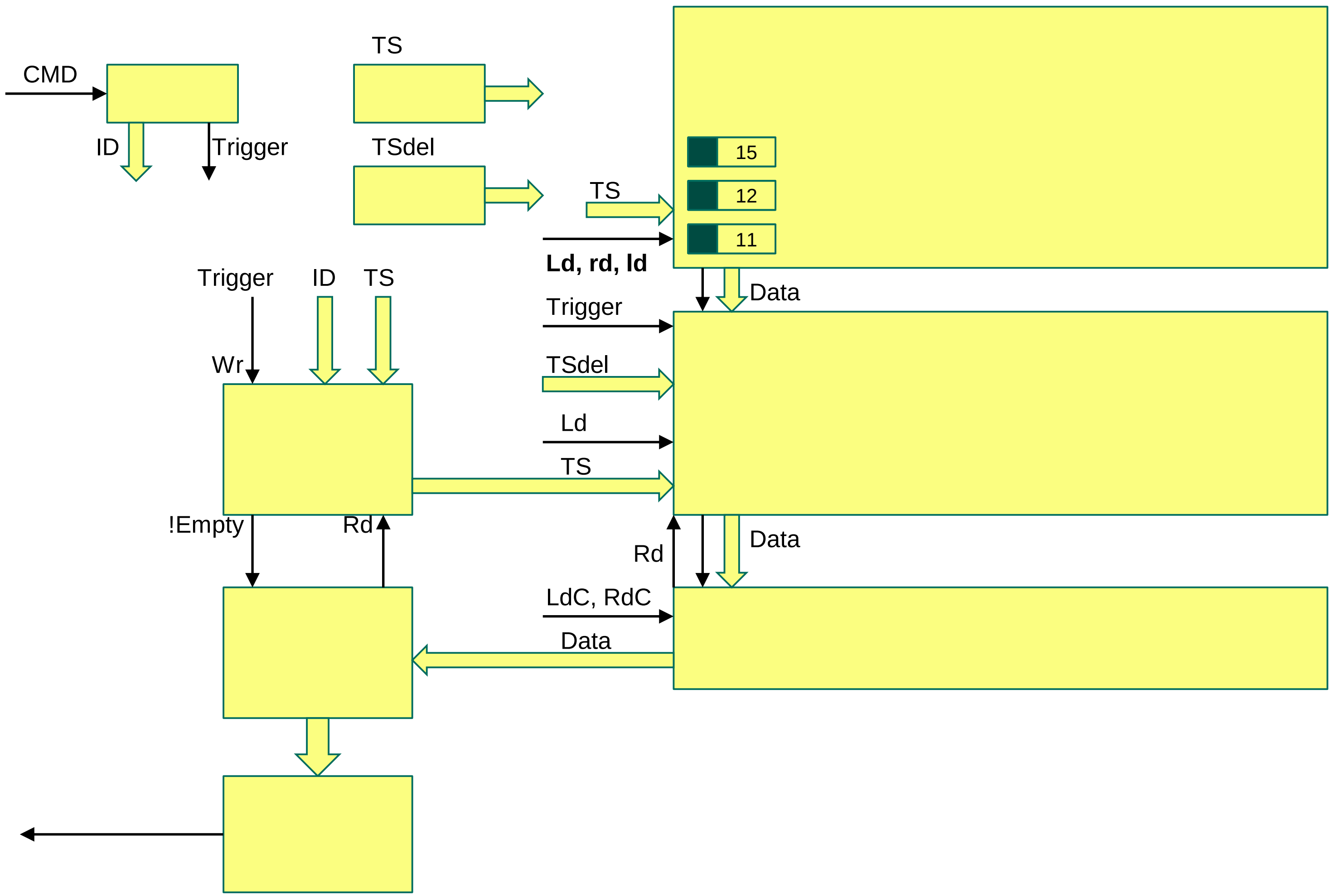


Hit
CMD
TS
12
ID
Trigger
TSdel
2
TS
12
11
Ld, rd, ld
Data
Trigger
ID
TS
Trigger
Wr
TSdel
Ld
TS
!Empty
Rd
Data
Rd
LdC, RdC
Data

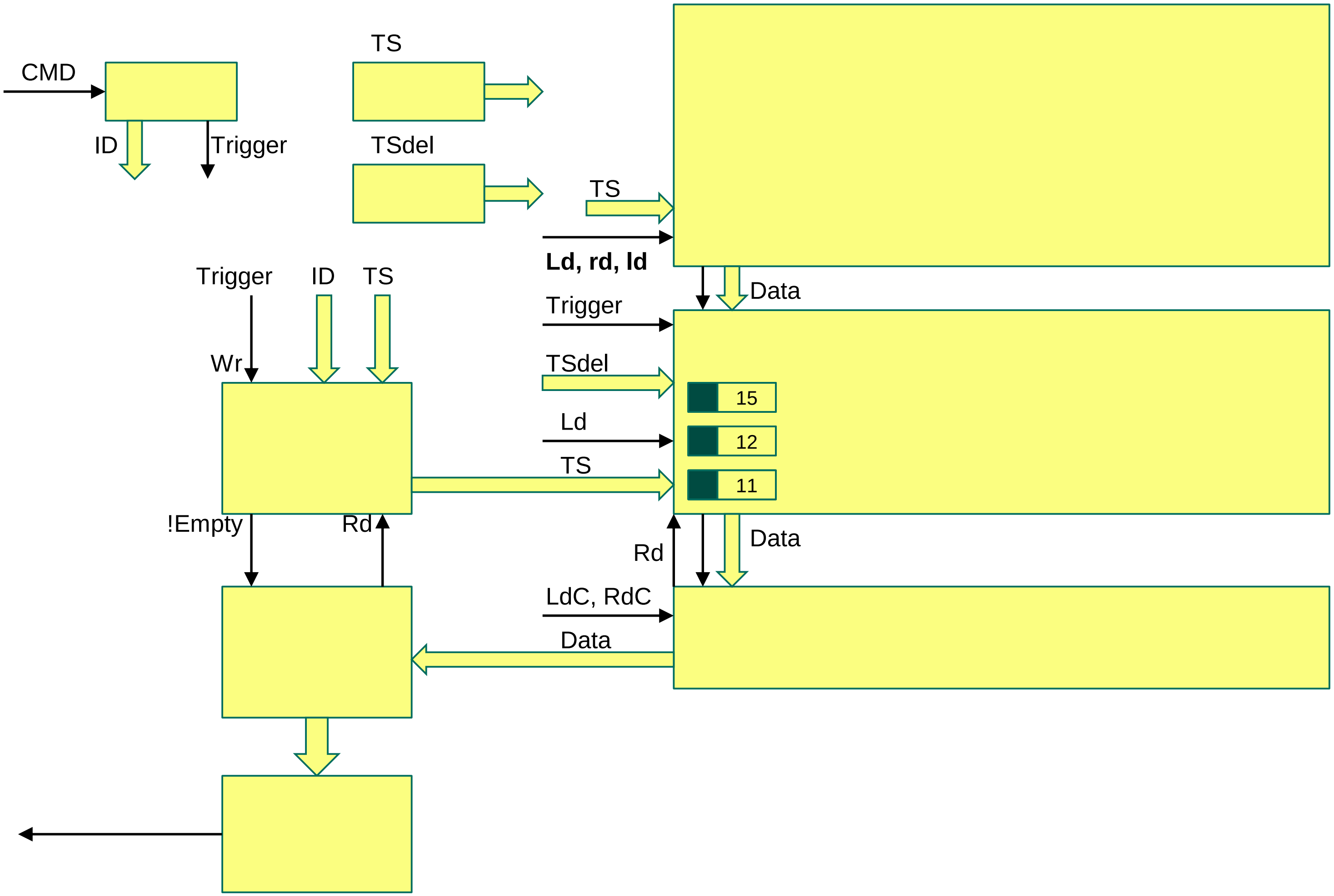

CMD
ID
Trigger
TS
15
TSdel
5
TS
12
11
Ld, rd, ld
Data
Trigger
ID
TS
Trigger
Wr
TSdel
Ld
TS
!Empty
Rd
Rd
Data
LdC, RdC
Data


Hit
CMD
TS
15
ID
Trigger
TSdel
5
15
12
11
TS
Ld, rd, ld
Data
Trigger
ID
TS
Trigger
Wr
TSdel
Ld
TS
!Empty
Rd
Data
Rd
LdC, RdC
Data

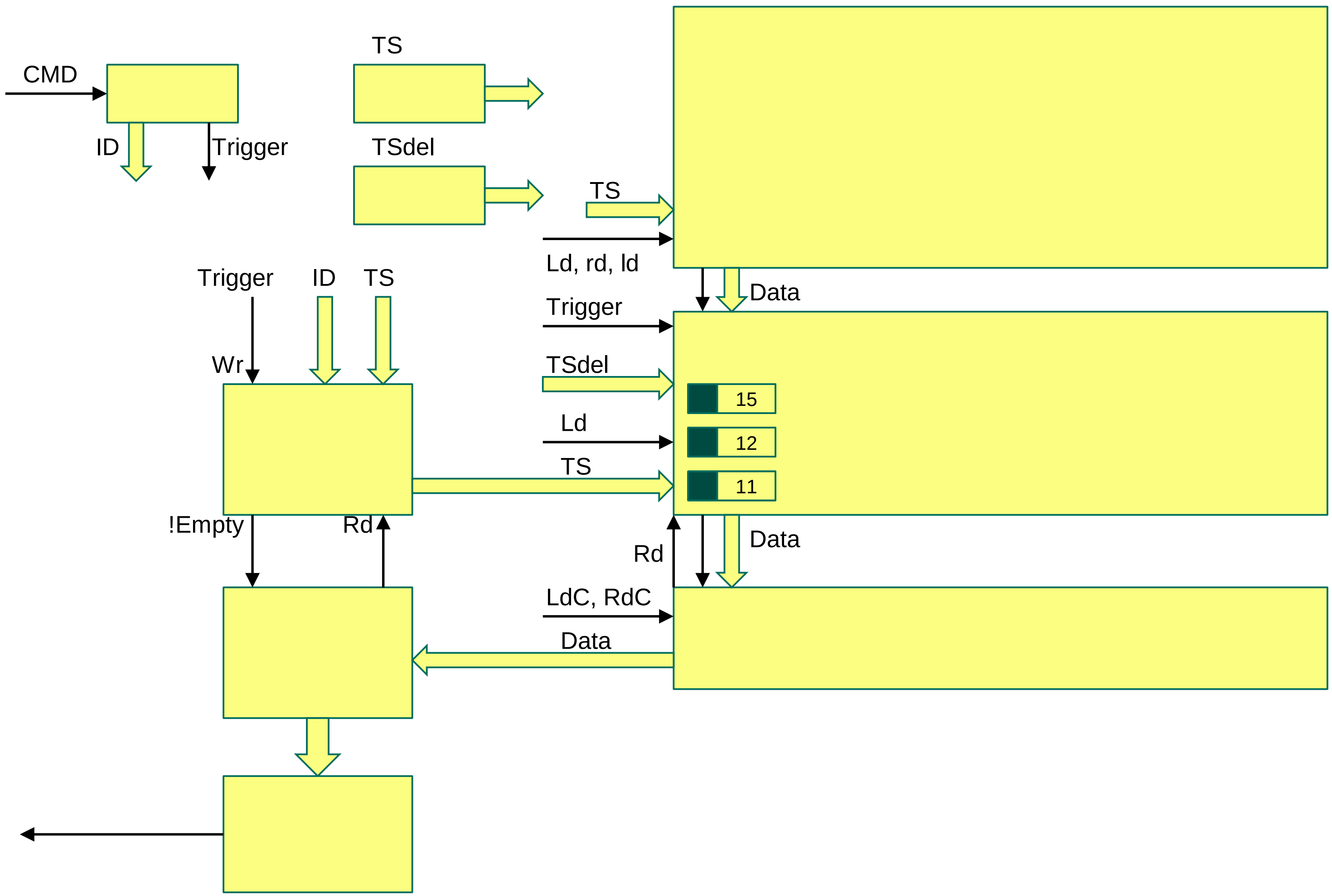

CMD
ID
Trigger
TS
TSdel
TS
15
12
11
Ld, rd, ld
Data
Trigger
ID
TS
Trigger
Wr
TSdel
Ld
TS
!Empty
Rd
Rd
Data
LdC, RdC
Data


CMD
ID
Trigger
TS
TSdel
TS
15
12
11
Ld, rd, ld
Data
Trigger
ID
TS
Trigger
Wr
TSdel
Ld
TS
!Empty
Rd
Data
Rd
LdC, RdC
Data

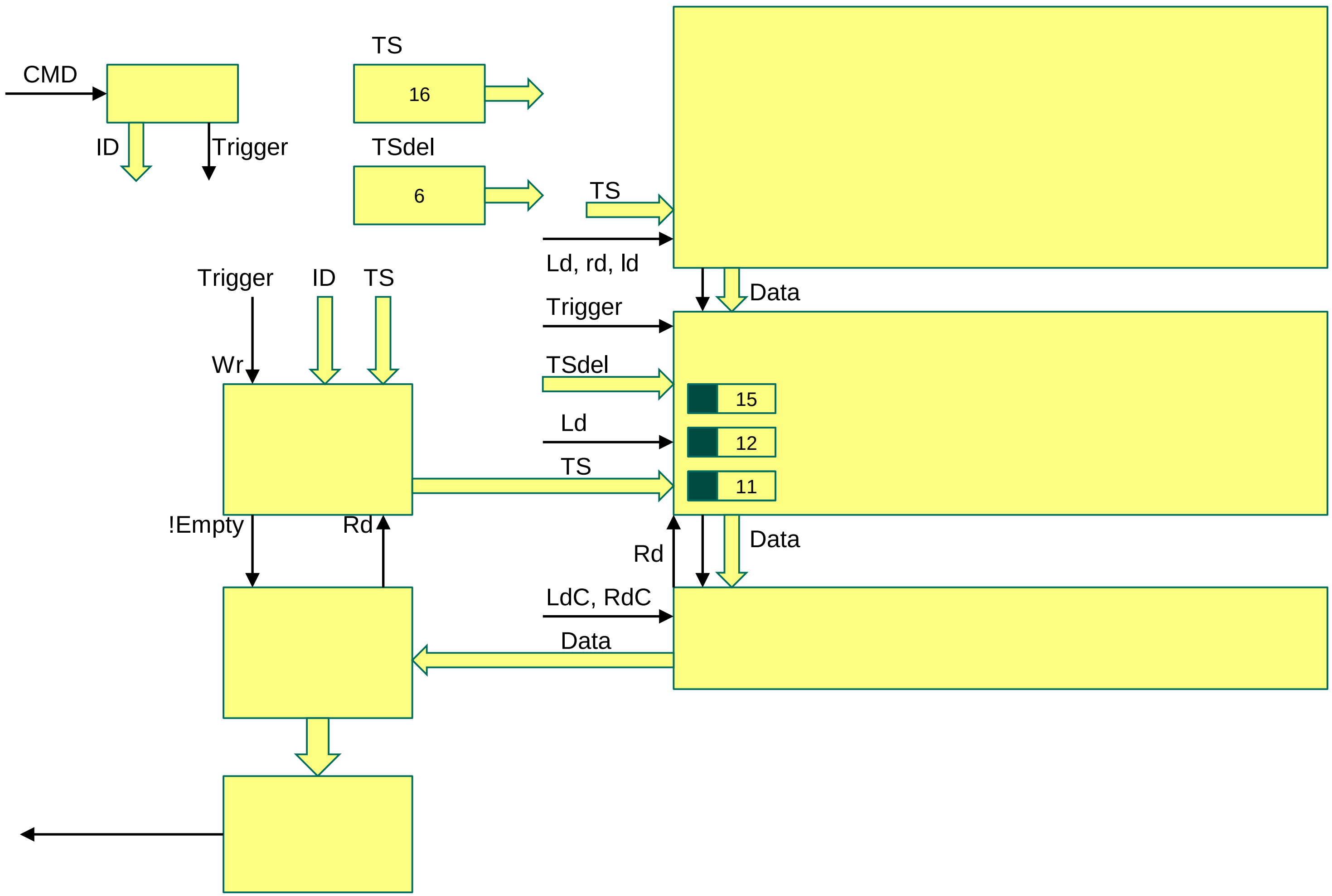
System



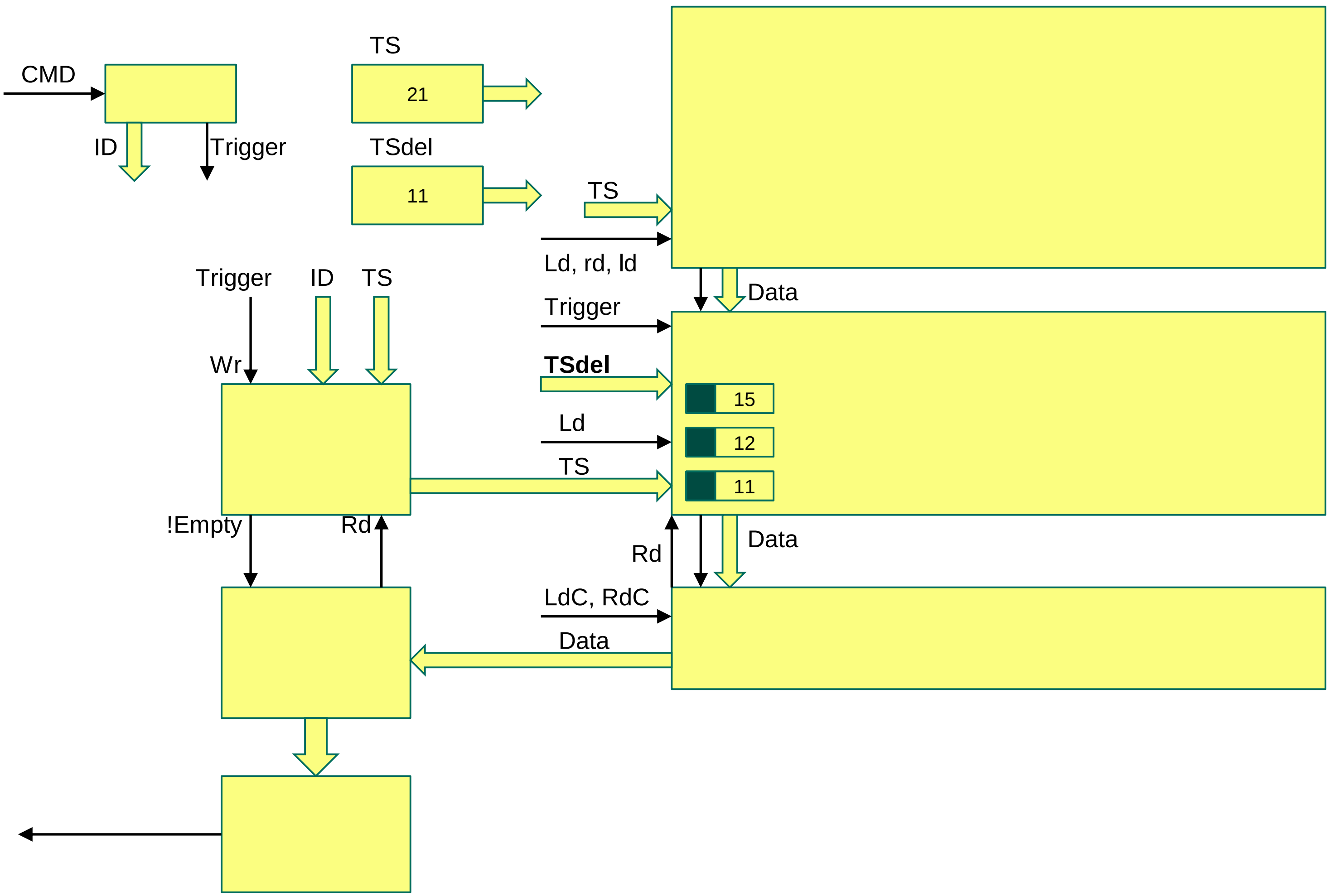
CMD
ID
Trigger
TS
TSdel
TS
Ld, rd, ld
Data
Trigger
ID
TS
Trigger
Wr
TSdel
15
Ld
12
TS
11
!Empty
Rd
Rd
Data
LdC, RdC
Data


CMD
ID
Trigger
TS
TSdel
TS
Ld, rd, ld
Data
Trigger
ID
TS
Trigger
Wr
TSdel
15
Ld
12
TS
11
!Empty
Rd
Data
Rd
LdC, RdC
Data

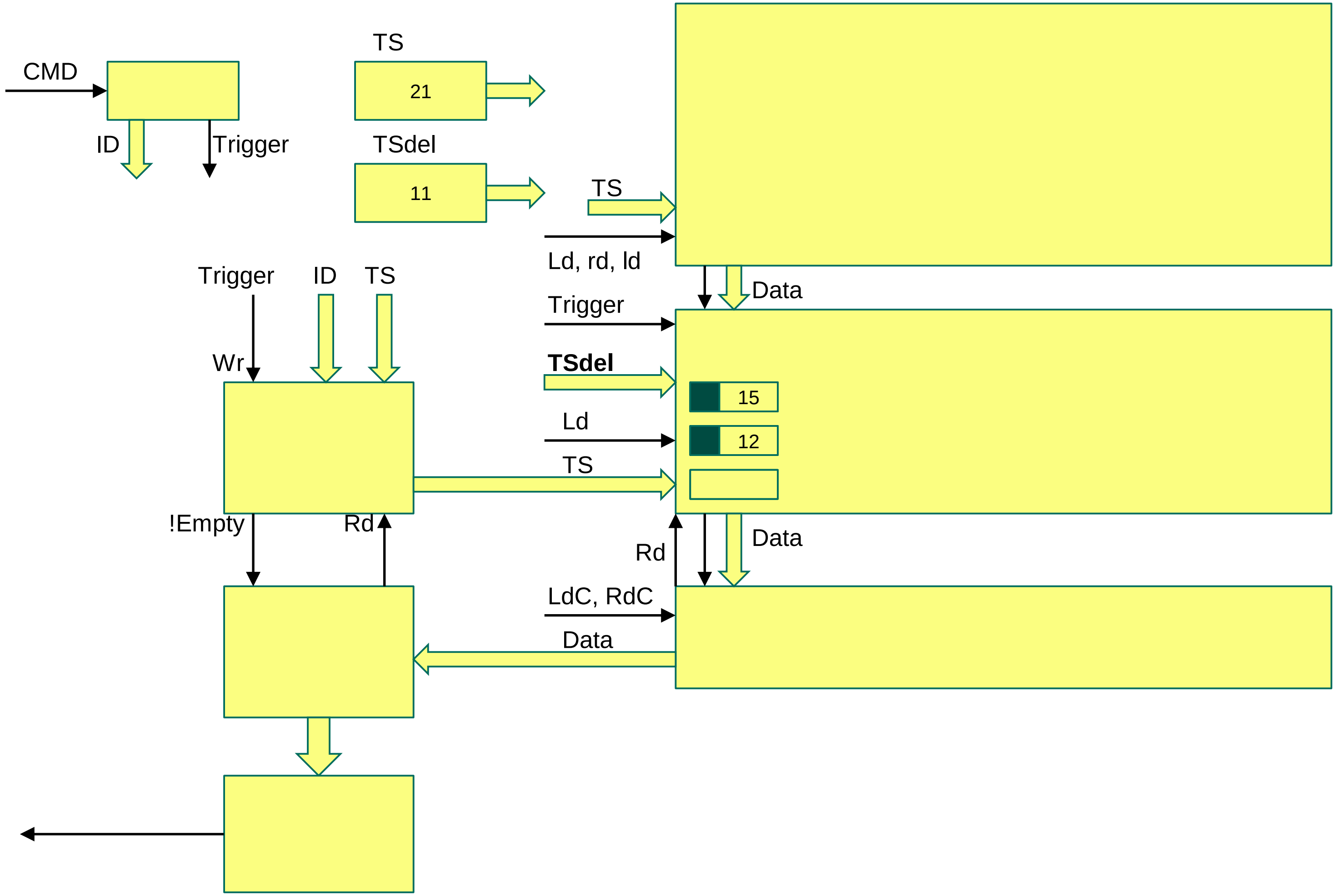
System



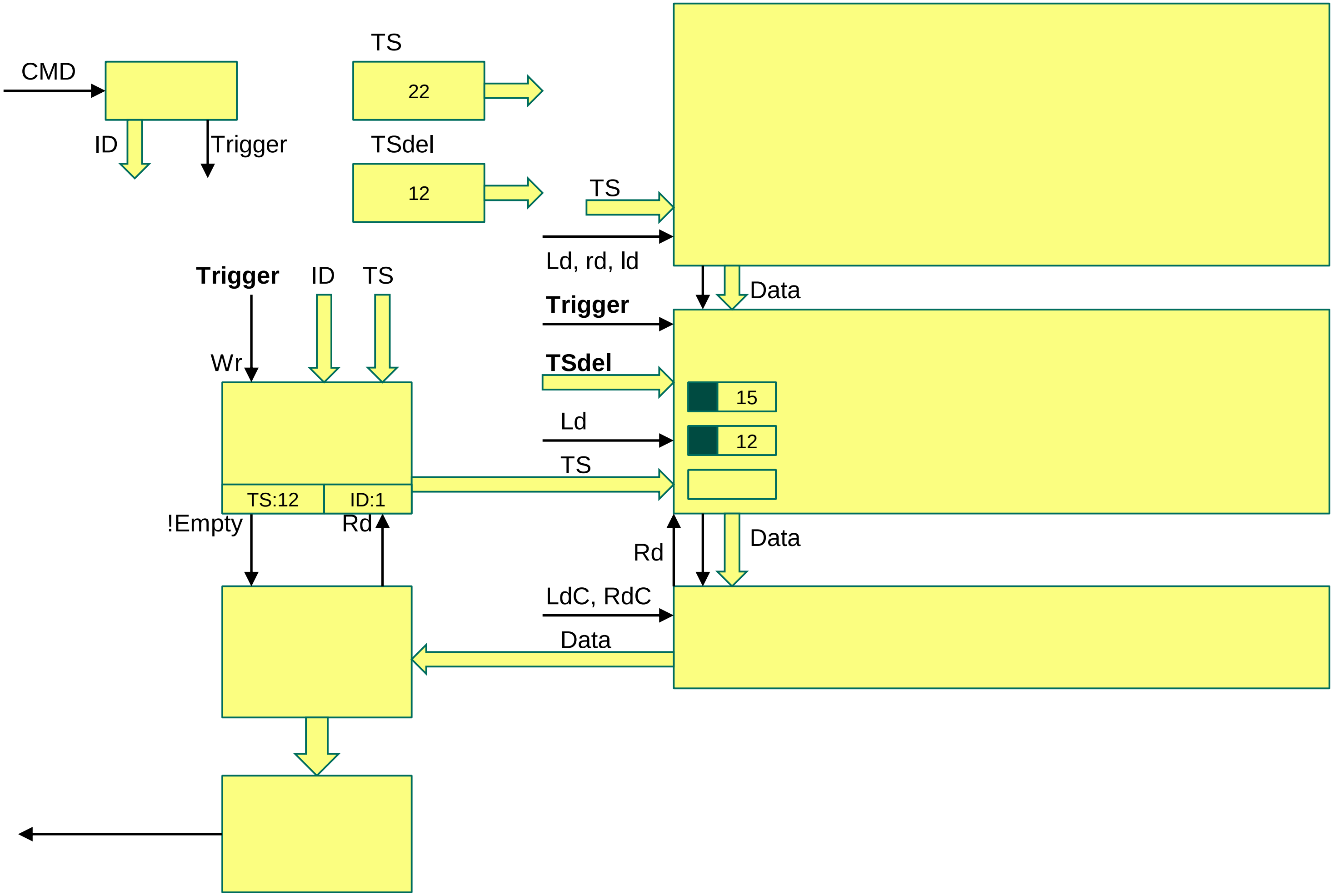
CMD
ID
Trigger
TS
16
TSdel
6
TS
Ld, rd, ld
Data
Trigger
ID
TS
Trigger
Wr
TSdel
15
Ld
12
TS
11
!Empty
Rd
Rd
Data
LdC, RdC
Data


CMD
ID
Trigger
TS
21
TSdel
11
TS
Ld, rd, ld
Trigger
ID
TS
Wr
Data
Trigger
TSdel
15
Ld
12
TS
11
!Empty
Rd
Data
Rd
LdC, RdC
Data

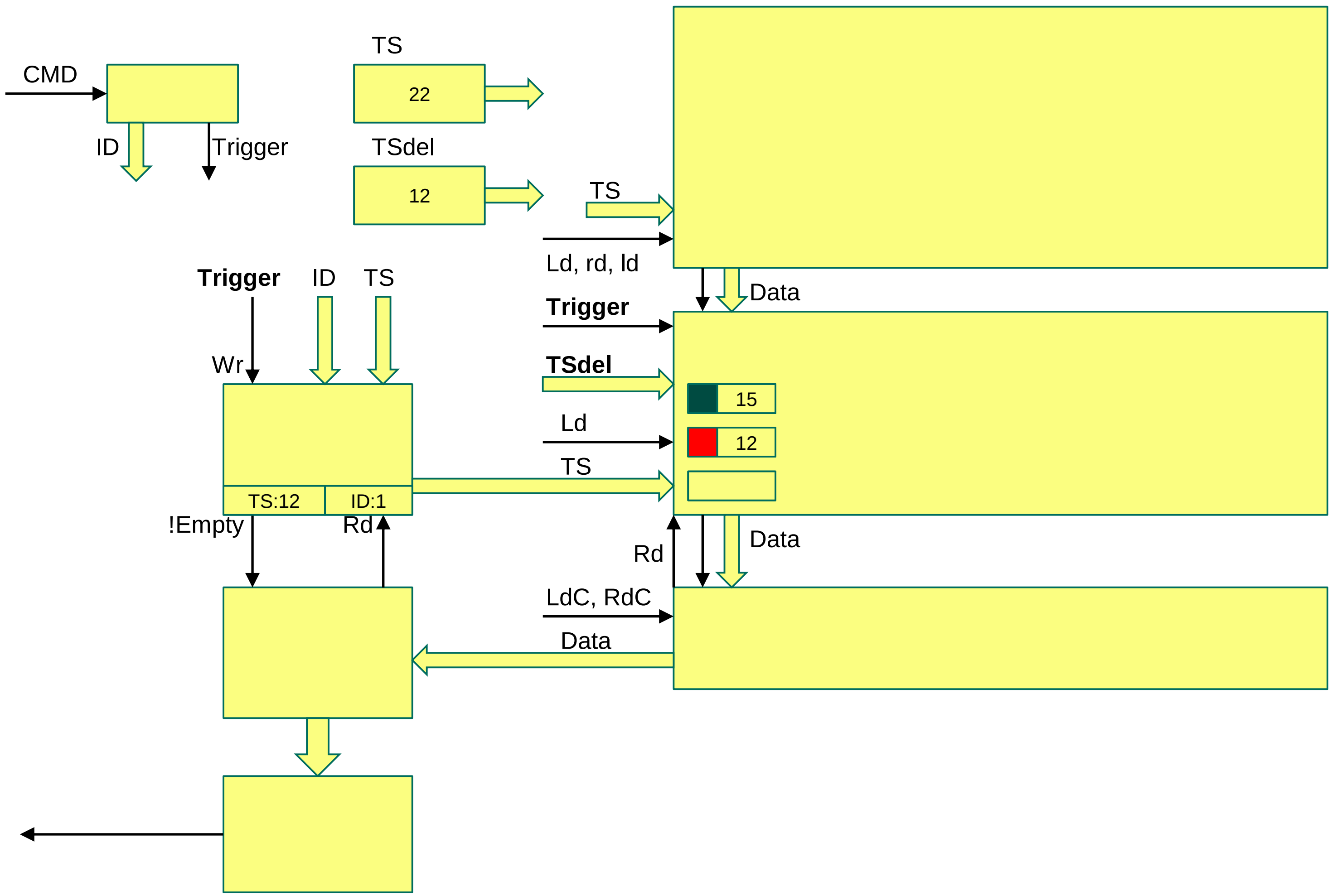
System



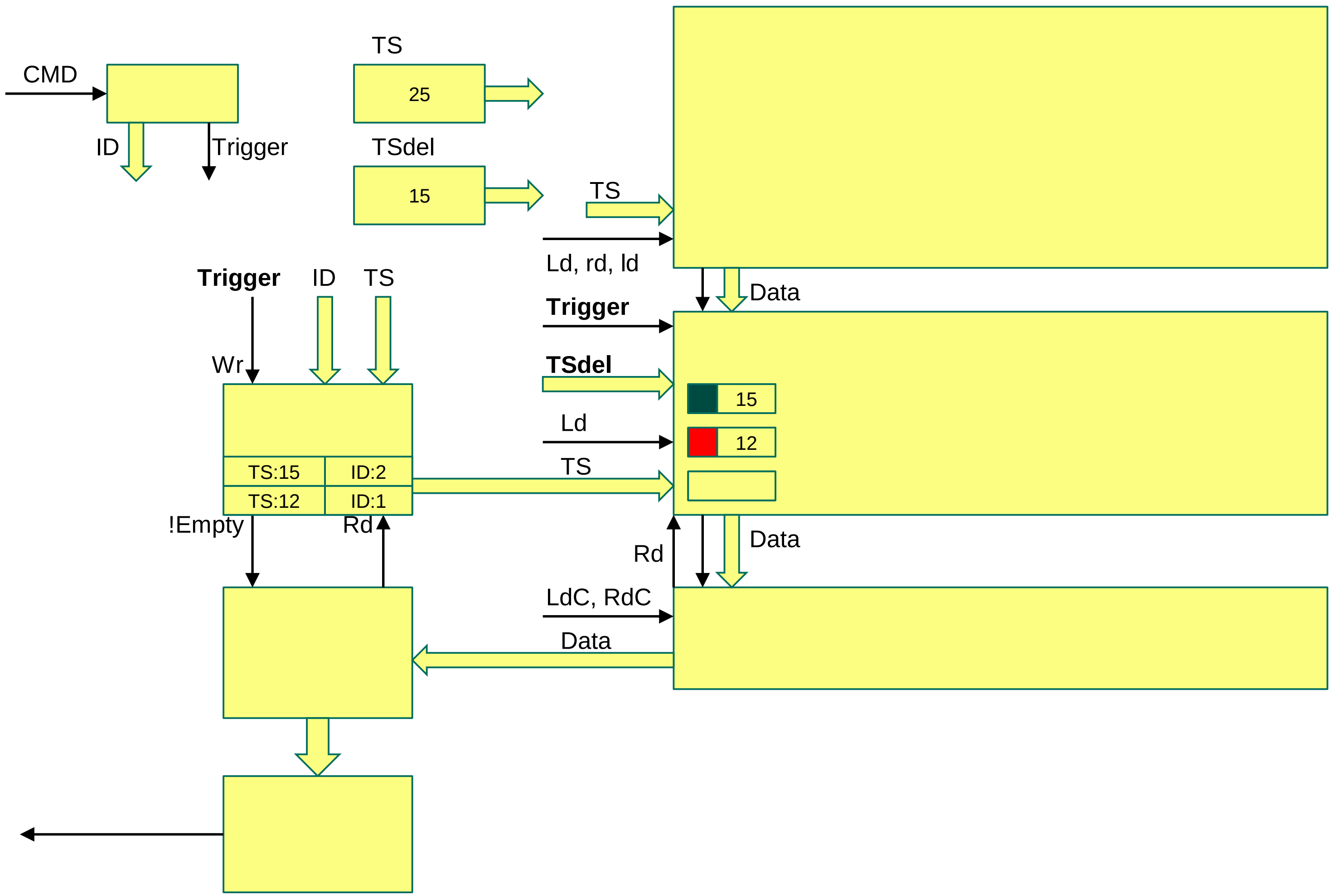
CMD
ID
Trigger
TS
21
TSdel
11
TS
Ld, rd, ld
Data
Trigger
ID
TS
Trigger
Wr
TSdel
15
Ld
12
TS
!Empty
Rd
Data
Rd
LdC, RdC
Data


CMD
ID
Trigger
TS
22
TSdel
12
TS
Ld, rd, ld
Data
Trigger
ID
TS
Wr
Trigger
TSdel
15
12
Ld
TS
TS:12
ID:1
!Empty
Rd
Rd
Data
LdC, RdC
Data

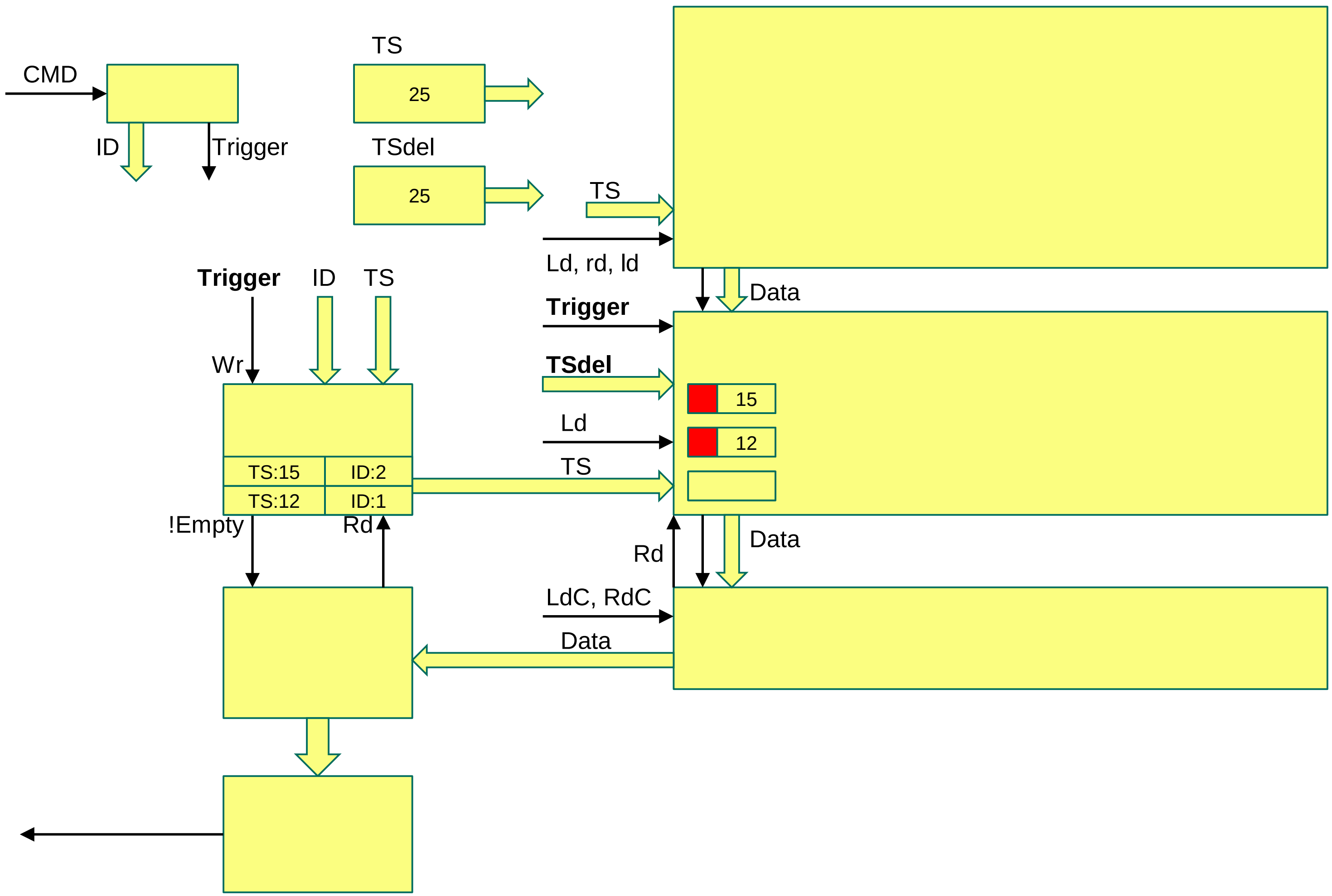
System



CMD
ID
Trigger
TS
22
TSdel
12
TS
Ld, rd, ld
Data
Trigger
ID
TS
Wr
Trigger
TSdel
15
12
Ld
TS
TS:12
ID:1
!Empty
Rd
Rd
Data
LdC, RdC
Data

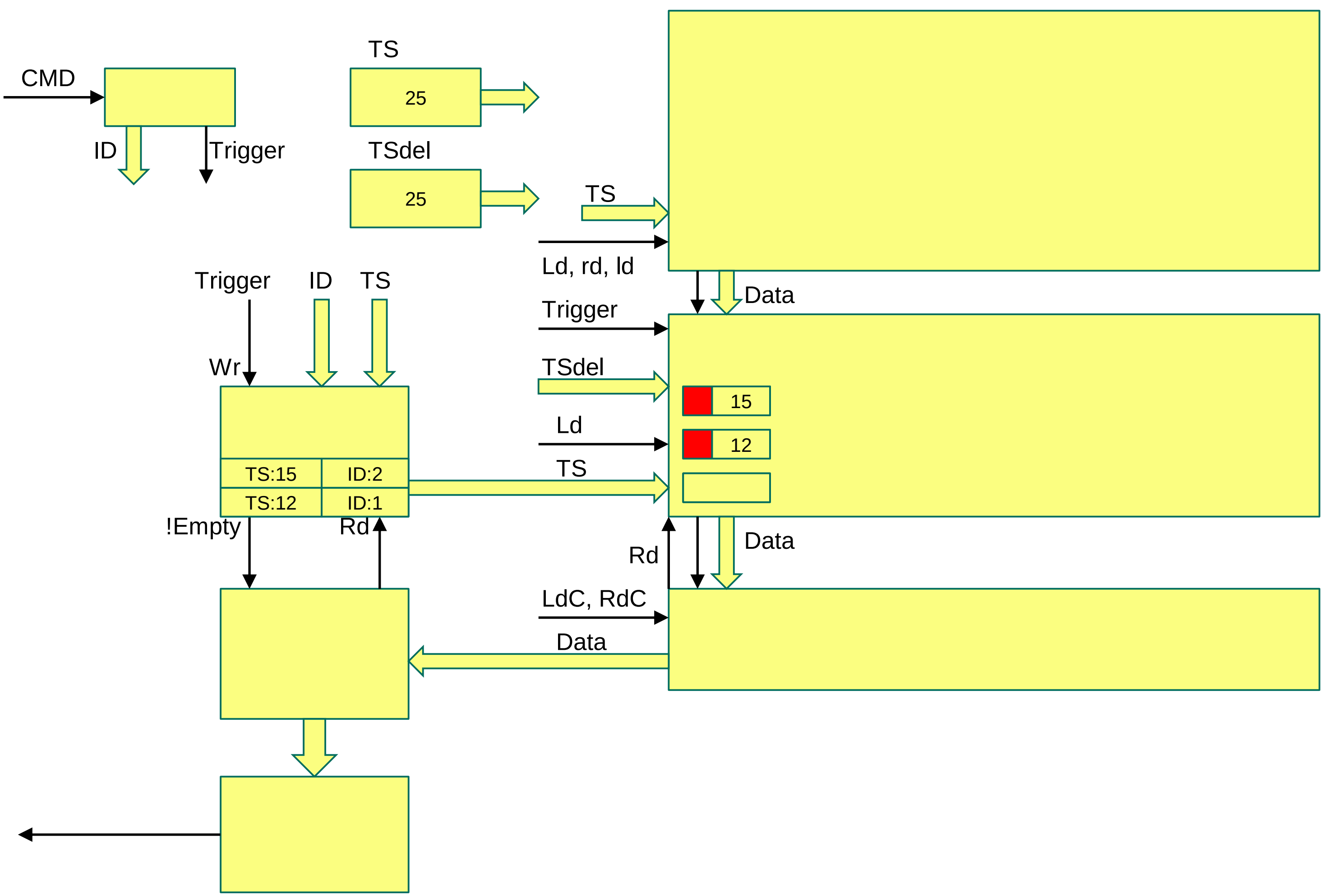


TS
CMD
25
ID
Trigger
TSdel
15
TS
Ld, rd, ld
Trigger
ID
TS
Data
Trigger
Wr
TSdel
15
Ld
12
TS
TS:15
ID:2
TS:12
ID:1
!Empty
Rd
Data
Rd
LdC, RdC
Data

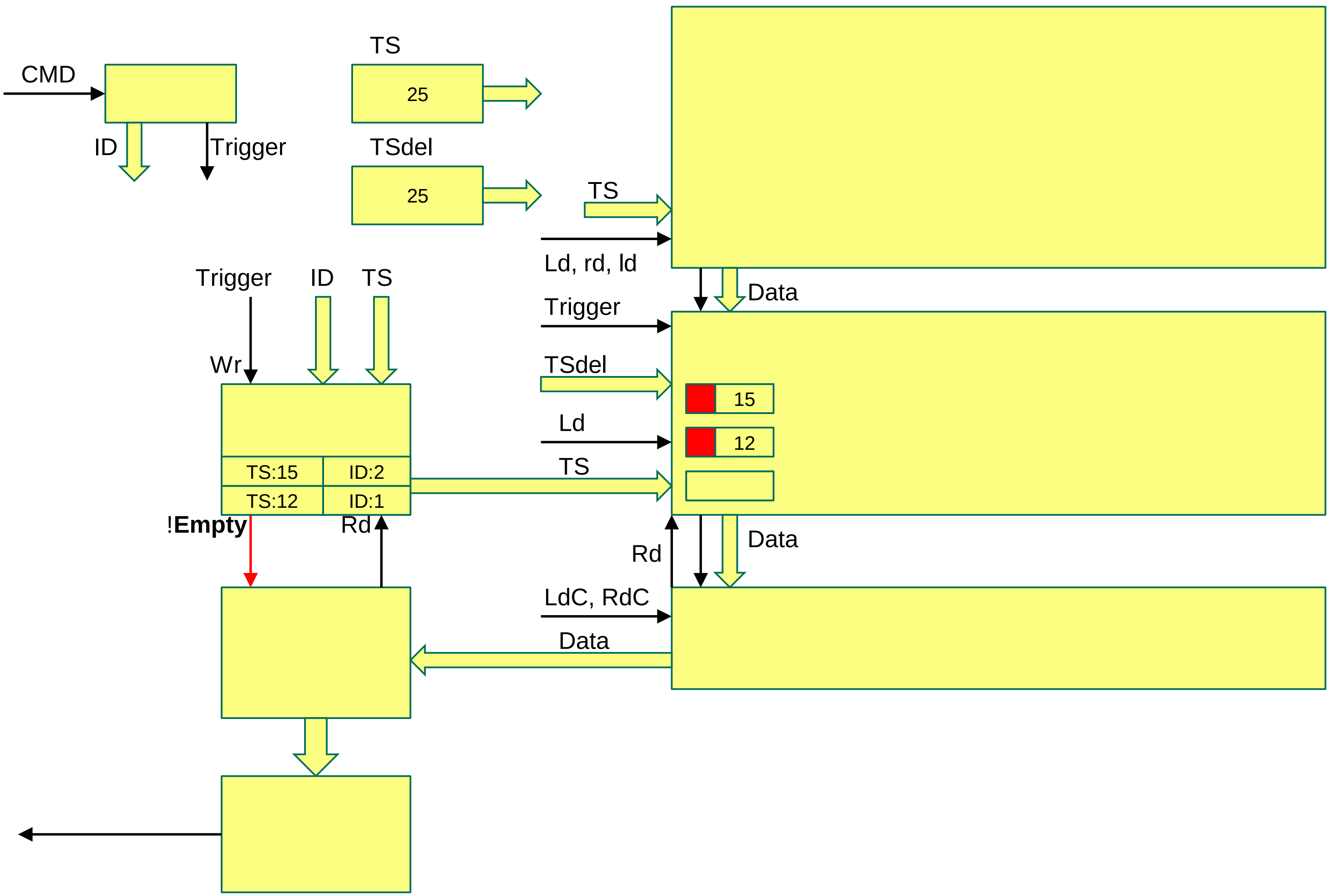


CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Data
Trigger
ID
TS
Trigger
Wr
TSdel
15
12
Ld
TS
TS:15
ID:2
TS:12
ID:1
!Empty
Rd
Data
Rd
LdC, RdC
Data

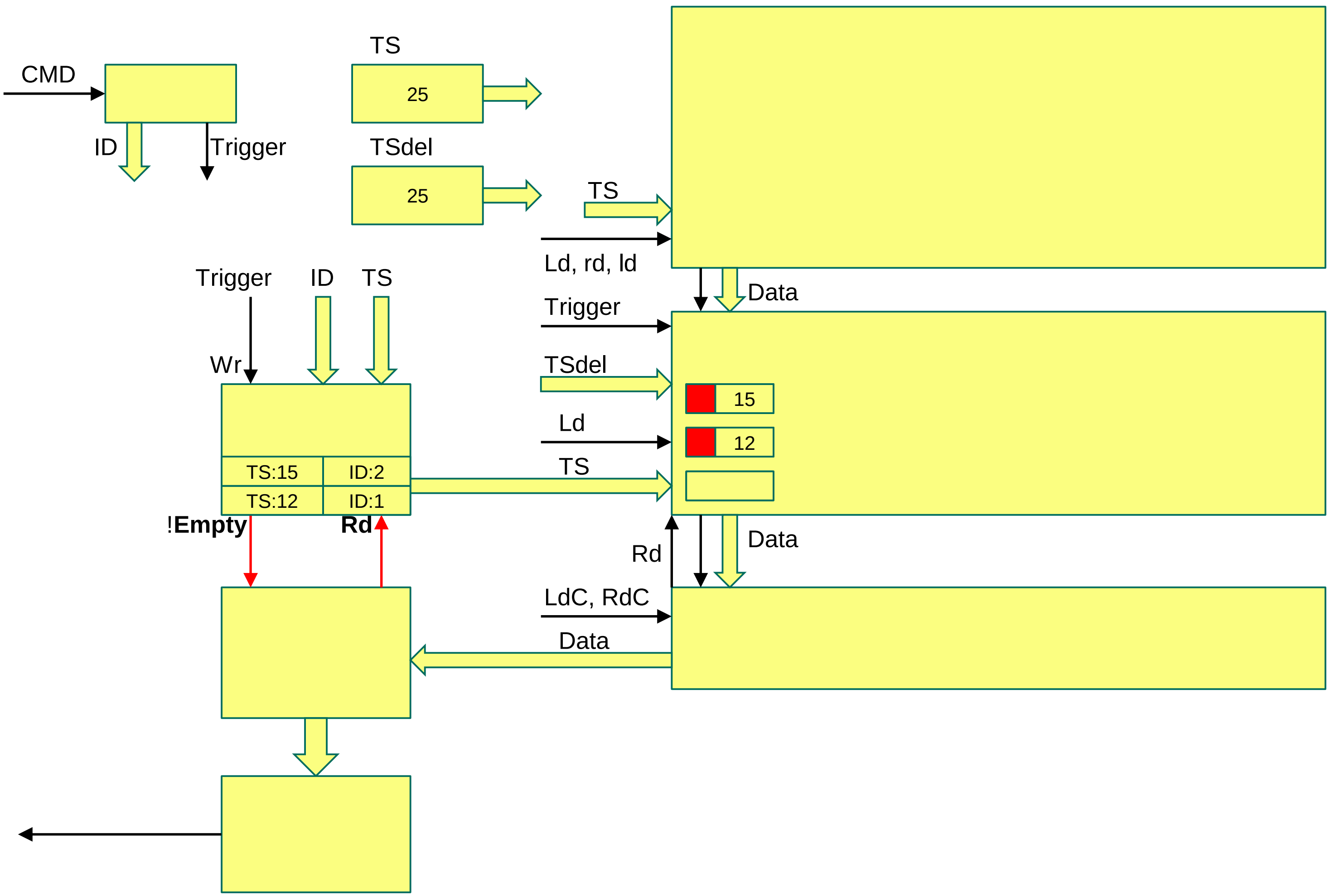
System



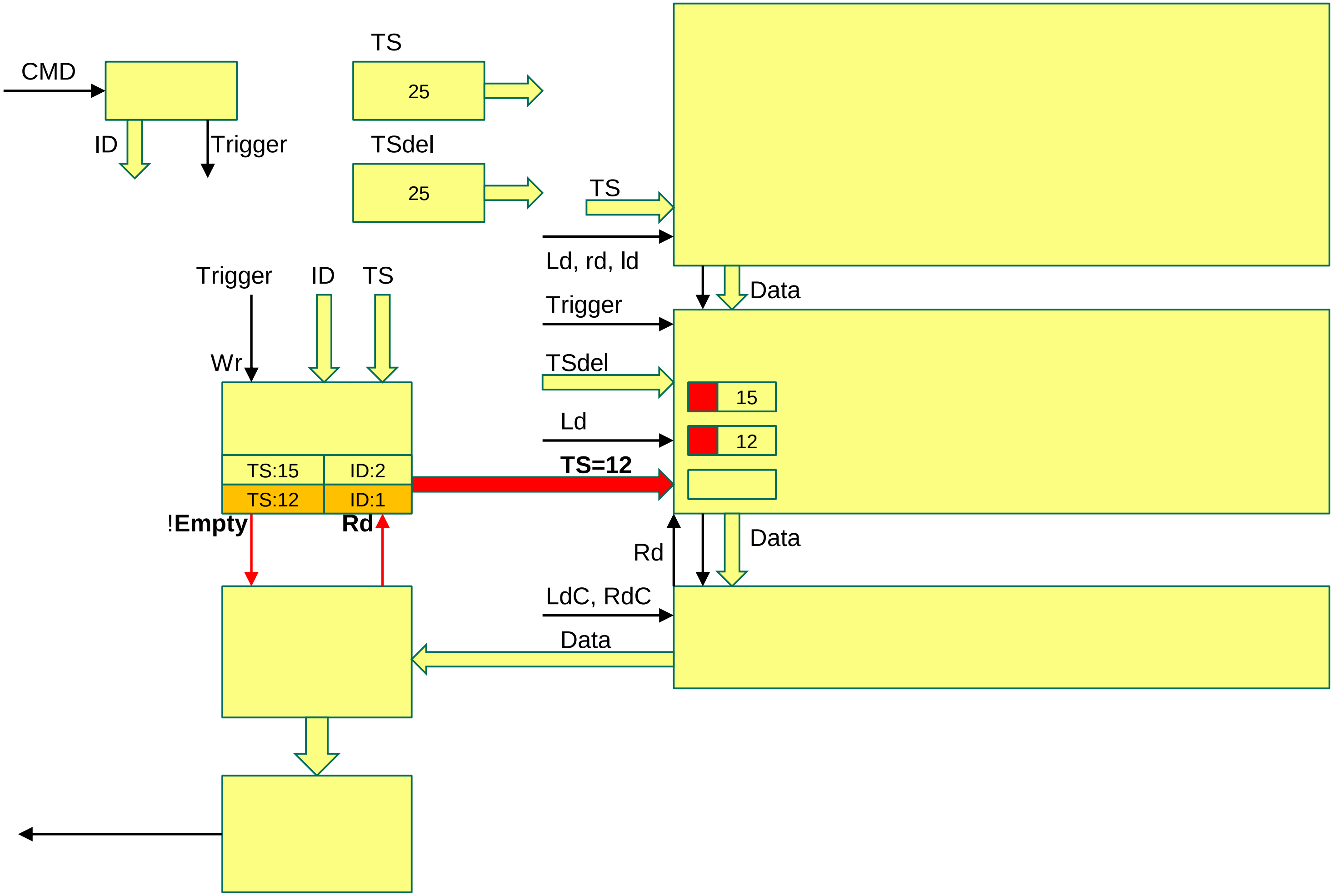
CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Data
Trigger
TSdel
15
12
Ld
TS
Trigger
ID
TS
Wr
TS:15
ID:2
TS:12
ID:1
!Empty
Rd
Rd
Data
LdC, RdC
Data


CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Trigger
ID
TS
Wr
Data
Trigger
TSdel
15
Ld
12
TS
TS:15
ID:2
TS:12
ID:1
!Empty
Rd
Rd
Data
LdC, RdC
Data

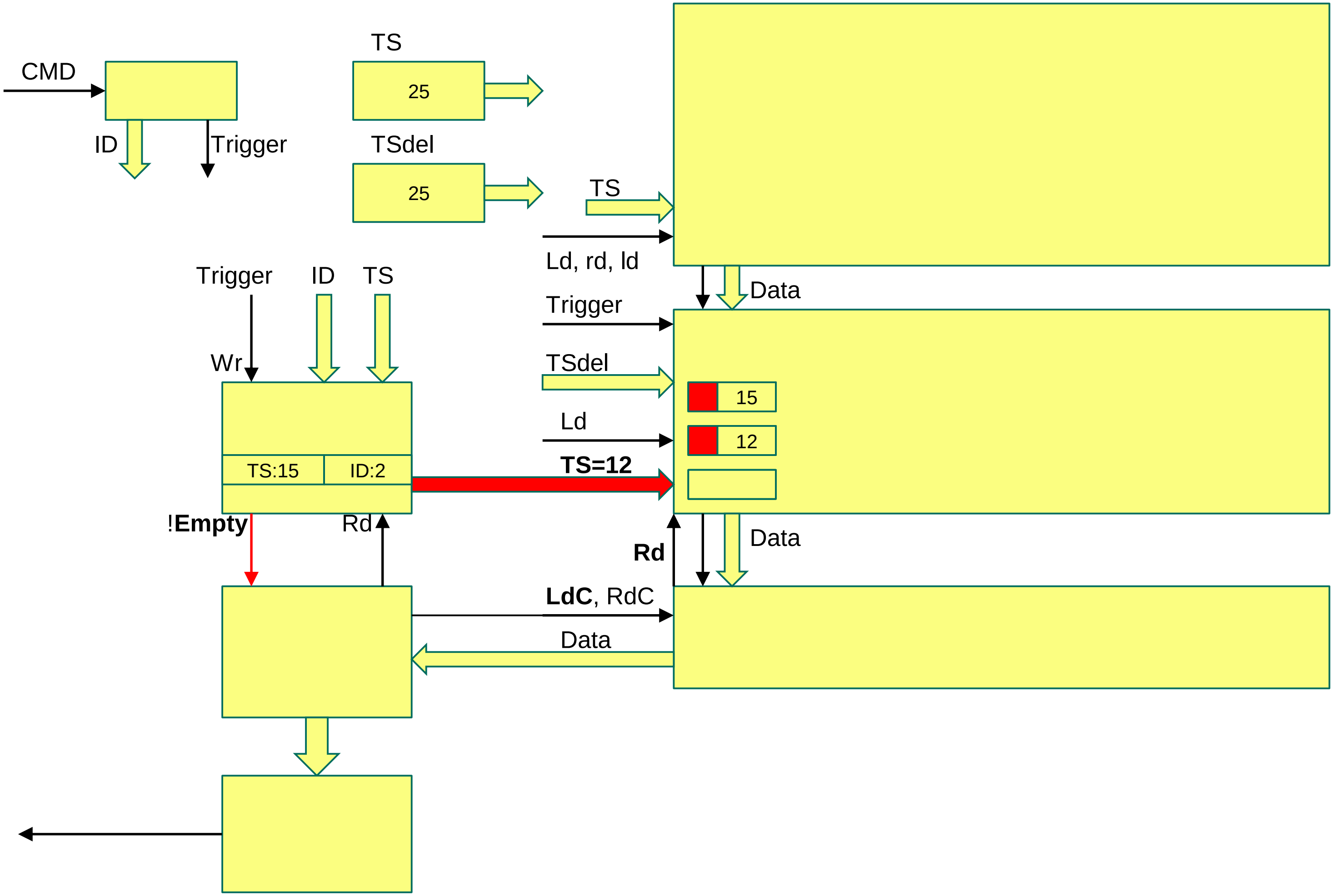
System


CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Data
Trigger
ID
TS
Trigger
Wr
TSdel
15
Ld
12
TS
TS:15
ID:2
TS:12
ID:1
!Empty
Rd
Data
Rd
LdC, RdC
Data

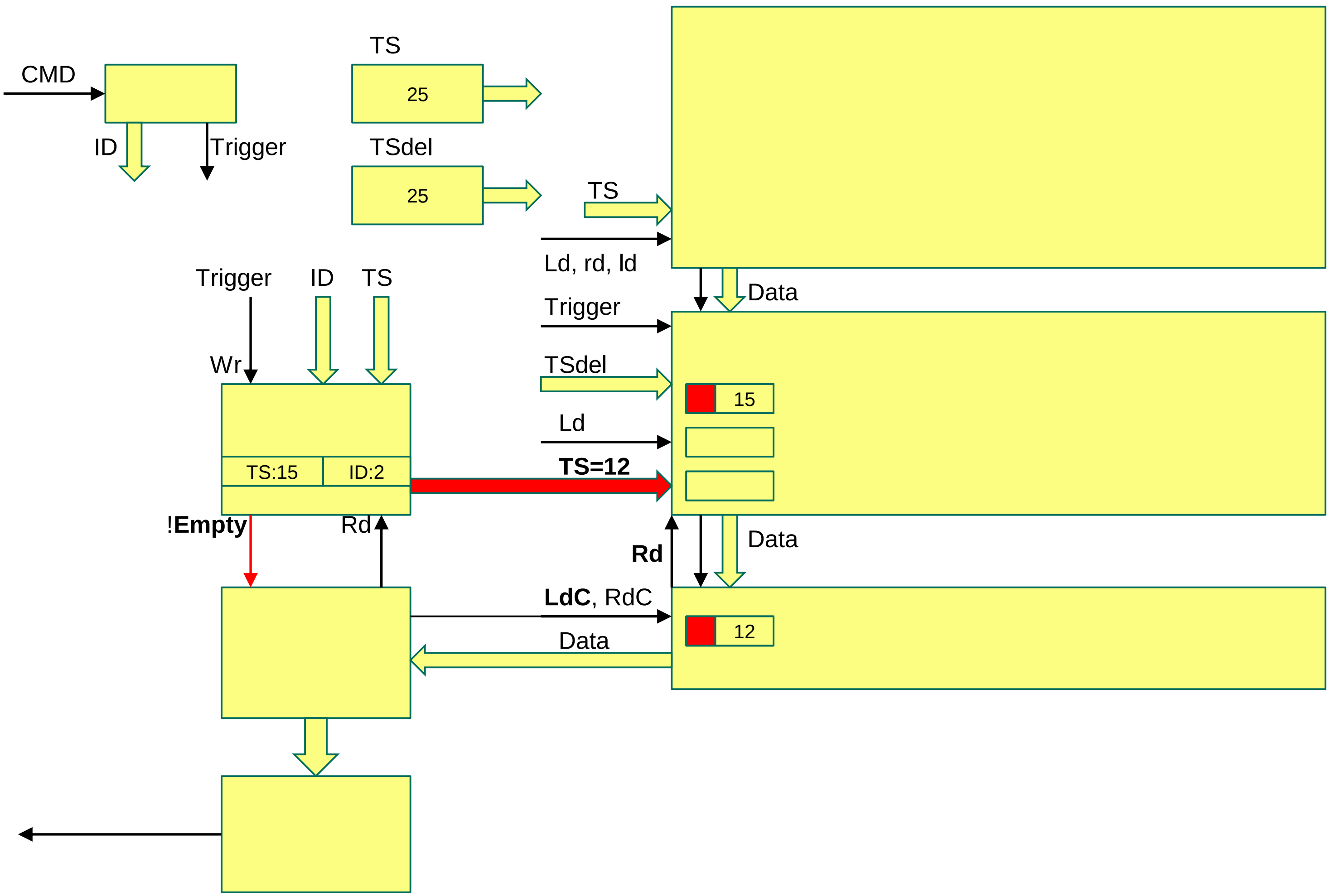
System

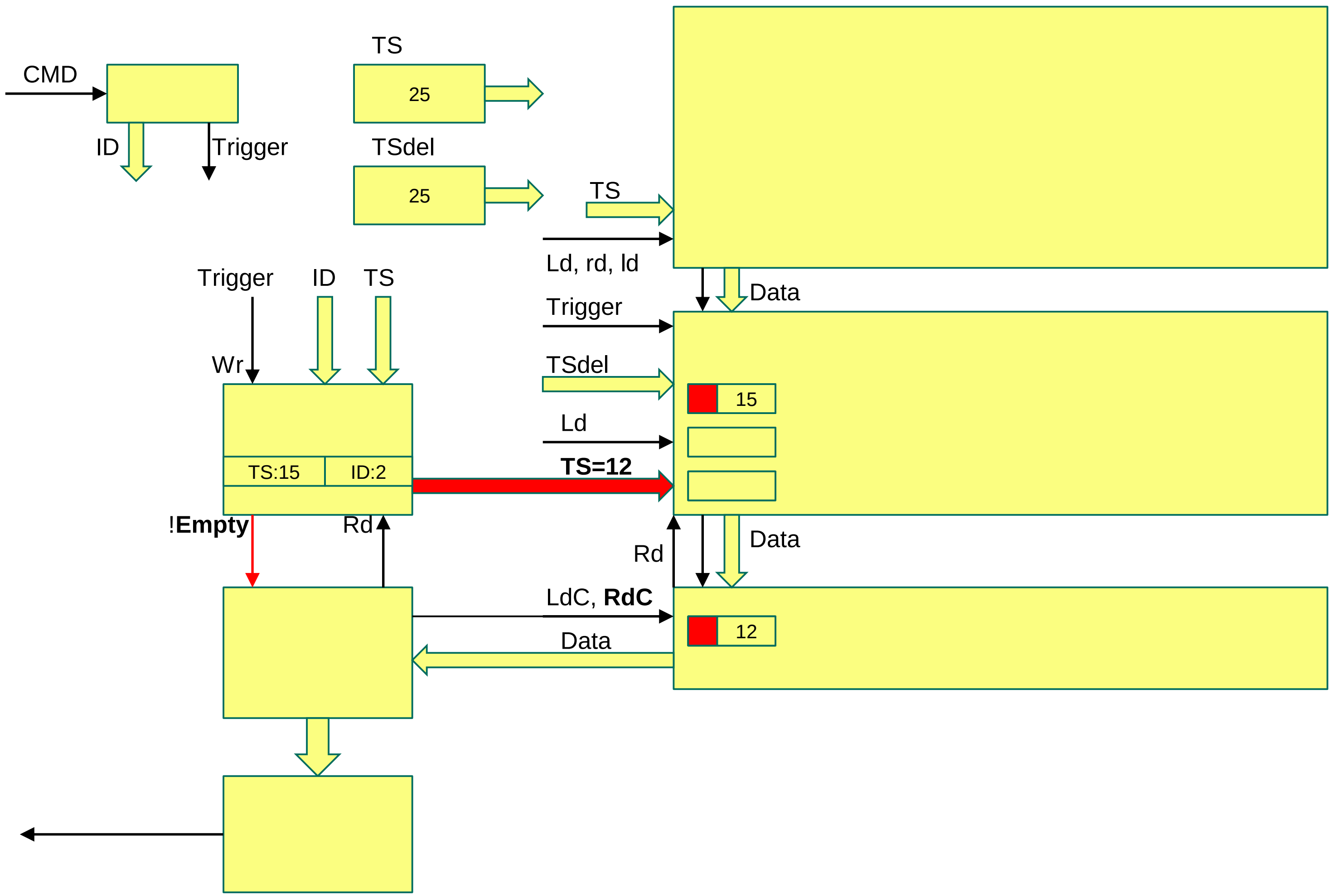

CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Data
Trigger
TSdel
15
Ld
12
TS=12
Trigger
ID
TS
Wr
TS:15
ID:2
TS:12
ID:1
!Empty
Rd
Rd
Data
LdC, RdC
Data

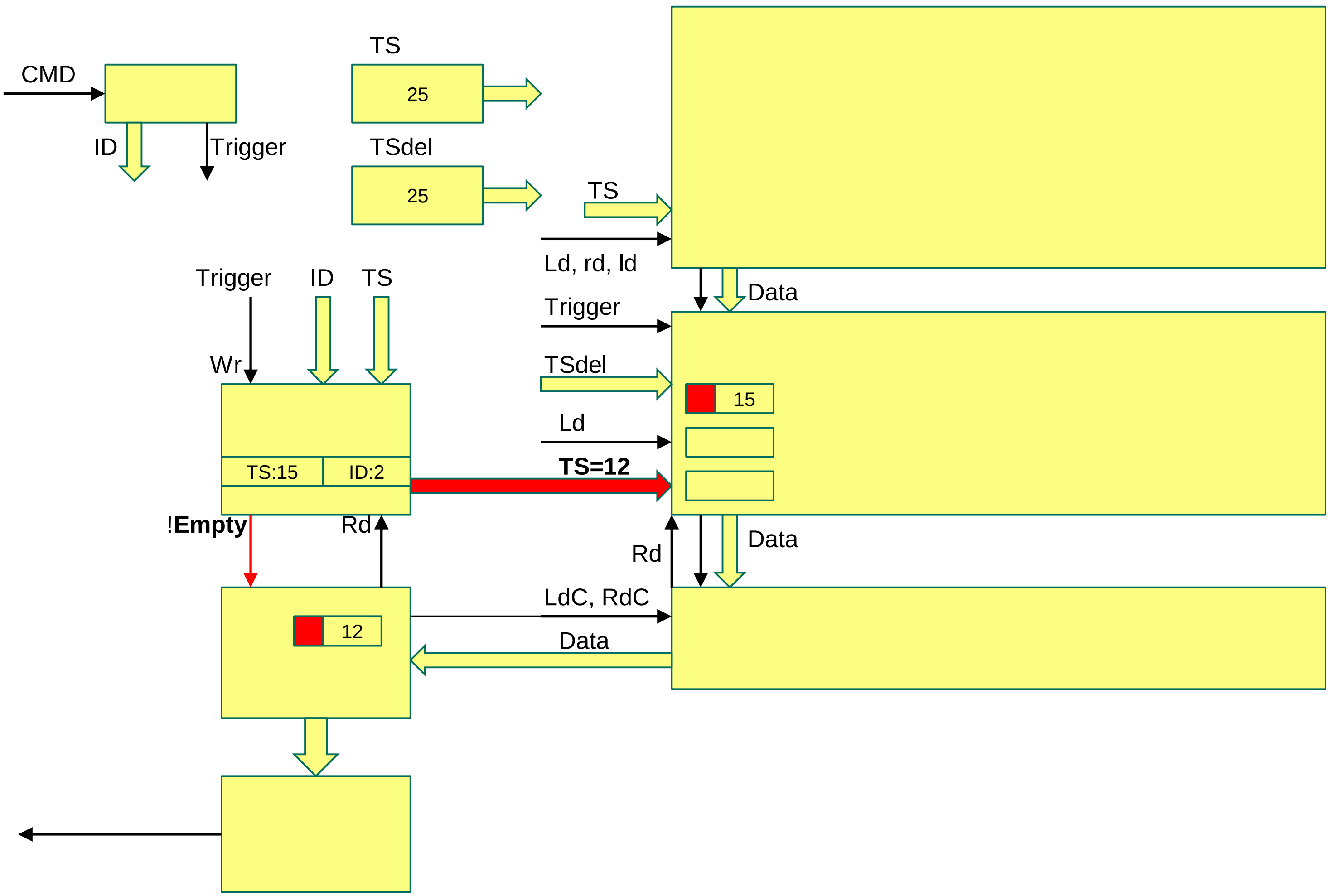
System

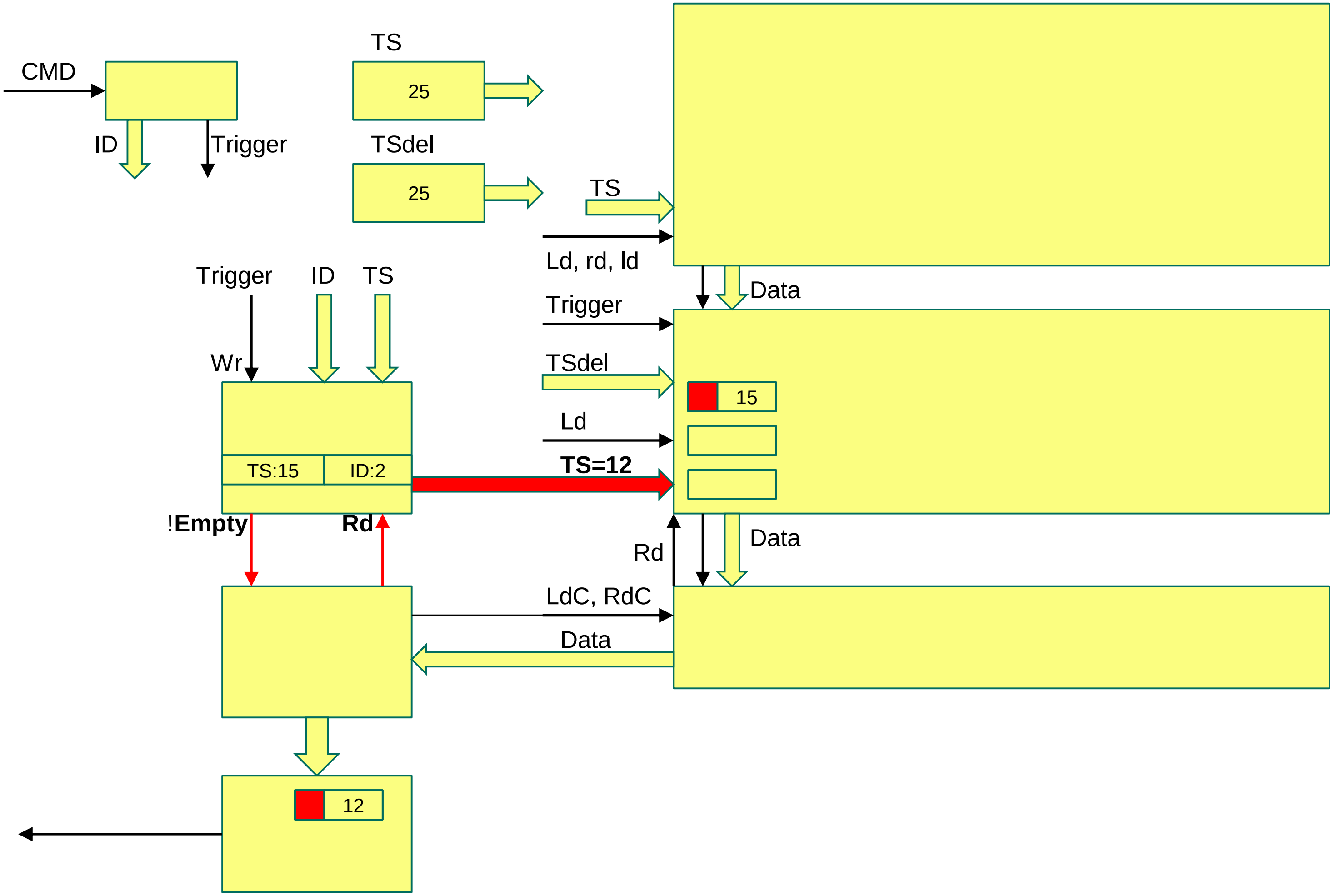


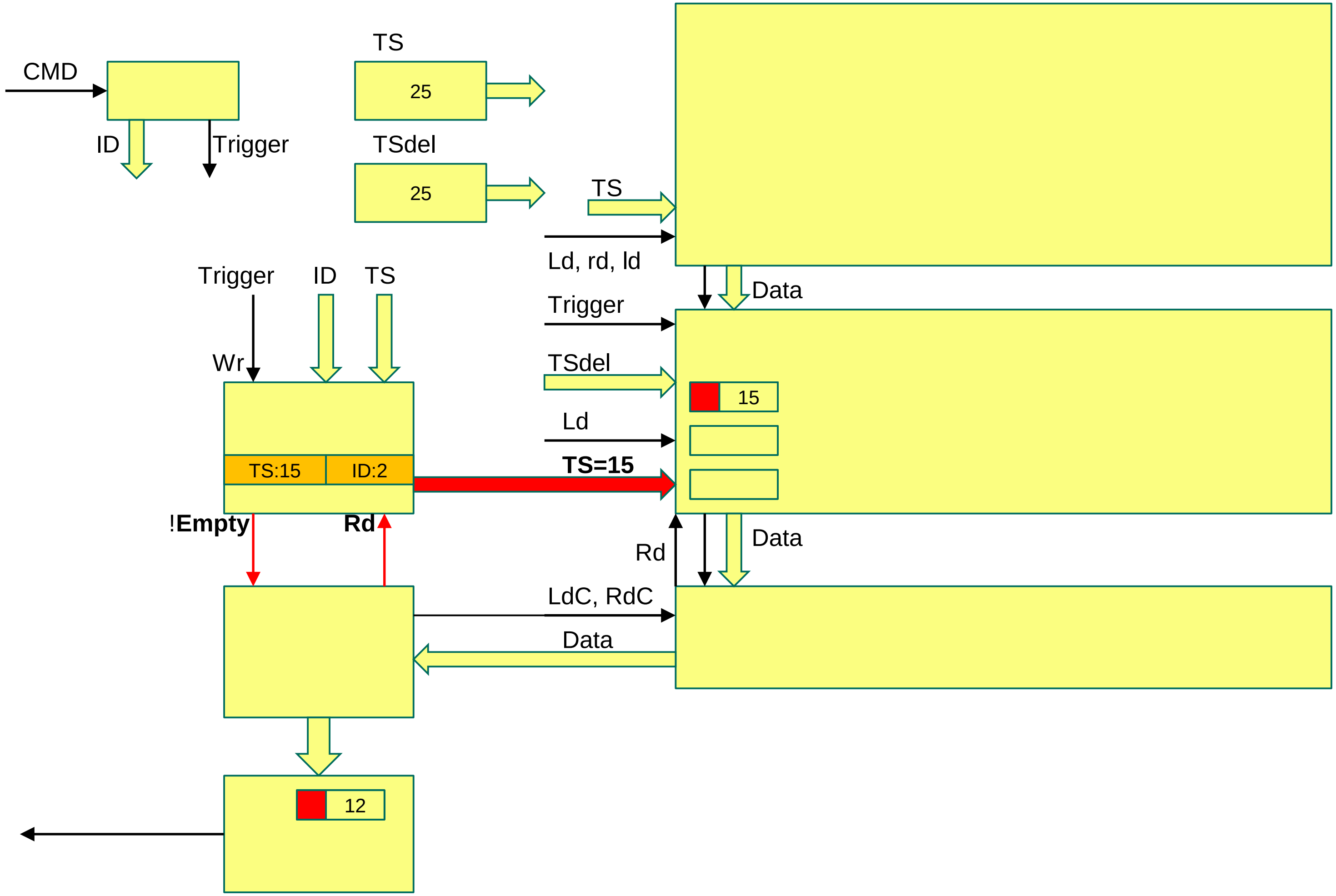
CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Data
Trigger
ID
TS
Trigger
Wr
TSdel
15
Ld
12
TS:15
ID:2
TS=12
!Empty
Rd
Rd
Data
LdC, RdC
Data

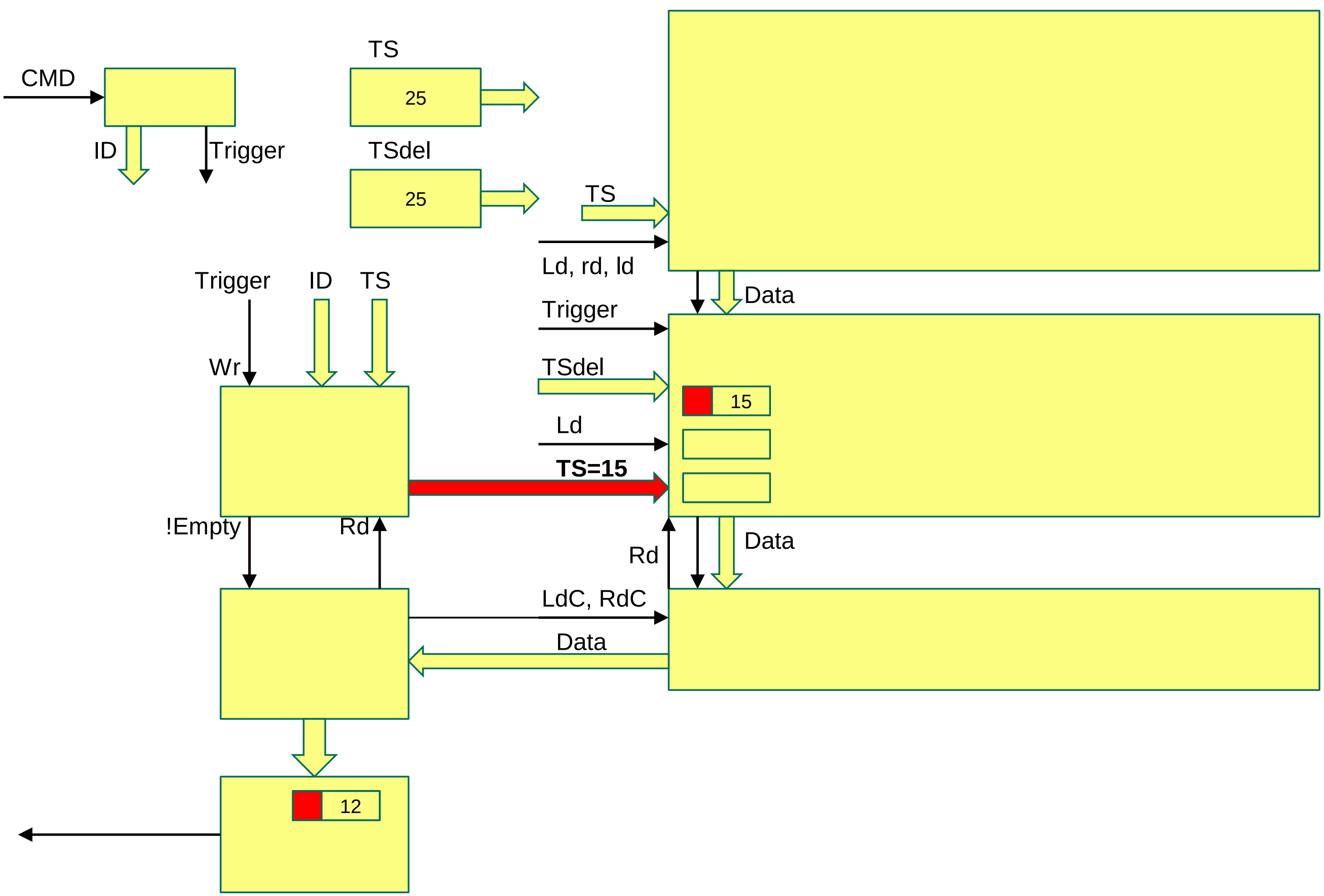

CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Data
Trigger
TSdel
15
Ld
TS=12
Trigger
ID
TS
Wr
TS:15
ID:2
!Empty
Rd
Rd
Data
LdC, RdC
Data
12

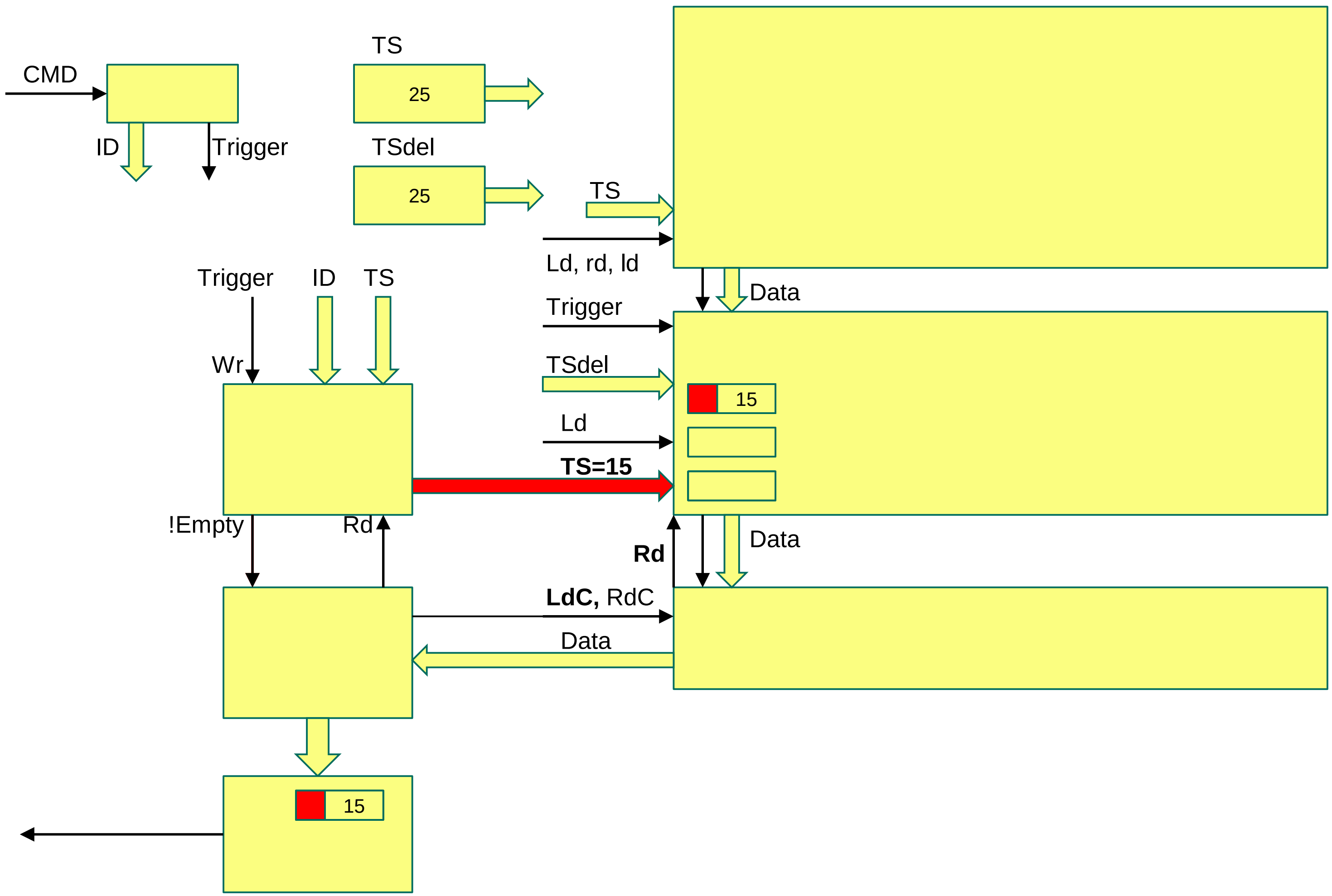

CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Data
Trigger
TSdel
15
Ld
TS=12
Trigger
ID
TS
Wr
TS:15
ID:2
!Empty
Rd
Rd
Data
LdC, RdC
Data
12


CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Trigger
ID
TS
Data
Trigger
Wr
TSdel
15
Ld
TS:15
ID:2
TS=12
!Empty
Rd
Rd
Data
LdC, RdC
12
Data

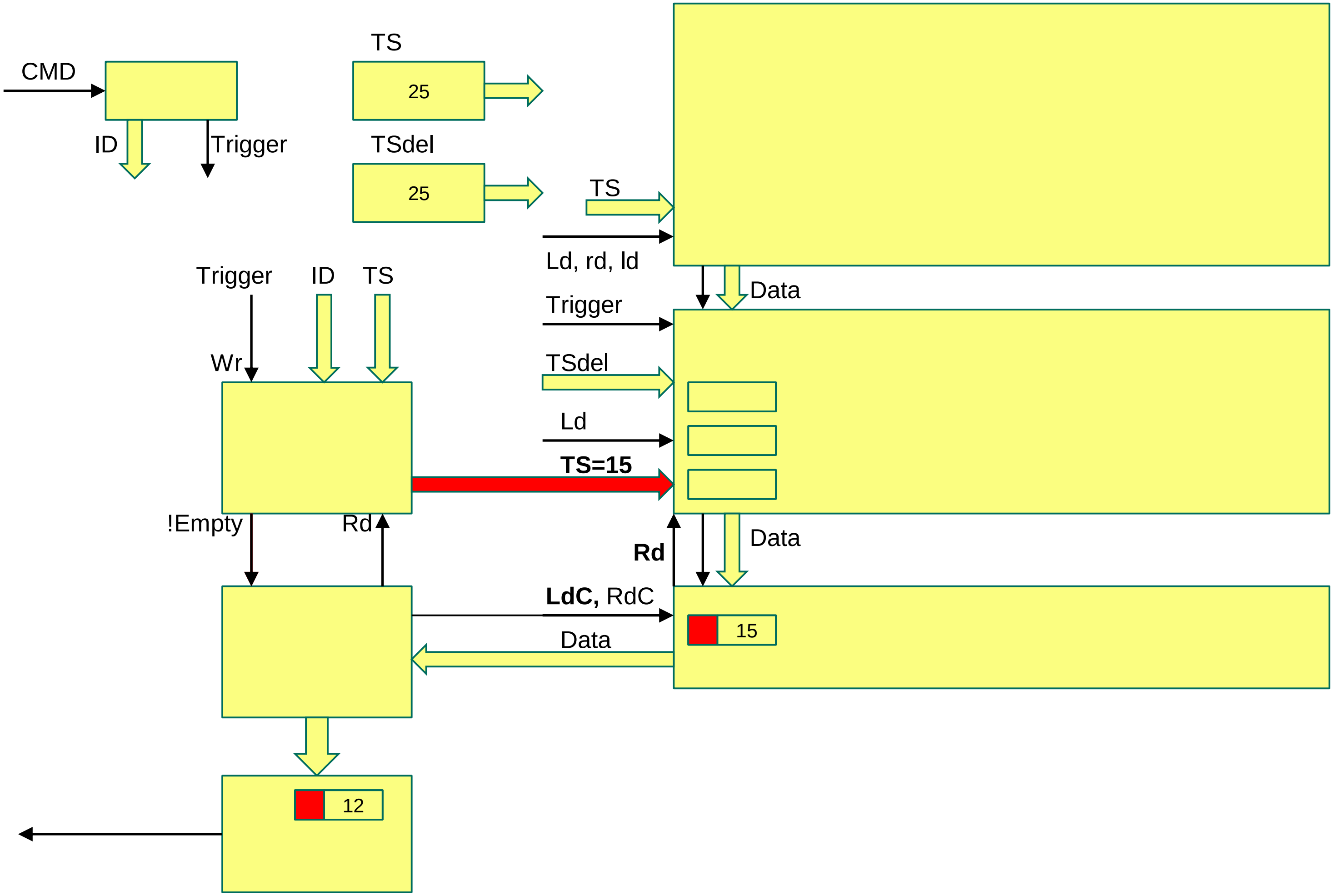

CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Data
Trigger
TSdel
15
Ld
TS=12
Trigger
ID
TS
Wr
TS:15
ID:2
!Empty
Rd
Rd
Data
LdC, RdC
Data
12


CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Data
Trigger
TSdel
15
Ld
TS=15
Trigger
ID
TS
Wr
TS:15
ID:2
!Empty
Rd
Rd
Data
LdC, RdC
Data
12

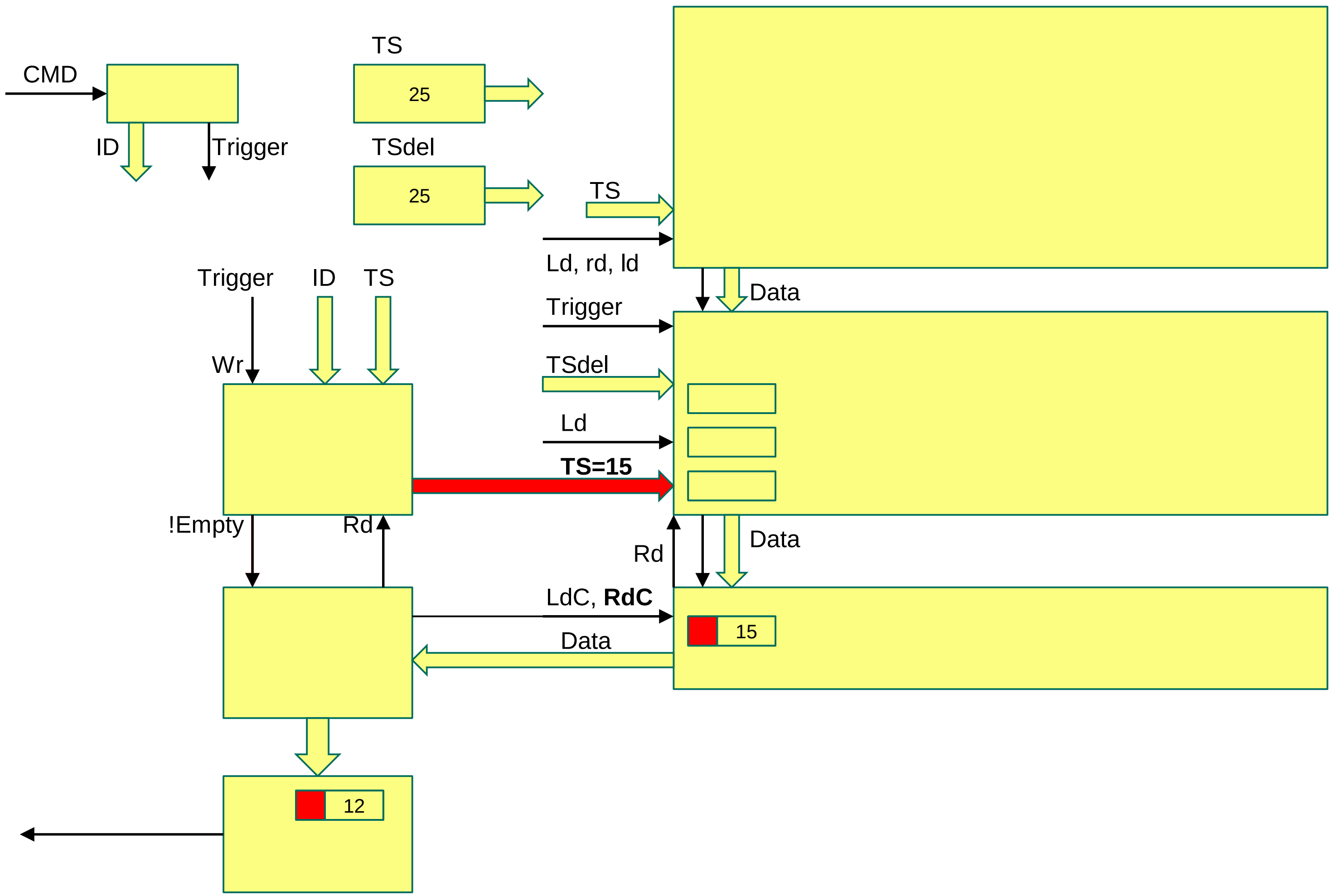

CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Data
Trigger
TSdel
15
Ld
TS=15
Trigger
ID
TS
Wr
!Empty
Rd
Rd
Data
LdC, RdC
Data
12

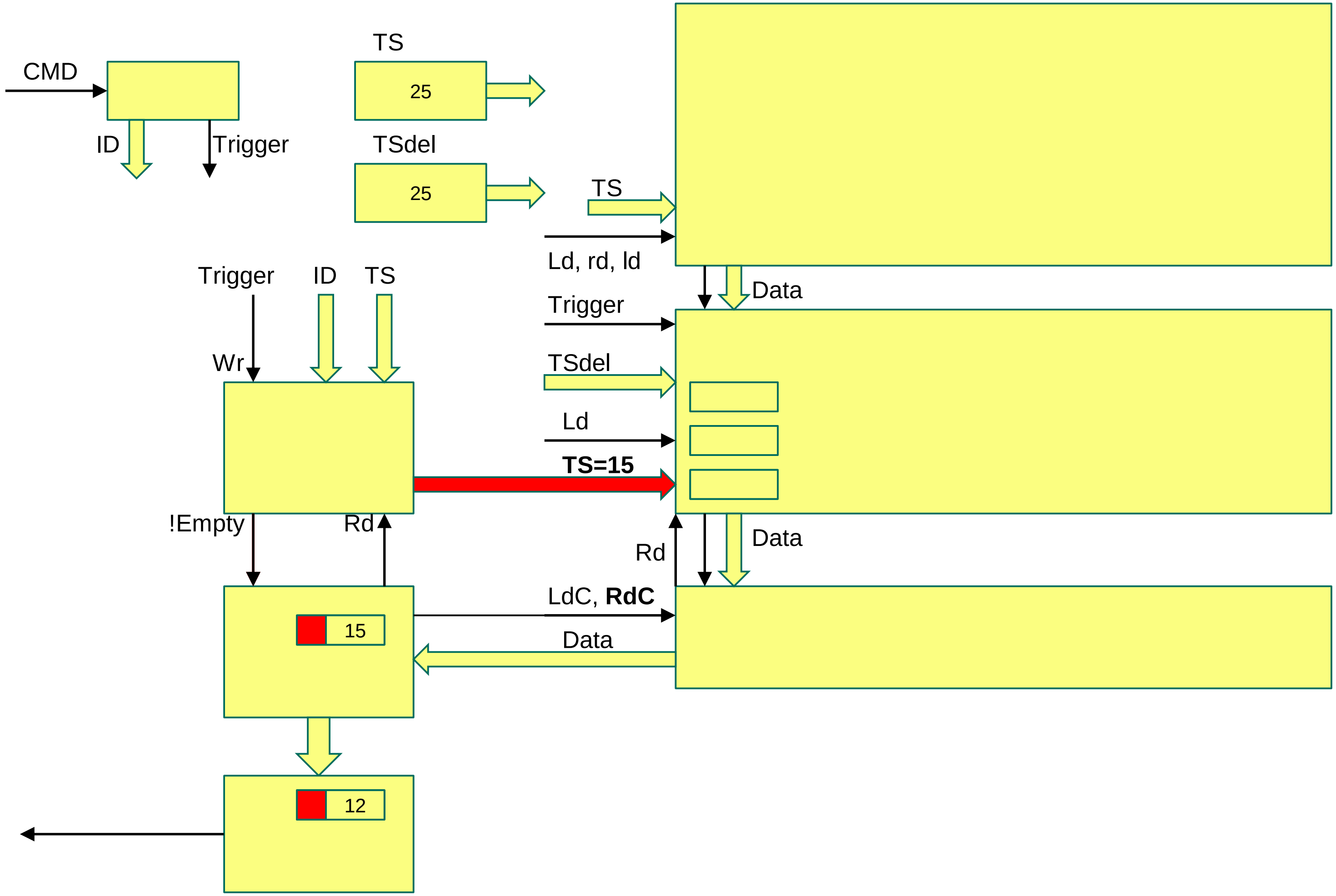

CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Trigger
ID
TS
Wr
Data
Trigger
TSdel
15
Ld
TS=15
!Empty
Rd
Rd
Data
LdC, RdC
Data
15

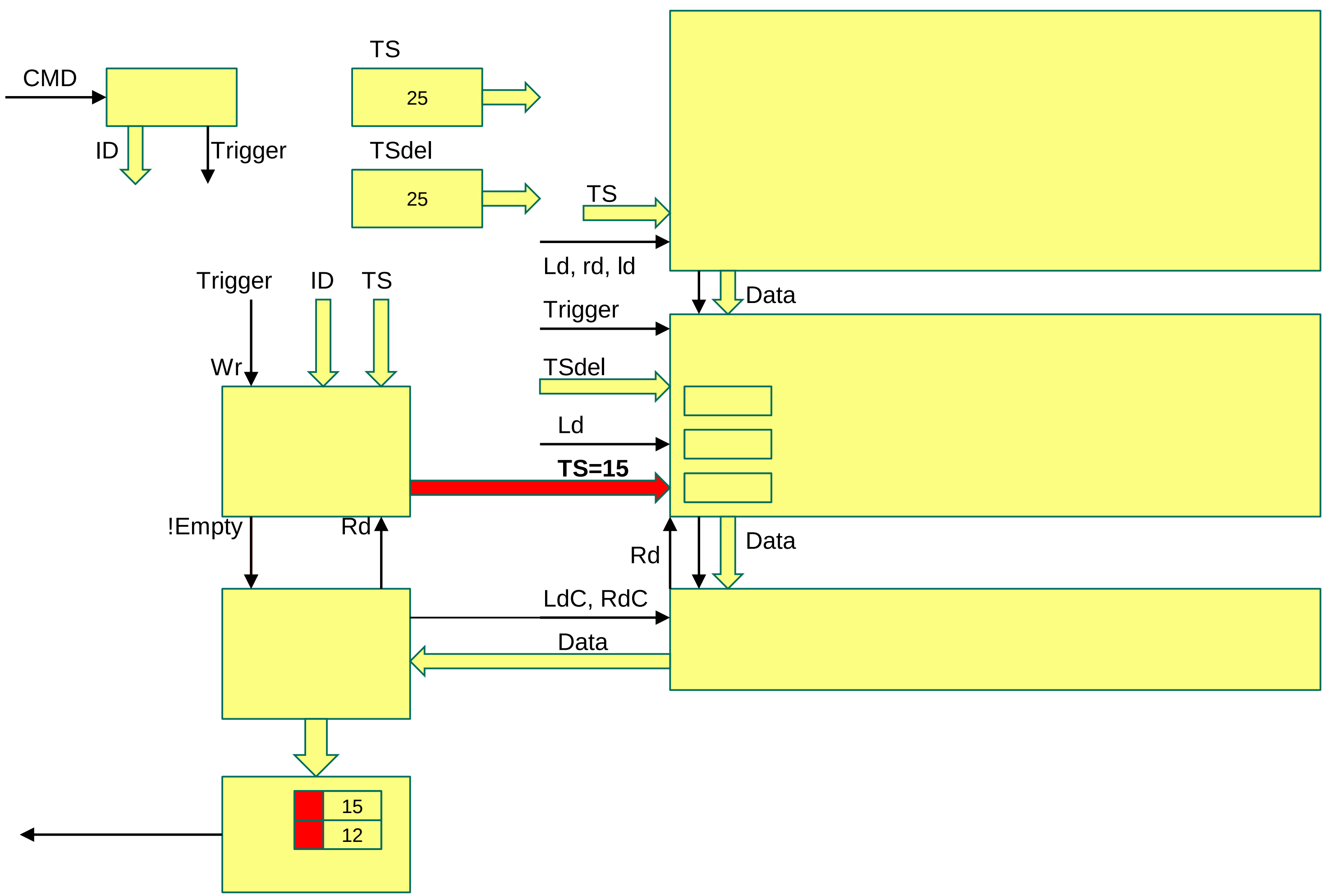
System

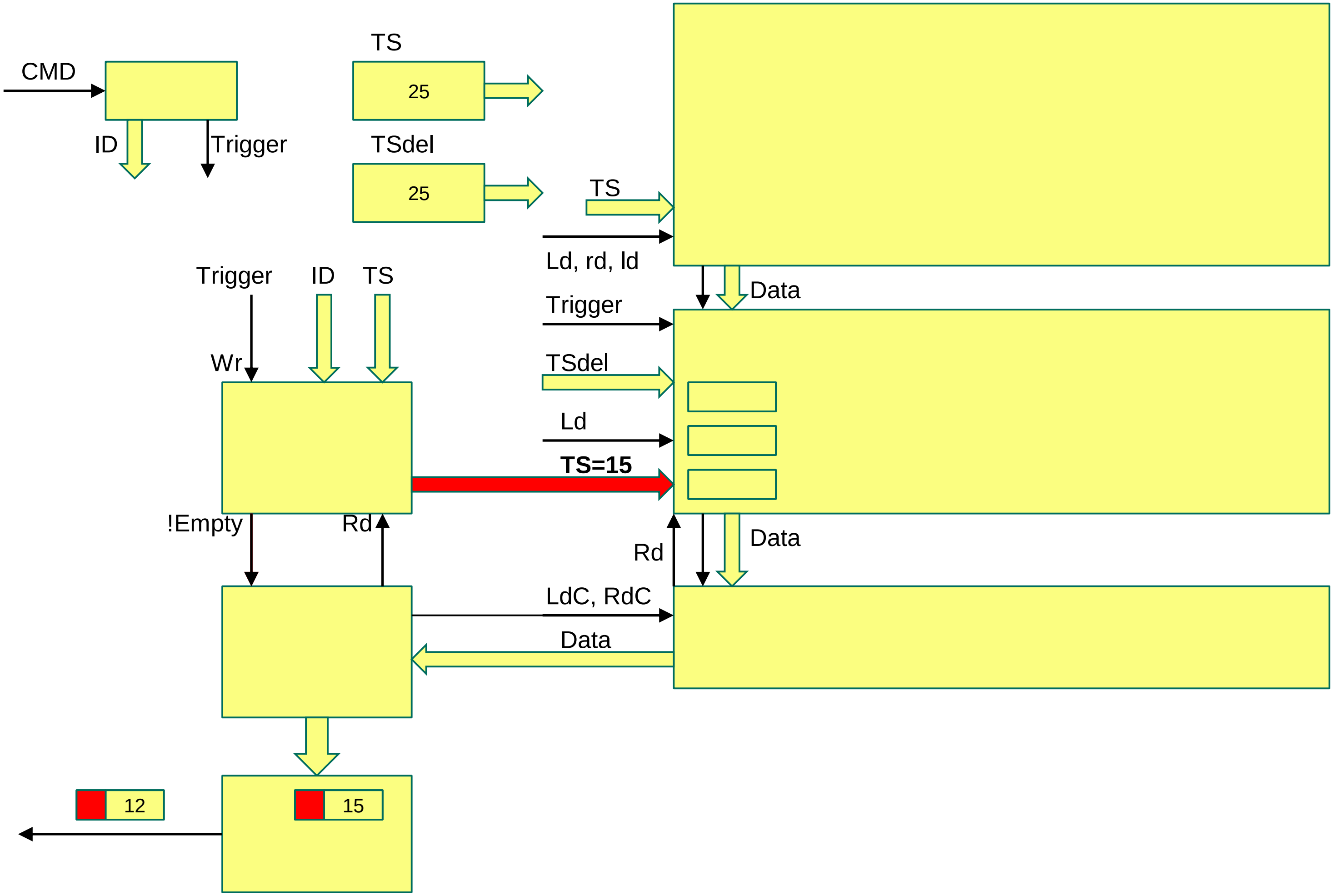

CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Trigger
ID
TS
Data
Trigger
Wr
TSdel
Ld
TS=15
!Empty
Rd
Rd
Data
LdC, RdC
15
Data
12

System

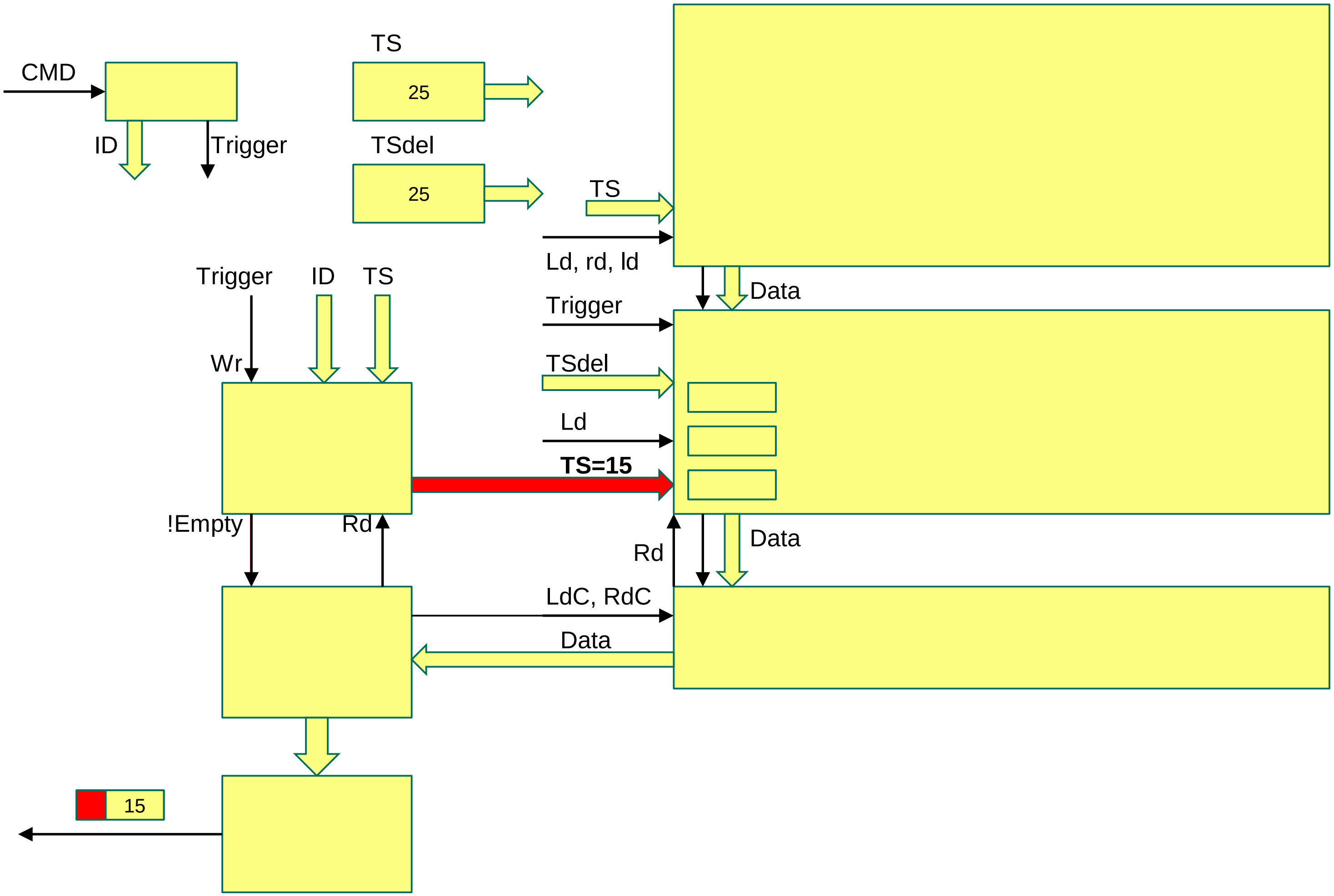

CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Data
Trigger
ID
TS
Trigger
Wr
TSdel
Ld
TS=15
!Empty
Rd
Rd
Data
LdC, RdC
Data
15
12


CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Trigger
ID
TS
Wr
Data
Trigger
TSdel
Ld
TS=15
!Empty
Rd
Rd
Data
LdC, RdC
15
Data
12


CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Trigger
ID
TS
Data
Trigger
Wr
TSdel
Ld
TS=15
!Empty
Rd
Rd
Data
LdC, RdC
Data
15
12

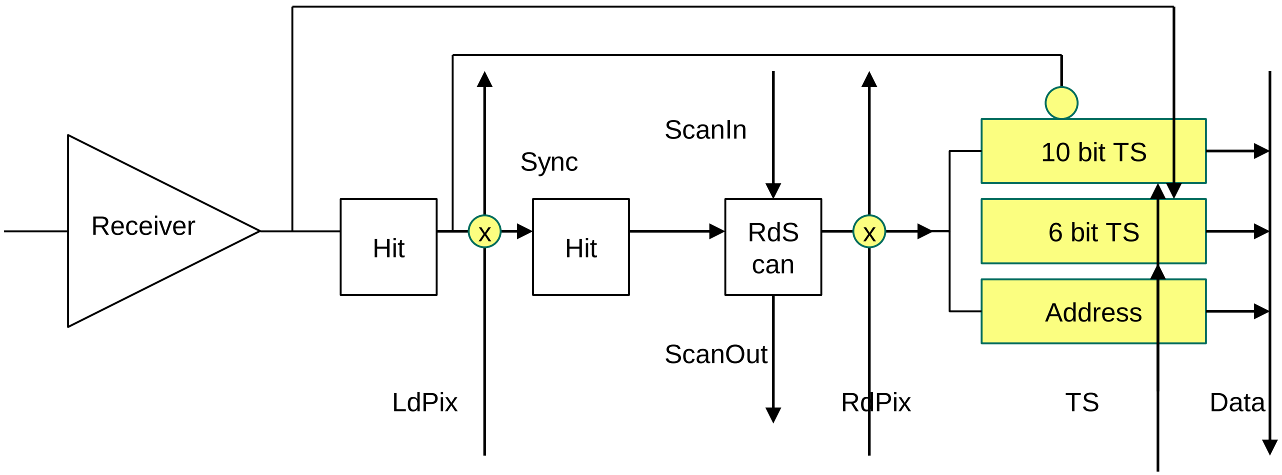


CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Trigger
ID
TS
Data
Trigger
Wr
TSdel
Ld
TS=15
!Empty
Rd
Data
Rd
LdC, RdC
Data
12
15



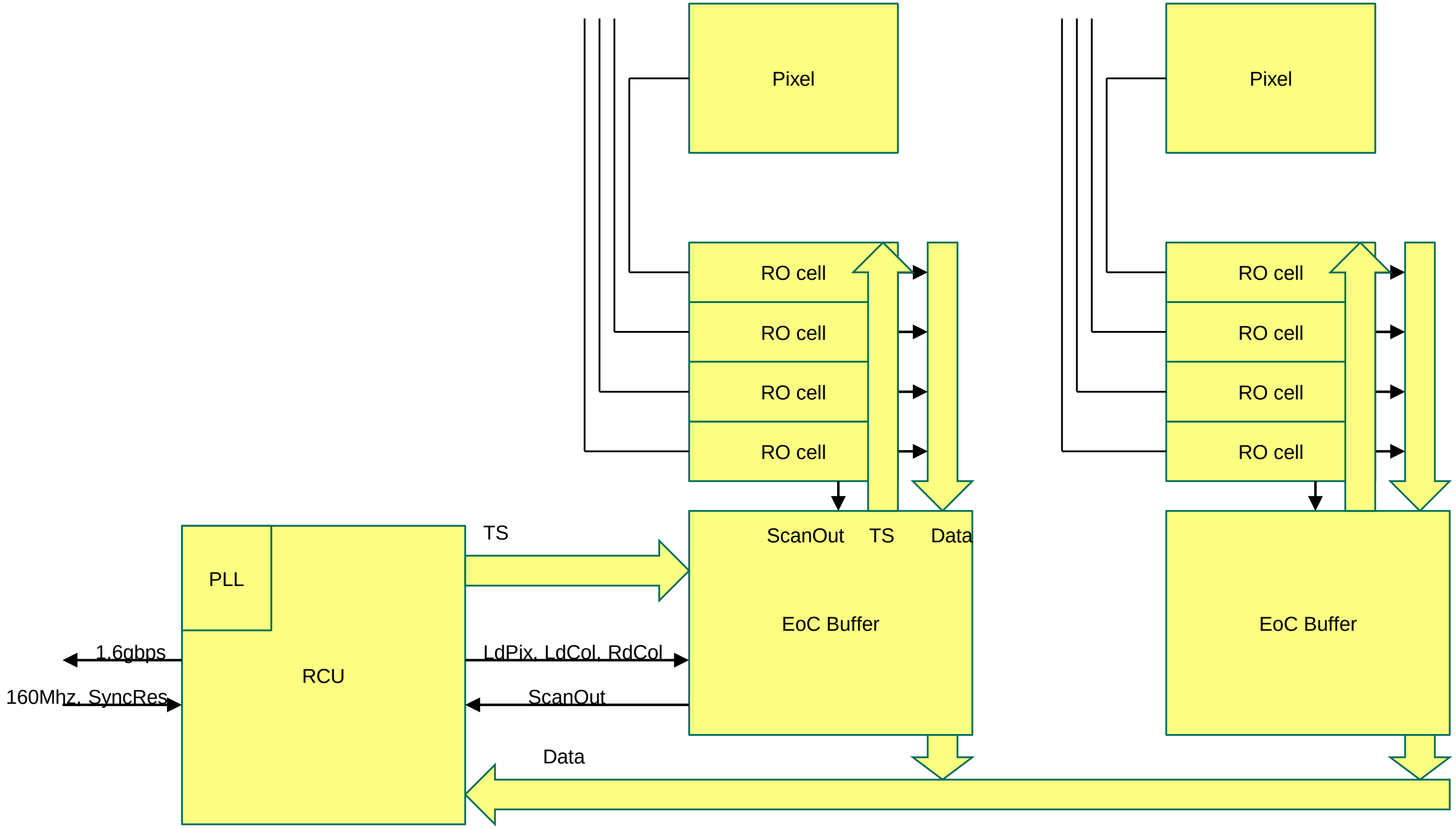
CMD
ID
Trigger
TS
25
TSdel
25
TS
Ld, rd, ld
Data
Trigger
ID
TS
Trigger
Wr
TSdel
Ld
TS=15
!Empty
Rd
Rd
Data
LdC, RdC
Data
15

- The readout circuit, that follows the comparator, resembles the one in FEI3.
- It is based on time stamps that are generated in the readout control unit RCU (pixel digital part) and distributed.
- When there is a comparator signals the leading edge time stamp is stored. Additionally the time over threshold is measured.
- Hit flags are set to 1.
- There is a priority based scan that selects the top most RO cell with active hit flag
- The data from this cell are transmitted to the eoc buffers and finally to the DCU



Chip architecture

- There is a priority based scan that selects the top most RO cell with active hit flag
- The data from this cell are transmitted to the EoC buffers and finally to the RCU



- RCU is the syntesized digital part.
- It controls readout (state machines), generates time stamps and does data processing, formatting (8b10b conversion) and serializing. The data are transmitted via up to 3 digital links at 1.6Gbitps.