Timing Vertex Detector (TVD) concept and Si Tracker ASIC in 130nm

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Introductory comments

• Am actually covering 2 different aspects
  – An ASIC for silicon strip upgrade
  – Thoughts on incorporating precision timing, with an extreme example given

• Improvements to Si strip tracker
  – LGAD (not necessarily timing, reduced thickness)
  – ASIC with smaller noise slope (outside acceptance)

• Benefits of precision timing
  – Reduced occupancy (robustness)
  – Reduced data to disk (storage cost)
  – Exchange a spatial dimension for time (chan cnt)

• Readiness: today versus tomorrow
APV25 replacement

- Short shaping time while keeping SNR comparable for increased input capacitance (well posed problem)
- Switch to 130nm node (from 250nm)
- Deeper analog pipeline (≈5us very marginal for trigger formation) at increased sampling rate
- (option) On-chip A->D conversion, feature extraction

GRAPH ASIC as CSA reference; SCAs for Belle II as analog pipeline
A similar application (JINST_002P_0416 v2)

- Total C depends on length
  - Order 5 – 20pF
- MHz single p.e. rates for next generation UV imaging space mission
- Low power, high hit-throughput
- Fit charge cloud distribution to extract um resolution
CSA for high rates

• Reduce shaping time
  – Reduce impact of pile-up
  – Combined with higher sampling rate to reduce out-of-time hits, template fit to improve SNR
  – Necessary to maintain SNR

• Optimize for detector config (and possible AD gain)
Combining with analog pipeline

- Baseline CSA almost on 50um pitch
- Zero-suppression and feature extraction
Interest in exquisite space-time Resolution

In a number of communities (future particle/astroparticle detectors, PET medical imaging, etc.) a growing interest in detectors capable of operating at the pico-second resolution and μm spatial resolution limit (for light 1 ps = 300 μm)

Extending to 1ps and lower, with advanced calibration techniques

Prediction: circa 2009

Measurement: circa 2014

Front-End Electronics

Fast signal collection x-ray detectors
A very different kind of Calorimeter

Askaryan Calorimeter Exp (ACE)

Radio (mm wave)

arXiv:1708:01798

2.3ps intrinsic timing resolution
(SLAC ESTB measurement)
AARDVARC $\Rightarrow \mu s$

sampling latency
Analog BW limitation – identify and improve

- BWworst≈2.3GHz @665mVdc @LowZ drive
- BWworst≈1.7GHz @665mVdc @50Ω drive

- Isolation is over 60dB over all parameter space
What would it take?

- Micron spatial pixel resolution (using timing)
  ➔ Fast timing brings many benefits:
    ➢ Minimal pile-up (fast clearing)
    ➢ Improved event timing (direct T0 for TOF/TOP measurements)
Understanding waveform sampling limits

Detailed simulation model developed to allow exploration of phase space – first need to verify results

Exploration of the space-time limit

- Sampling at high sampling rate and high bandwidth
- Resolve small distances

Current Goals: Spatial resolution of 10μm in z and 20μm in rφ
In Silicon 10μm in z corresponds to timing resolution of about 100fs
20μm in rφ will depend on the SNR

Pixel detector (PDX) at SuperKEKB
Signal Propagation

![Graph showing signal propagation delay and speed versus substrate relative permittivity.](image-url)
Pushing to the femtosecond regime

And pushing the space-time limit
(new type of PID or DIRC devices?)

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Performance Parameter Space

- **BW = 3GHz**
- **f_s = 20GHz**
- **N = 0.5 mV_{RMS}**
Timing Vertex Detector

• **Moves to the femtosecond regime**
• **Allows one to exchange time for one of the spatial dimensions**
• **Idea is not to improve vs. DEPFET, but significantly reduce the data size/event**
• **Expect many M$/億円 savings on disk storage alone, more at higher Luminosity**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum desired value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling frequency (ASIC)</td>
<td>20 GHz</td>
</tr>
<tr>
<td>Bandwidth (Detector and ASIC)</td>
<td>3 GHz</td>
</tr>
<tr>
<td>Signal to Noise Ratio (Detector and ASIC)</td>
<td>58dB ($V_{signal}=1$ Volt)</td>
</tr>
<tr>
<td>Velocity of Propagation (Transmission Line/ strip line)</td>
<td>0.35c</td>
</tr>
<tr>
<td>Number of Bits of Resolution</td>
<td>9.4 bit</td>
</tr>
</tbody>
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Pushing the **space-time limit**

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Example of a critical component
RFpix1 ASIC Snapshot

Key Design components verified

Work still needed on the digital control/address decoding

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Desired value</th>
<th>Simulated value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling period</td>
<td>50 ps @20 GS/s</td>
<td>50 ps @20 GS/s</td>
</tr>
<tr>
<td>Analog bandwidth a</td>
<td>≈ 3 GHz</td>
<td>≈ 3.56 GHz</td>
</tr>
<tr>
<td>Input referred noise b</td>
<td>≤ 0.5 mV_{RMS}</td>
<td>≈ 1.05 mV_{RMS}</td>
</tr>
<tr>
<td>Added jitter per channel</td>
<td>≈ 40 fs</td>
<td>≈ 29 fs</td>
</tr>
<tr>
<td>ENOB c</td>
<td>≥ 10</td>
<td>≈ 9.6</td>
</tr>
<tr>
<td>Power consumption per channel b</td>
<td>40 mA</td>
<td>41.71 mA</td>
</tr>
</tbody>
</table>

a The simulated value is the tracking bandwidth of the SCA.
b The simulated value does not take into account the input buffer.
c The simulated value does not take into account distortion.
Summary Thoughts

Since we are pondering improvements, should also consider fundamental improvements

- **Si strips – reduced material, occupancy**
  - Improve Signal (intrinsic gain)
  - Reduce/maintain Noise (for larger C)
  - Self-triggering?
  - Data push?

- **Pixel detector – what timing can bring?**
  - Incorporating more precise timing
  - Increase to precision timing (not much gain?)
  - Increase to femtosecond timing (-1D reduction)