Status of LGAD development at BNL (and other silicon R&D activities)

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U.S. DEPARTMENT OF
ENERGY

Outline

- Low Gain Avalanche Diode (LGAD) R&D
  →High Energy Physics and Photon Science
  - fabrication
  - measurements

- HV silicon JFET
  → for multiplexing in ATLAS ITk
  - concept
  - Measurements after irradiation (TRIGA, JSI, Ljubljana, Slovenia)

All silicon process done in BNL Instrumentation Division Class-100 Clean Room

Furnaces for dry oxidations and annealings

Double-sided mask aligner

Wet bench (HF, RCA I & II, piranha, polyetch, …)

Sputtering (Al, Al1%Si, Ti)

RTA for sintering

Laser dicing

+ dry etching and thin-film deposition, but we need to outsource:

- Ion implantation
- Polysilicon deposition

Si-Fab, Si-Lab, and Interconnect Lab.

- **BNL resources used for Silicon R&D**
  - Silicon Fabrication Facility in BNL Instrumentation Div (**Si-Fab**)
  - Capabilities for wire and bump bonding in BNL Instr. Div. (**High Density Interconnect Lab.**)
  - Laboratory to fully characterize, design and simulate silicon sensors and exp. apparatuses (**Si-Lab**)

- **Si-Lab** : probe station, TCT, ambient chamber, rad. sources, instruments, DAQ equipment etc.

- **High Density Interconnect Lab**
  ➔ wire and bump bonding etc.

Interconnect Lab


Bump Deposition


Wire Bonding


Flip-Chip bonder


Micro Dot dispensing

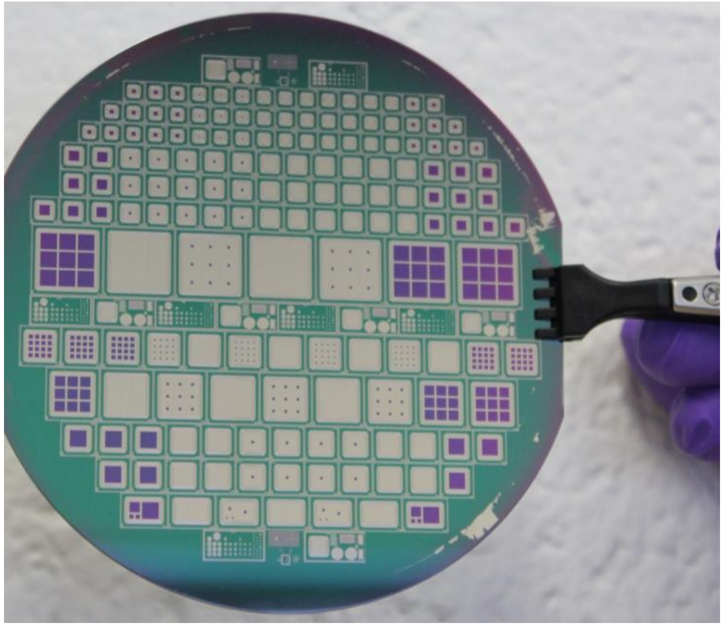

Shear /Pull tester

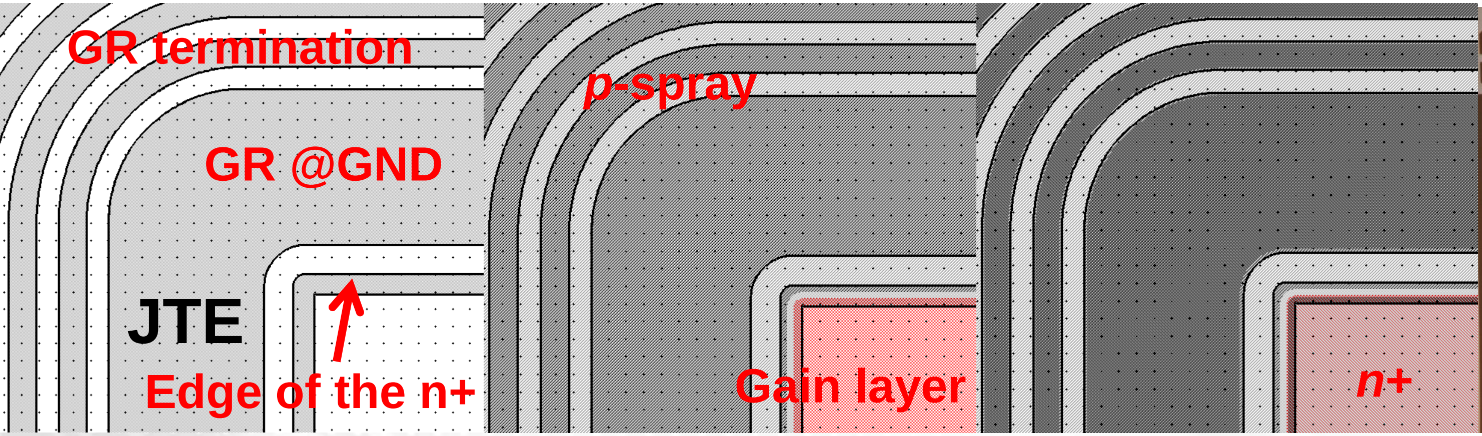

Reflow Oven

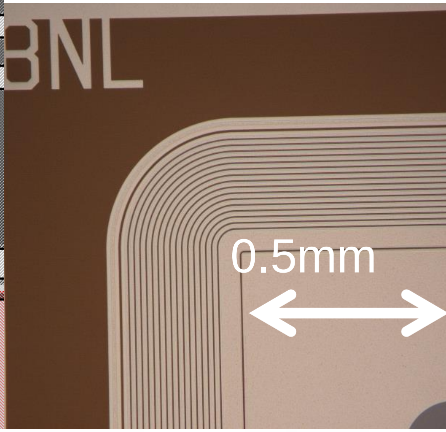
LGAD fabrication at BNL

- 4” *p*-type epitaxial wafers (100), N_A~<1e14cm^{-3}, 50µm thick (→ V_{depl} ~120V). Also FZ used.
- 4 ion implantations (JTE and gain at high energy)
- 6 photolithographic masks
- *p*-spray isolation (patterned externally to the active area to avoid implant on gain region).
- Little thermal drive-in (mainly for the JTE – Junction Termination Edge for protection from high **E** at the border of the shallow n$^+$ implant)

- layout with pads of 1x1 mm^2, 2x2 mm^2, 3x3 mm^2 and arrays.







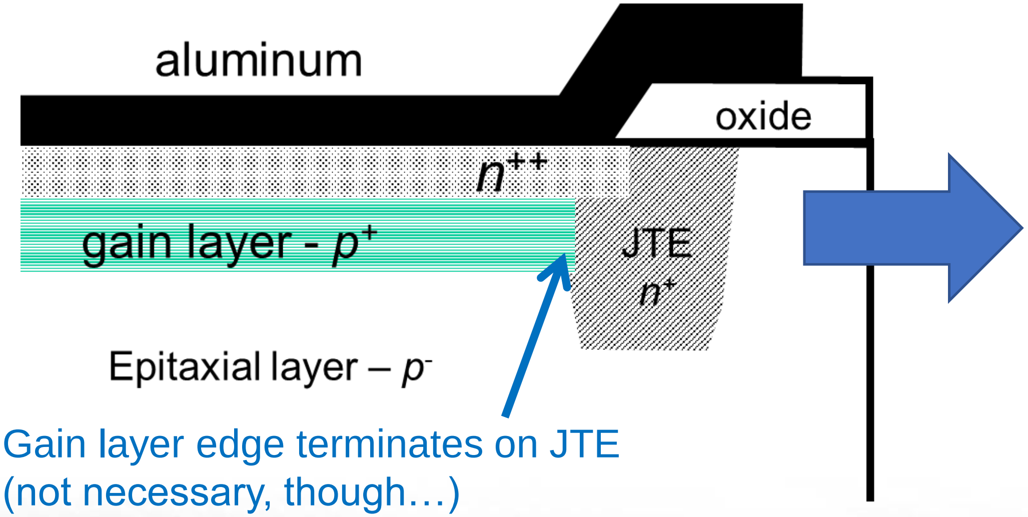
G. Giacomini, et al. “Development of a technology for the fabrication of Low-Gain Avalanche Detectors at BNL”, Nuclear Inst. and Methods in Physics Research, A 934 (2019) 52–57.

LGAD fabrication at BNL

4 ion-implantations (Innovion, San Jose):

- JTE layer as deep as possible (~400keV) → channeling effect on 100 substrates
- *p*-spray (2e12cm^{-2}), external to the active area
- Gain layer as deep as possible, within the JTE
- N+ as shallow as possible

  (to avoid compensation of gain layer)



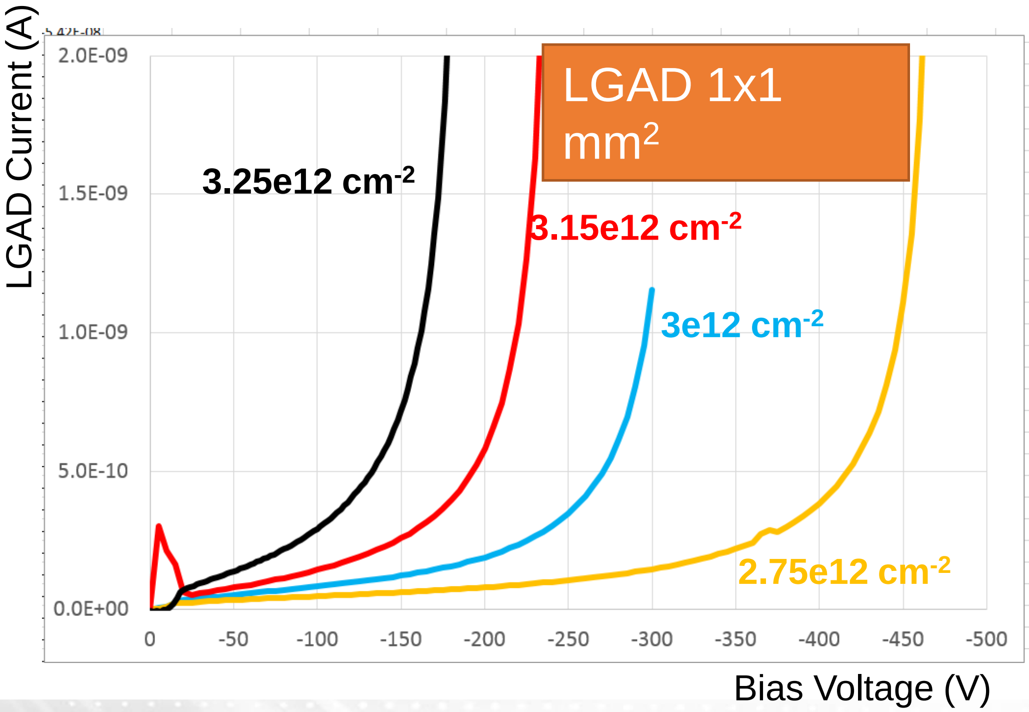
Gain layer edge terminates on JTE
(not necessary, though…)

Multi Guard-Ring Termination
(over dimensioned,
because it must be a general
purpose termination)

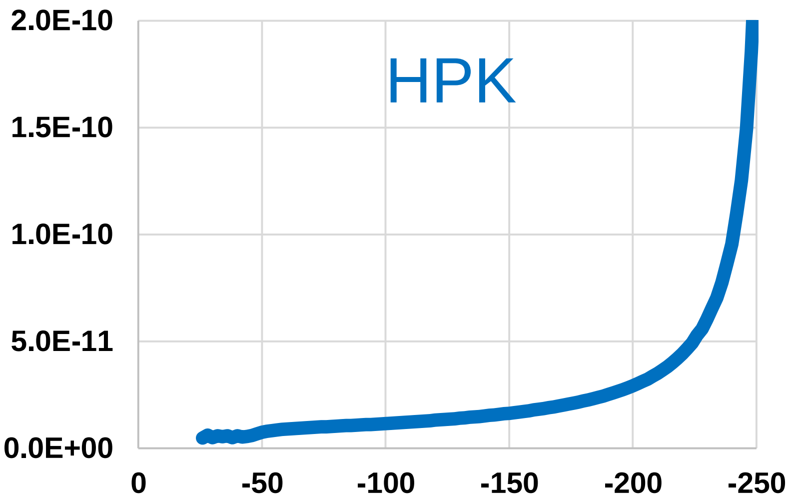
I-V

BNL’s LGADs :

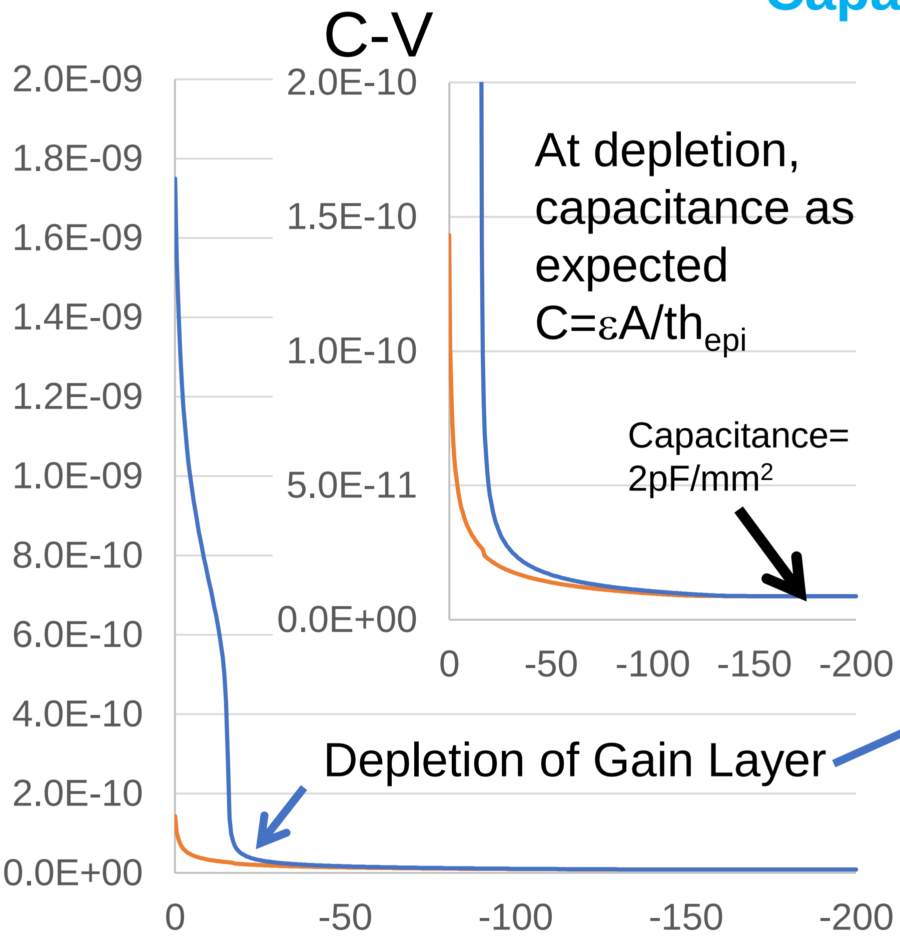
- Leakage current as measured on diodes (gain=1) 1x1 mm^2 is ~ 10pA (1nA/cm^2)
- Consistent from batch to batch
- Clearly current depends on gain layer dose, so does the breakdown voltage
- GR can stand higher voltages



BNL is involved in the testing of HPK and CNM LGAD for the ATLAS Timing Detector (HL-LHC).



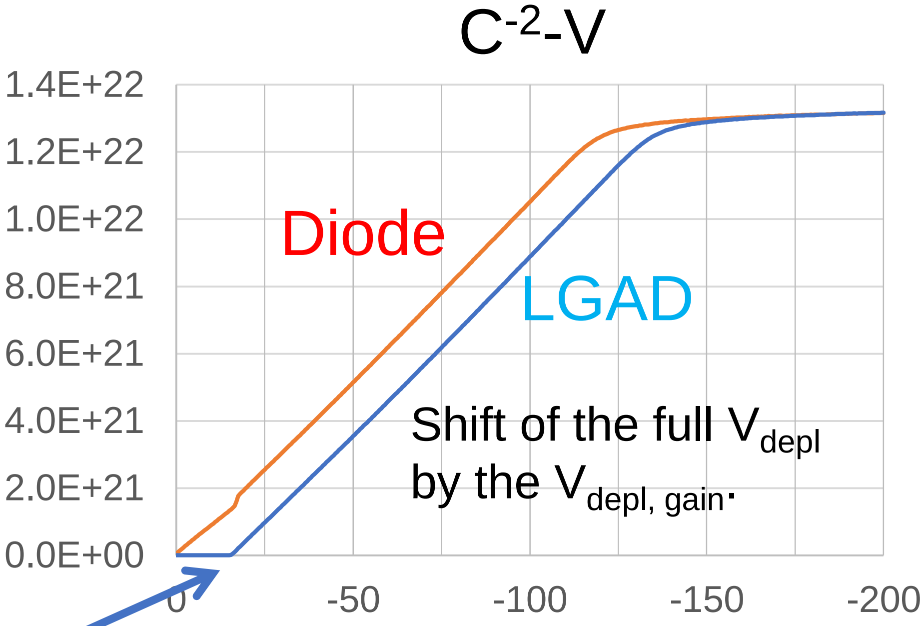
Capacitance


C-V

At depletion, capacitance as expected $C=\varepsilon A/th_{epi}$

Capacitance= 2pF/mm^2

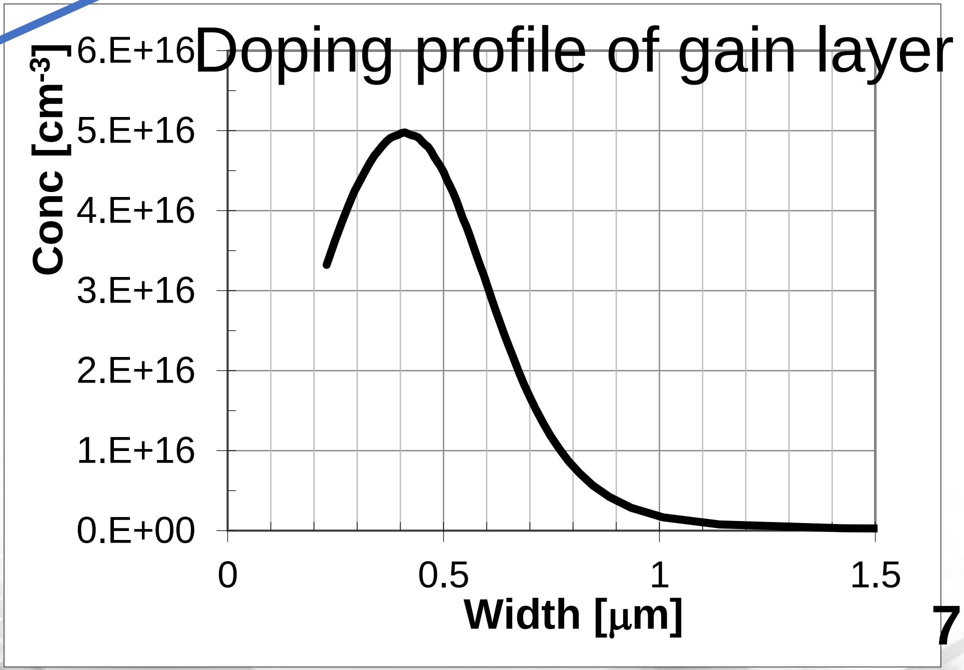
Depletion of Gain Layer


C^{-2}-V

Diode

LGAD

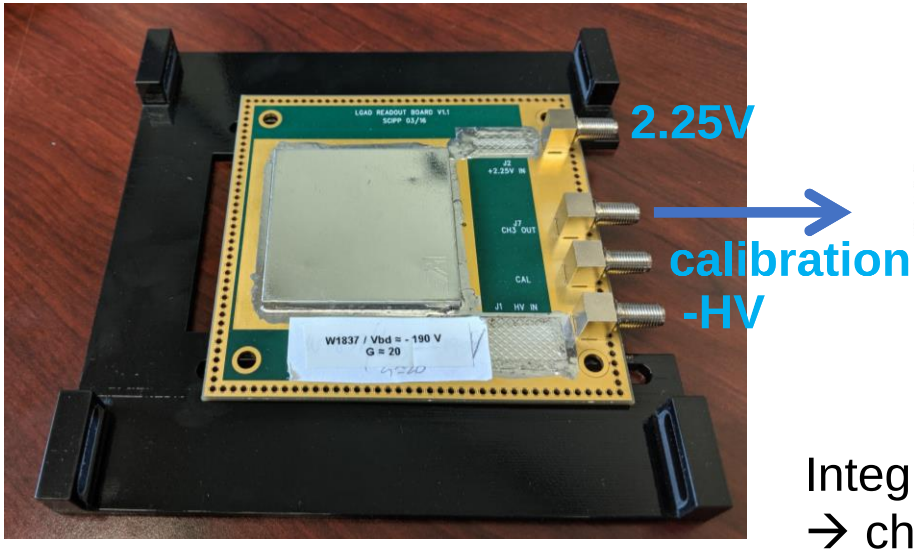
Shift of the full V_{depl} by the $V_{depl,\ gain}$.


Doping profile of gain layer

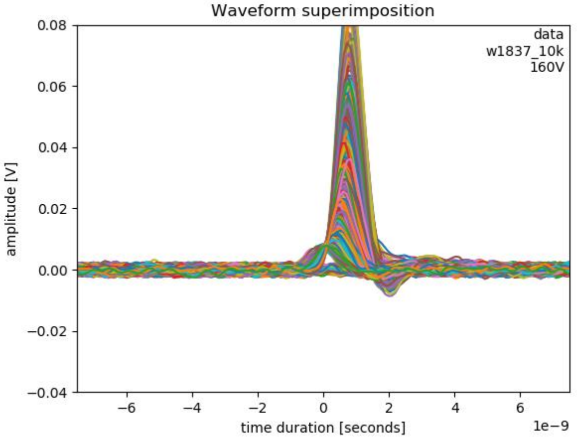
From TCAD simulations, gain layer should be deeper → compensated by n+. Go with Arsenic implant

Gain Measurements

TA board from SCIPP

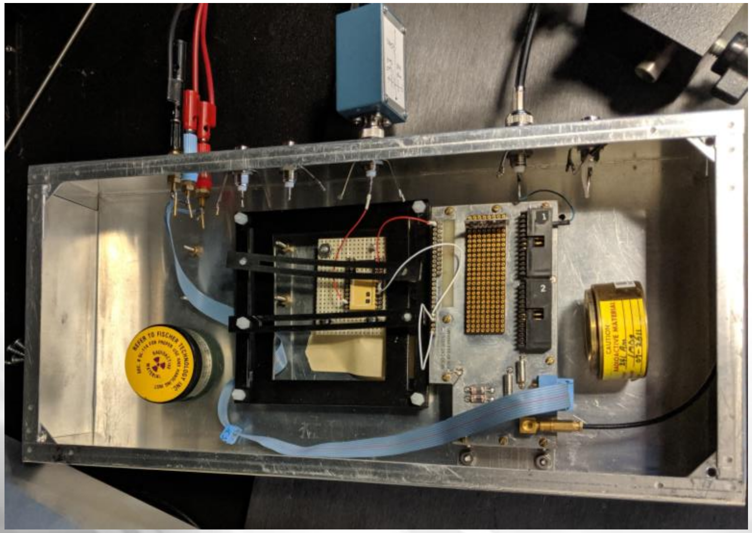


1Ghz scope (50Ohm termination)

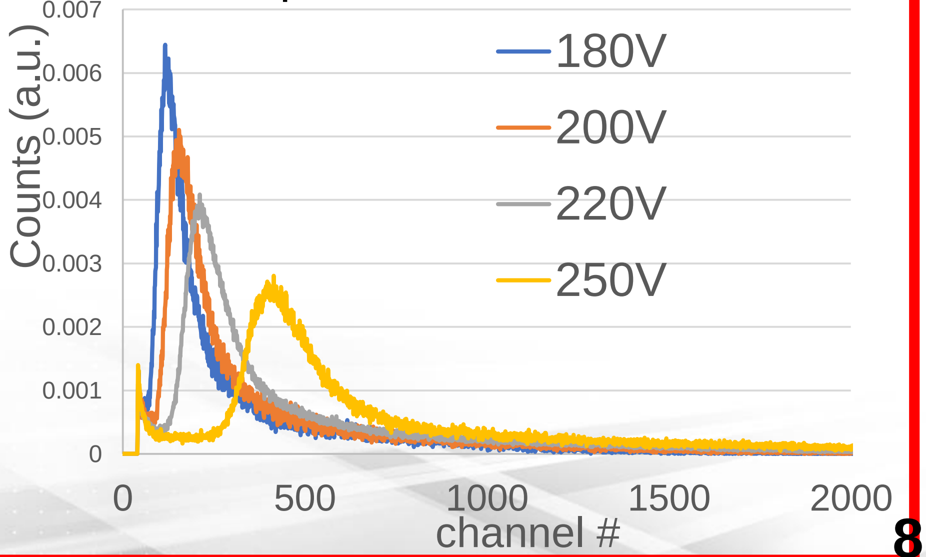


Integral(waveform[Vs]) / R_{feedback}
→ charge[C]

CSA from BNL



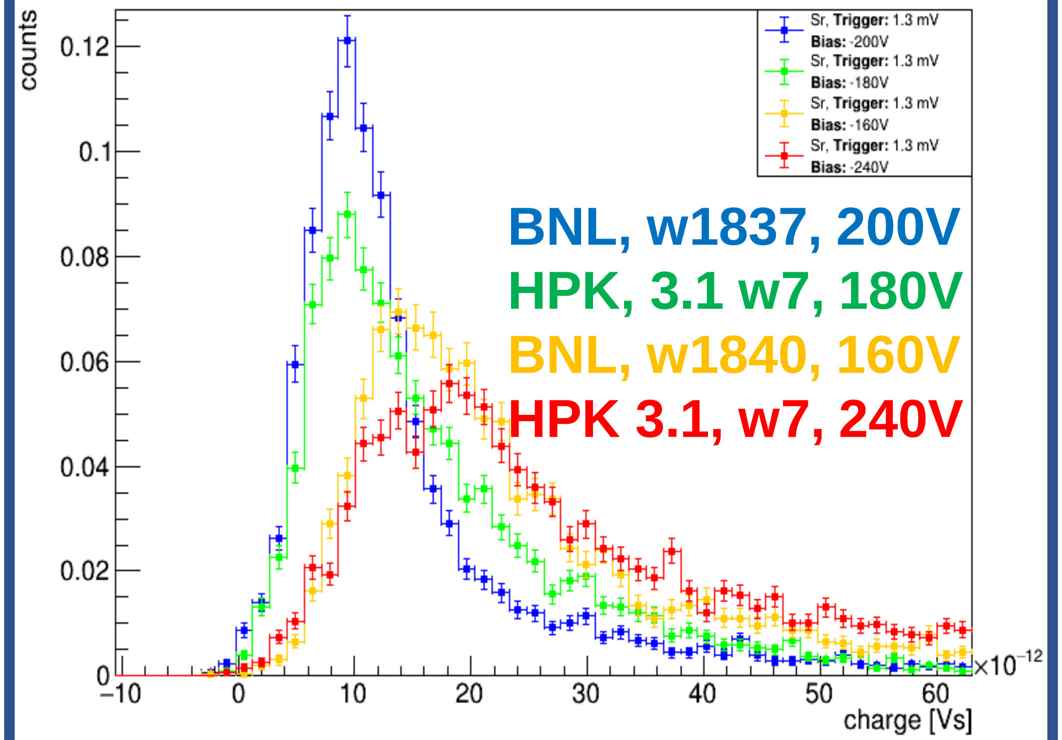
Sr spectra from HPK 3.1 w7



Gain Measurements -TA

signals from a ^{90}Sr source, TA measurements

Spectra from different LGADs mounted on SCIPP TA boards



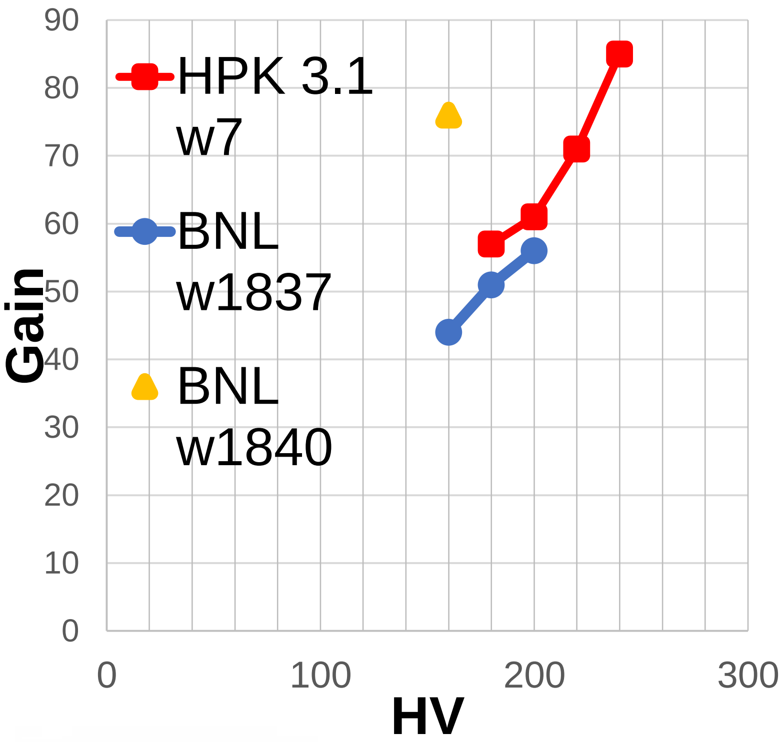
BNL, w1837, 200V

HPK, 3.1 w7, 180V

BNL, w1840, 160V

HPK 3.1, w7, 240V

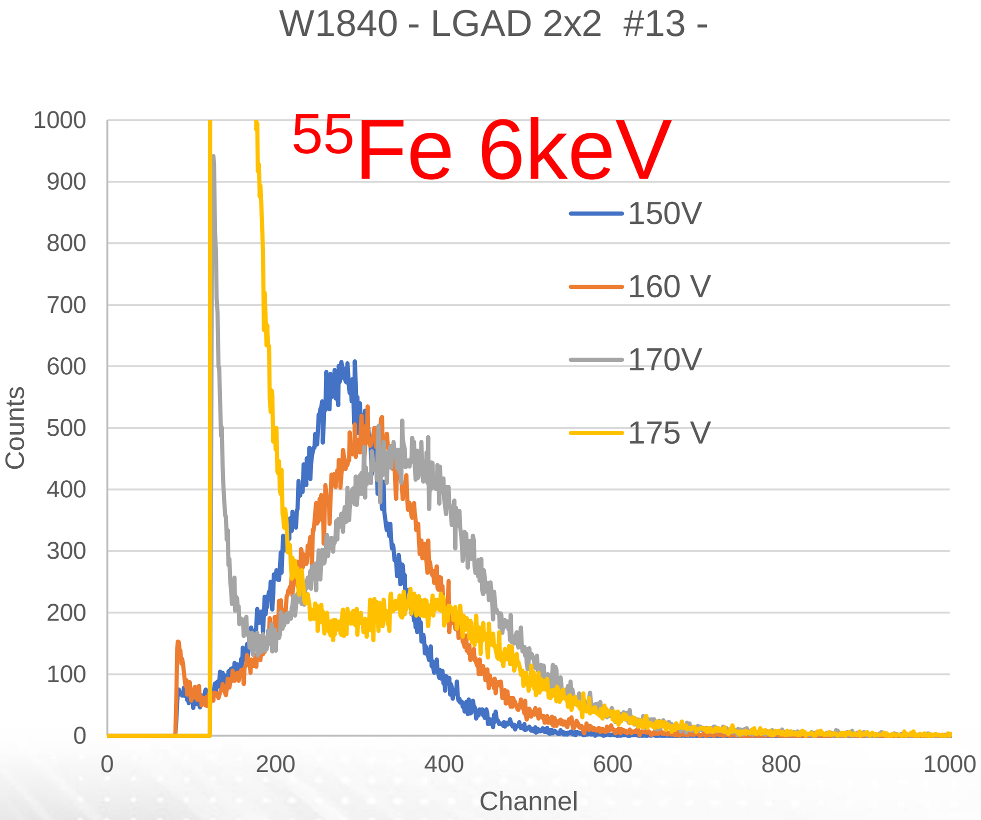
All LGADs are 50-um thick



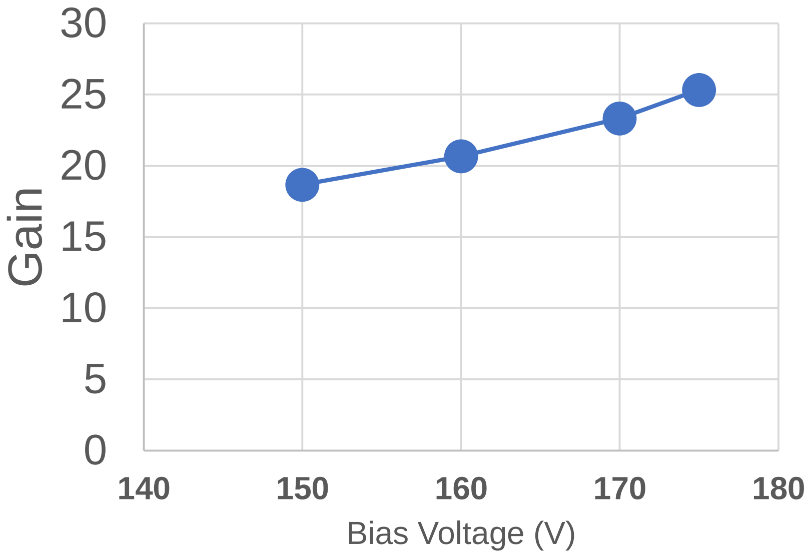
Gain Measurements - CSA

signals from X-ray sources

- ^{251}Am, ^{55}Fe + (Cu, Rb, Mo, Ag, Ba, Tb K lines generated by 60keV X-rays against targets)
- Signal from ^{55}Fe ~ ½ m.i.p. in 50µm of Silicon.



Gain of 70 with ^{90}Sr !!

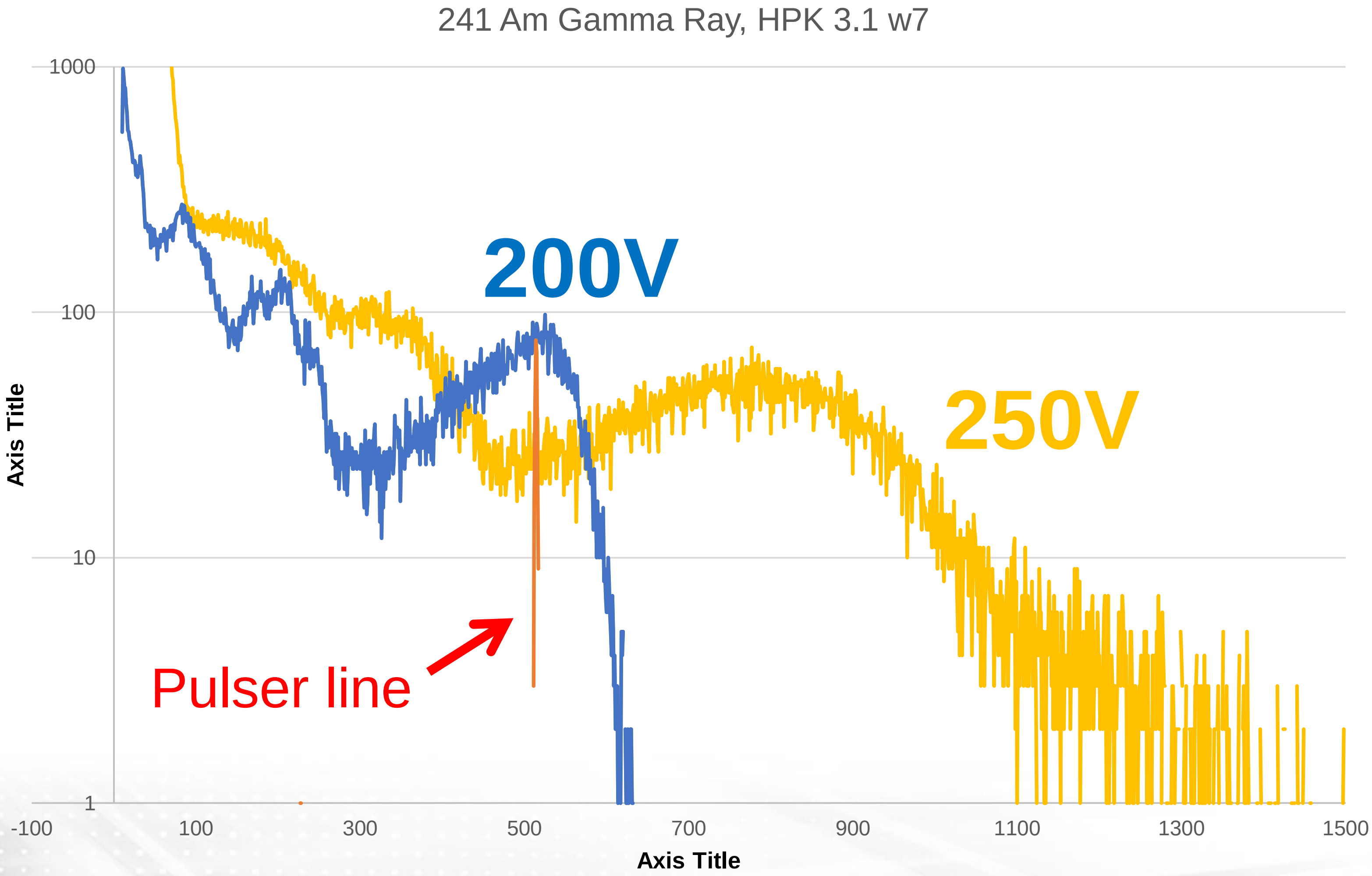


- Gain much less than Gain measured with ^{90}Sr: different shape of the charge cloud
- ^{55}Fe higher than gain with ^{251}Am: shielding effects?

Broad peaks are due to multiplication noise.
Pulser peaks are very narrow in this scale

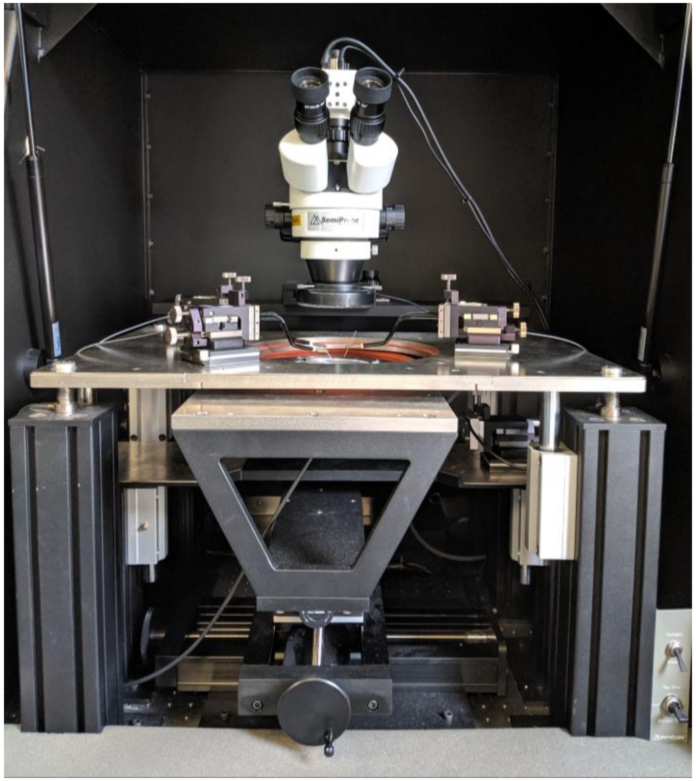
Gain Measurements - CSA

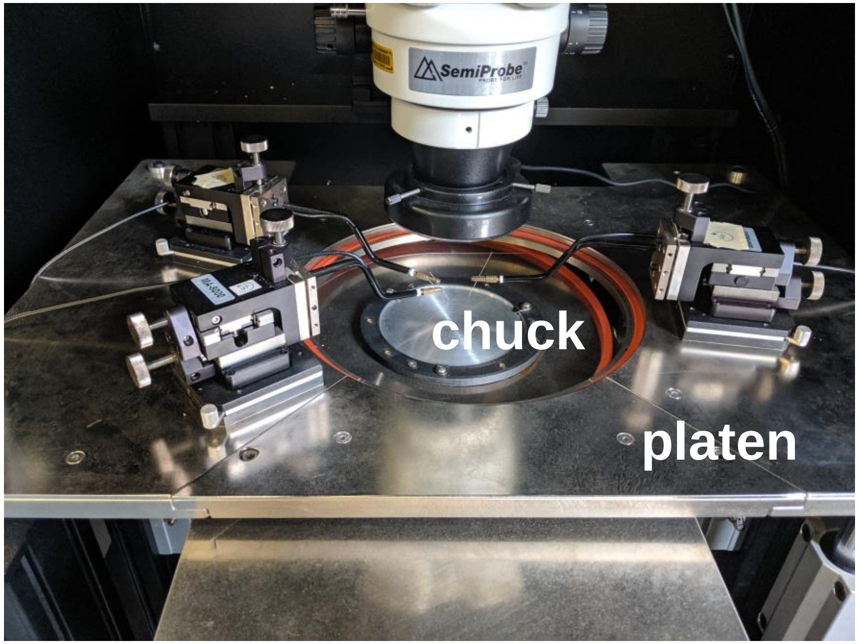
Also for HPK, gain with Sr >> gain with Gamma rays

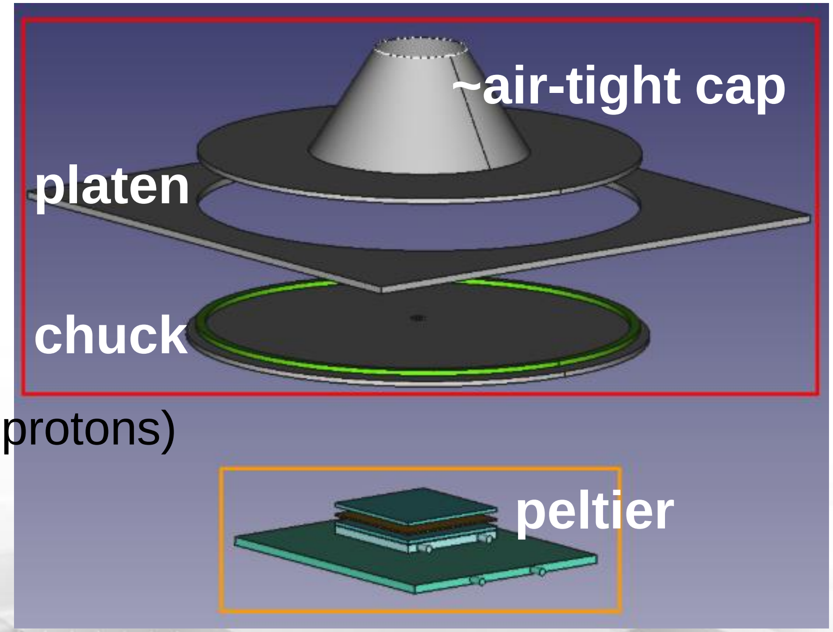


Next steps - 1

Upgrading of the probe station for “cold” I-V & C-V of irradiated devices







Irradiation campaigns:

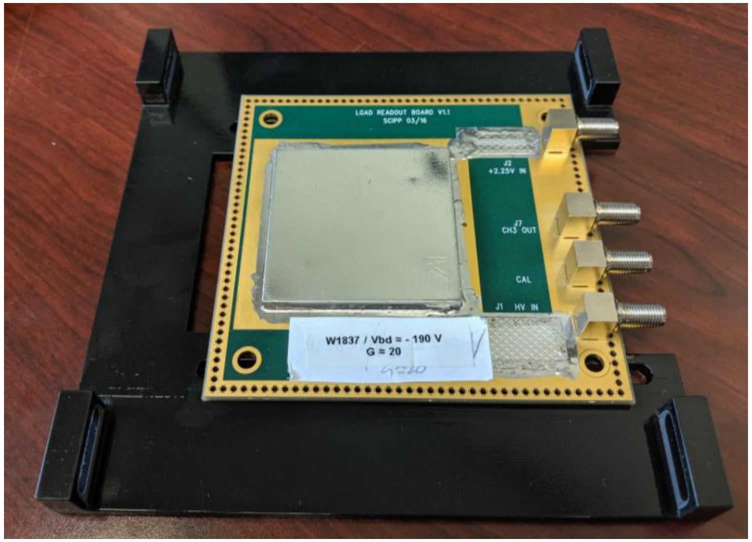
- Los Alamos (800-MeV protons)
- Tandem Van der Graaff (BNL) (26-MeV protons)
- TRIGA JSI (neutrons)

- Up to 1e16 n/cm^2, in steps

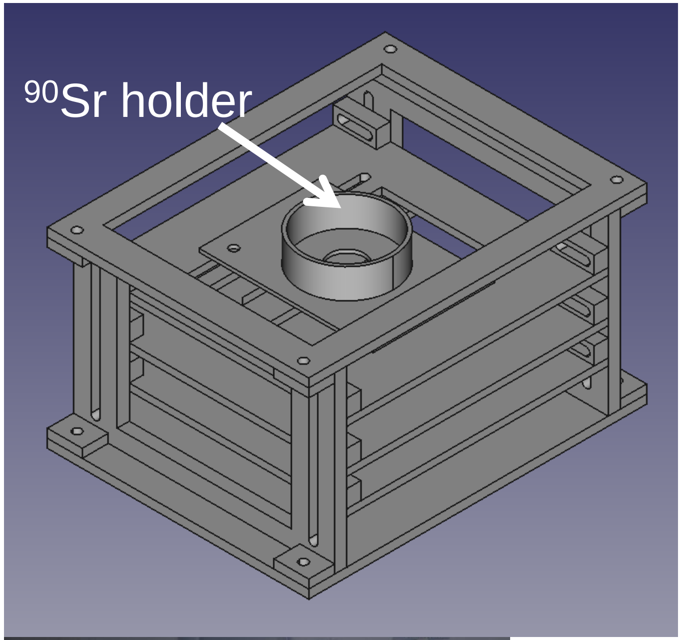
Next steps - 2

Telescope for timing measurements: Beta scope as SCIPP

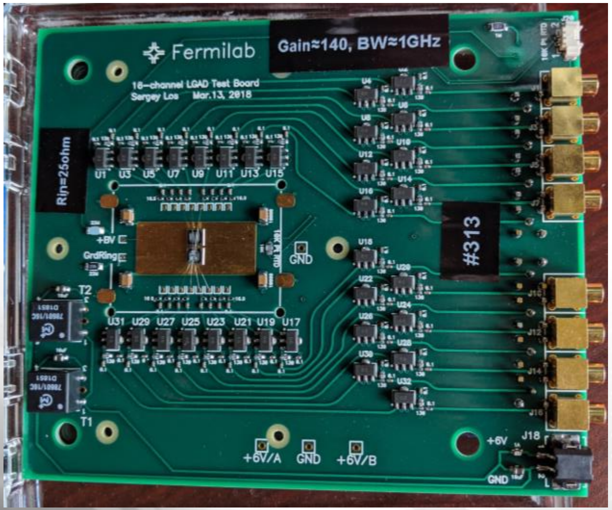
SCIPP TA on 3D-printed support



3D-printed telescope



Also multi-channel TA from FermiLab



A novel HV silicon JFET for ATLAS, and other silicon R&D activities at BNL

32nd RD50 workshop – 4-6 June 2018 Hamburg

Gabriele Giacomini, Wei Chen, Francesco Lanni, David Lynn, Alessandro Tricoli
(Brookhaven National Lab)

Enrico Rossi
(Stony Brook University and Brookhaven National Lab)

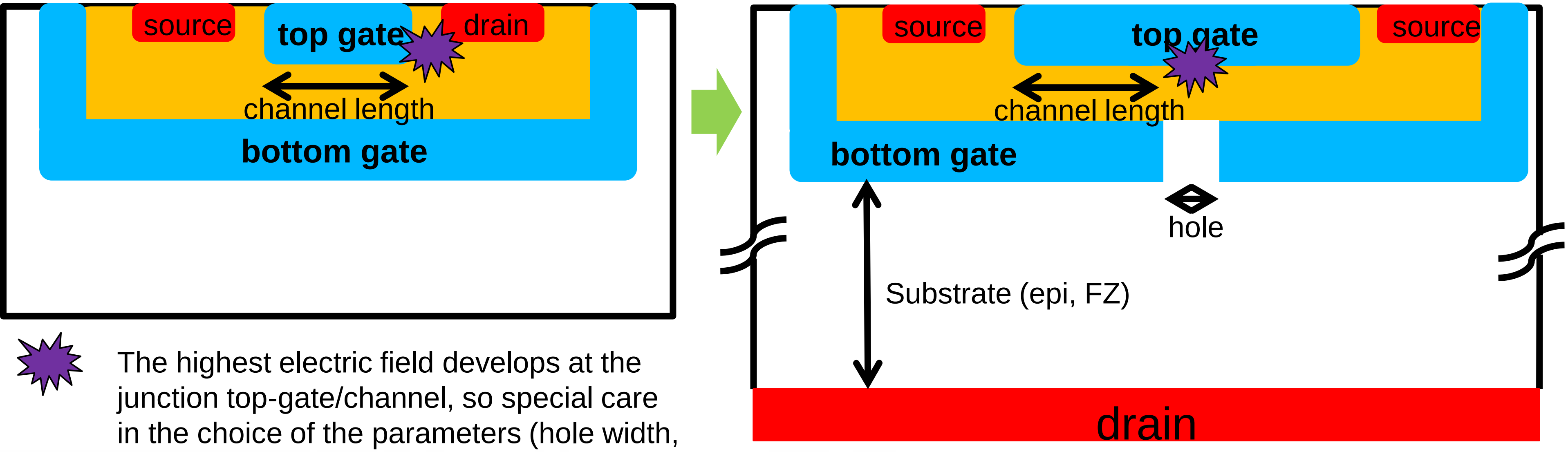
Irradiated at the TRIGA reactor at JSI with 4e14, 8e14, 1.5 e15 n_{eq}/cm^2

G. Giacomini, et al., “Fabrication and Electrical Characterization of High-Voltage Silicon JFETs”, 2019 JINST 14 P05007.
G. Giacomini, et al., “High-Voltage Silicon JFET for HV Multiplexing for the ATLAS MicroStrip Staves” POS(TWEPP2018)030.
G. Giacomini, et al., “A HV Silicon vertical JFET: TCAD simulations,” Nucl. Instrum. Methods A, vol. 919, 2019 , pp. 119-124.

The vertical HV Silicon JFET

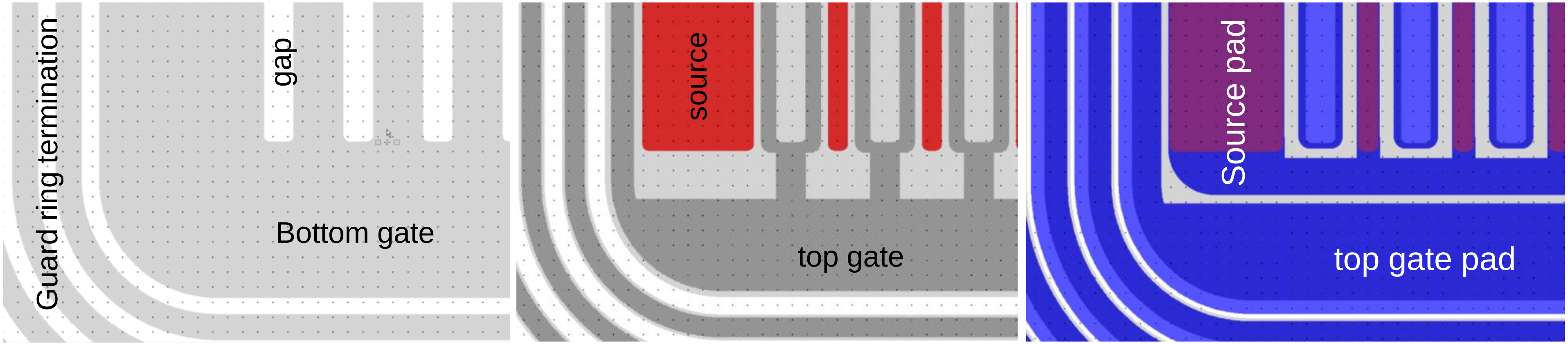
Originally, conceived as a rad-hard switch to be used in the ATLAS ITk HV-Mux. GaN JFETs are very rad-hard, so HV-Mux will go with GaN.

We can modify the structure of the standard JFET by making a gap in the bottom-gate.
Over the gap, the top-gate. The channel and the source as in the standard JFET. The drain is the back contact.
The current flows (= drifts) from source to drain through the gap in the bottom-gate.
The high voltage applied to the drain falls in the thick substrate, being the bottom-gate almost a planar implant.

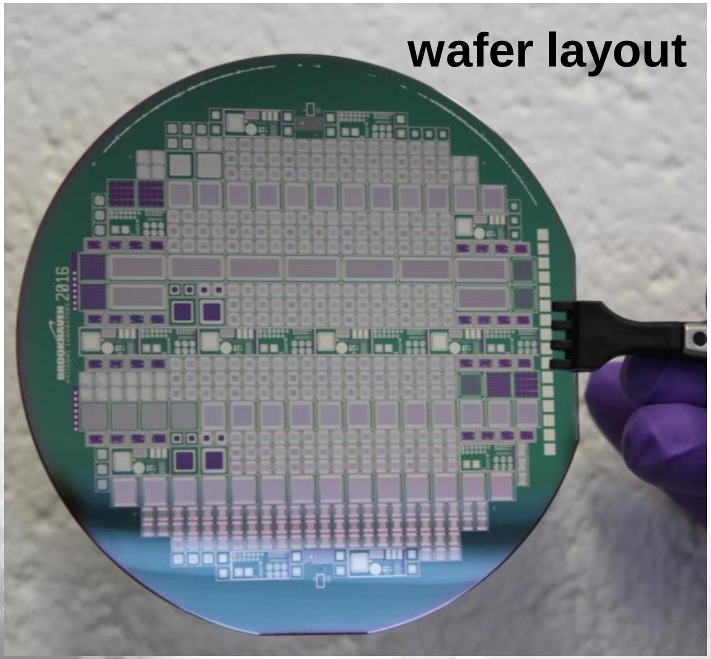


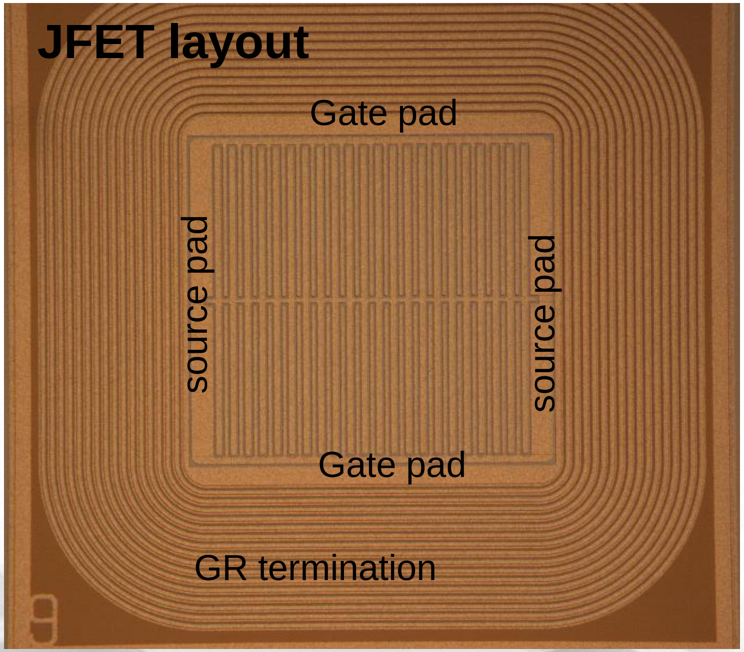
✸ The highest electric field develops at the junction top-gate/channel, so special care in the choice of the parameters (hole width, channel doping concentration).
GR termination also needed at the border of the bottom-gate.

The layout



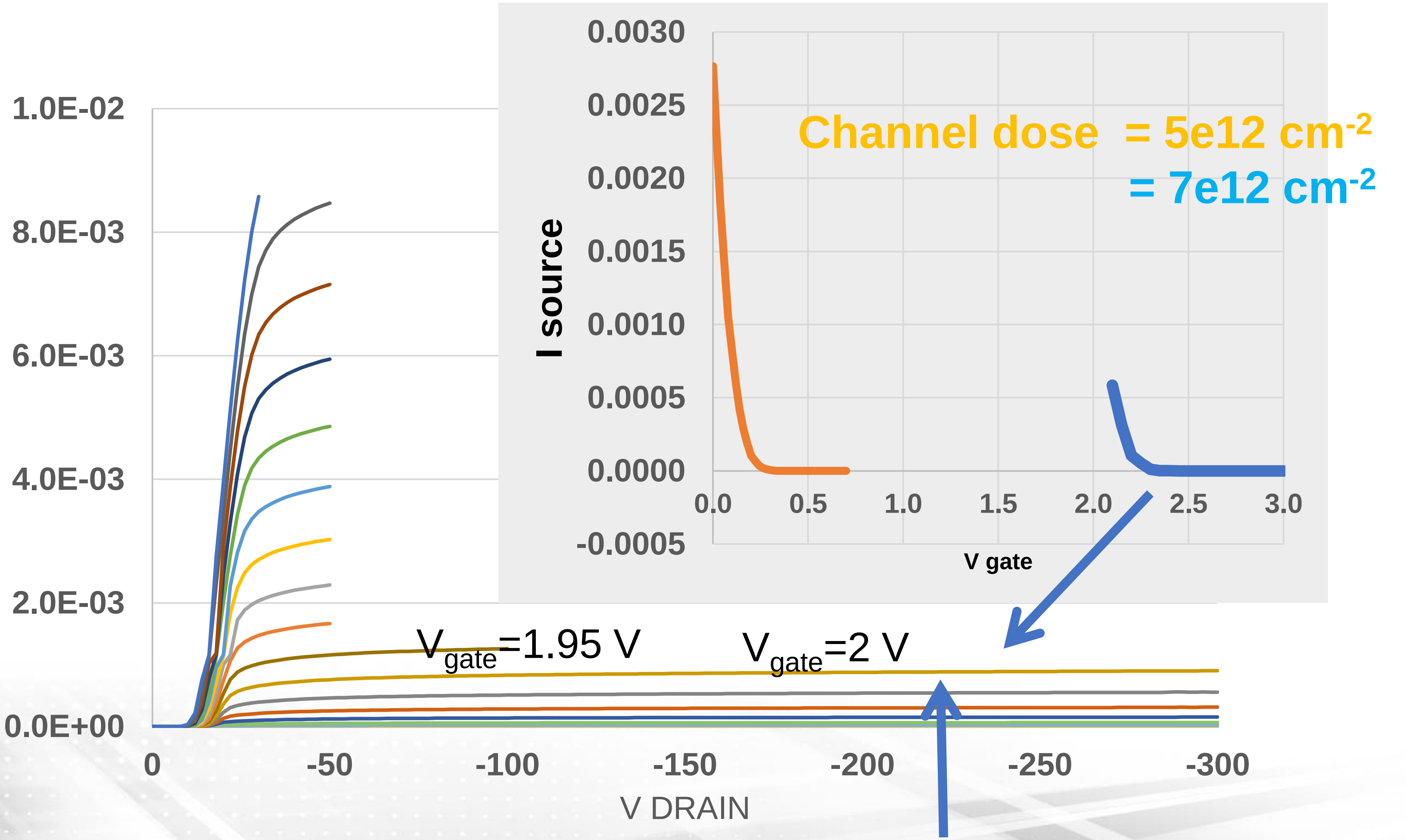
Interdigitated design to increase the gate width and thus the ON current (especially after irradiation).
The active area is 1x1 mm^2, which sets the gate width to 20 cm.
Triode configuration, top-gate connected to the bottom-gate.
6 photolithographic masks, 4 implants.
Both *n*-type and *p*-type JFET, on 4” epitaxial wafers (TOPSIL): 50μm thick, N_C~ 1e14cm^{-3}.





I-V characteristics before irradiation

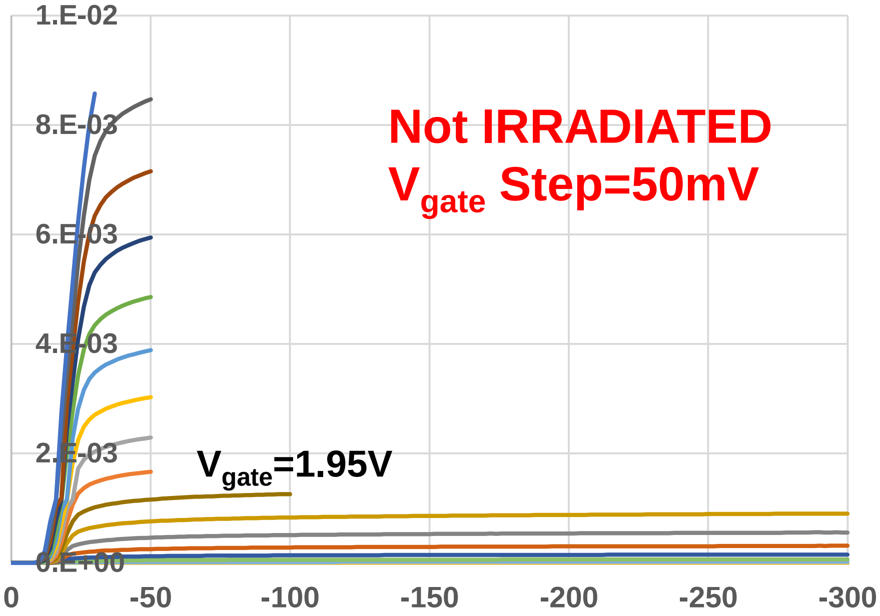
Splittings on the channel dose.
At the lower doses, the channel was pinched-off already at V_{gate}=0V
The higher the dose, the lower V_{BD}.



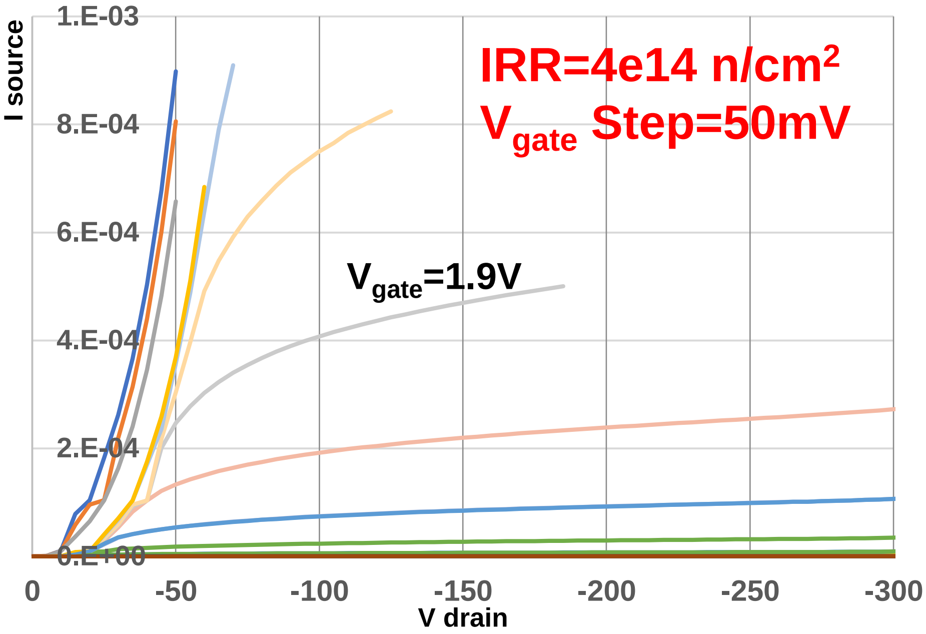
We irradiated the devices with higher current capability (but lower V_{bd})

Irradiation results

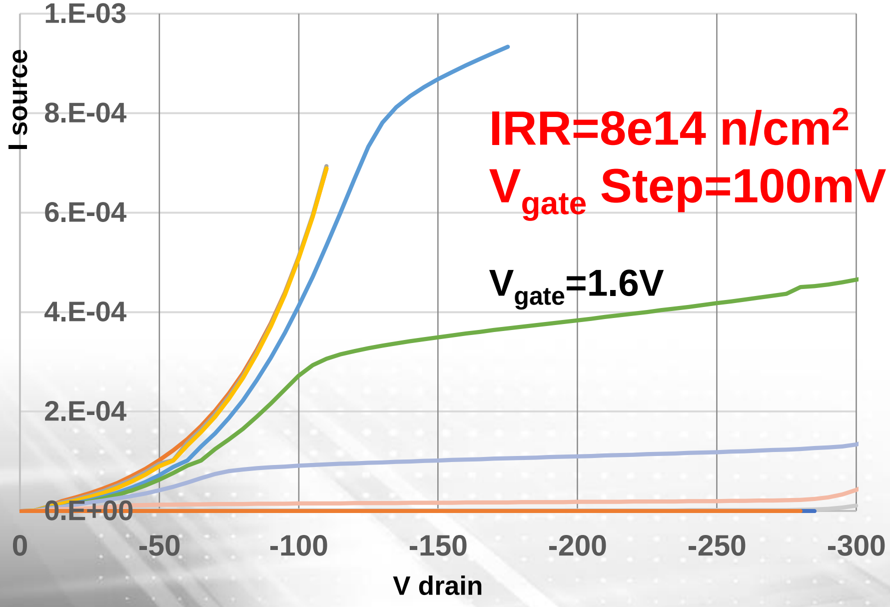
Neutrons at TRIGA, JSI


Not IRRADIATED
V_{gate} Step=50mV

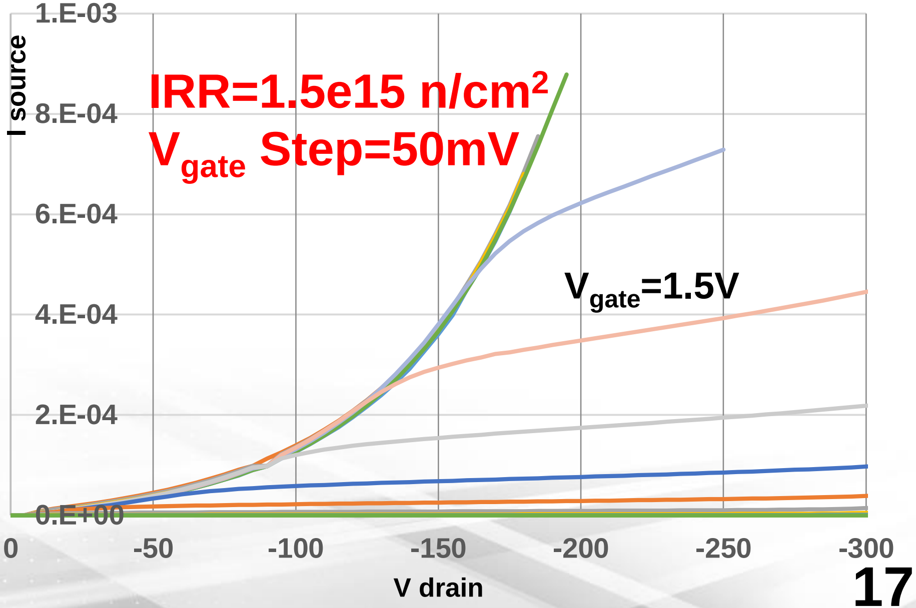
V_{gate}=1.95V


IRR=4e14 n/cm^2
V_{gate} Step=50mV

V_{gate}=1.9V

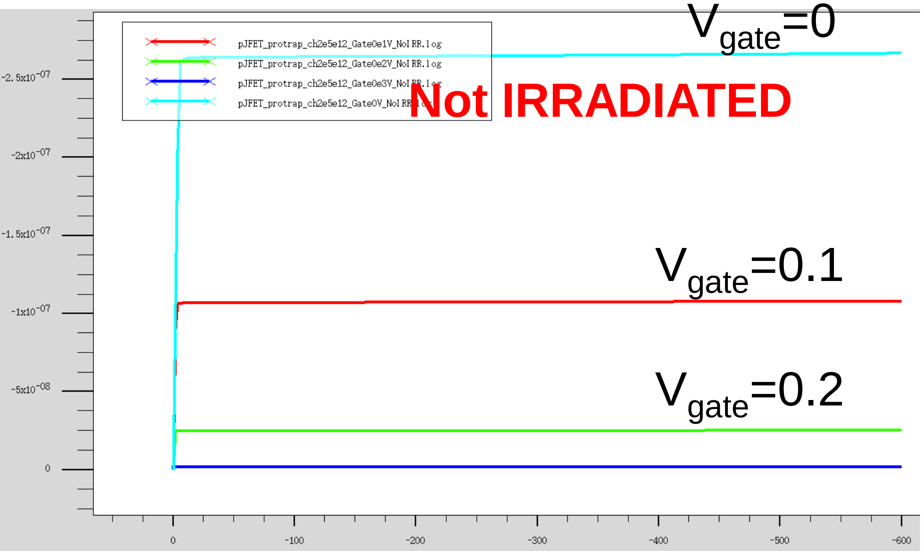

IRR=8e14 n/cm^2
V_{gate} Step=100mV

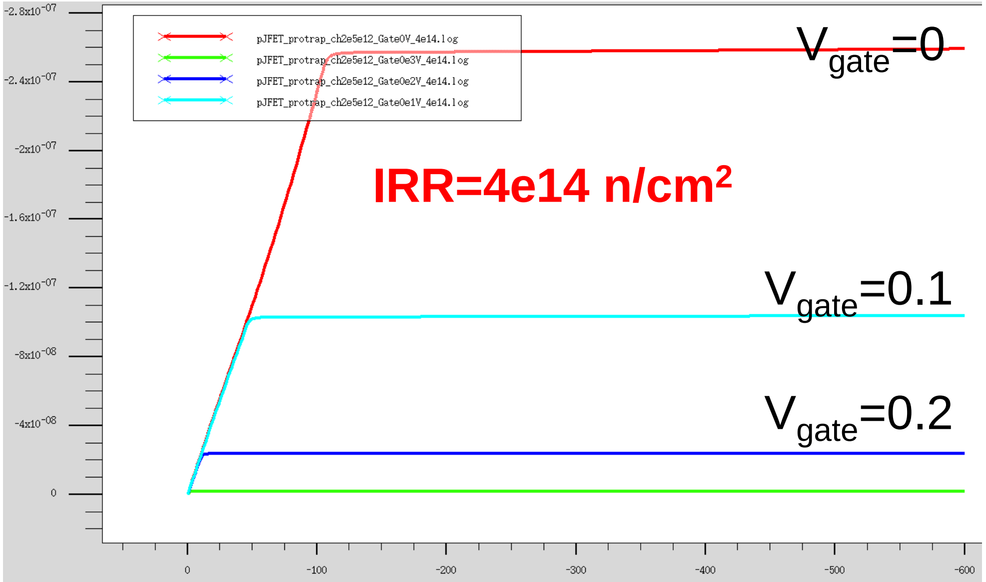
V_{gate}=1.6V

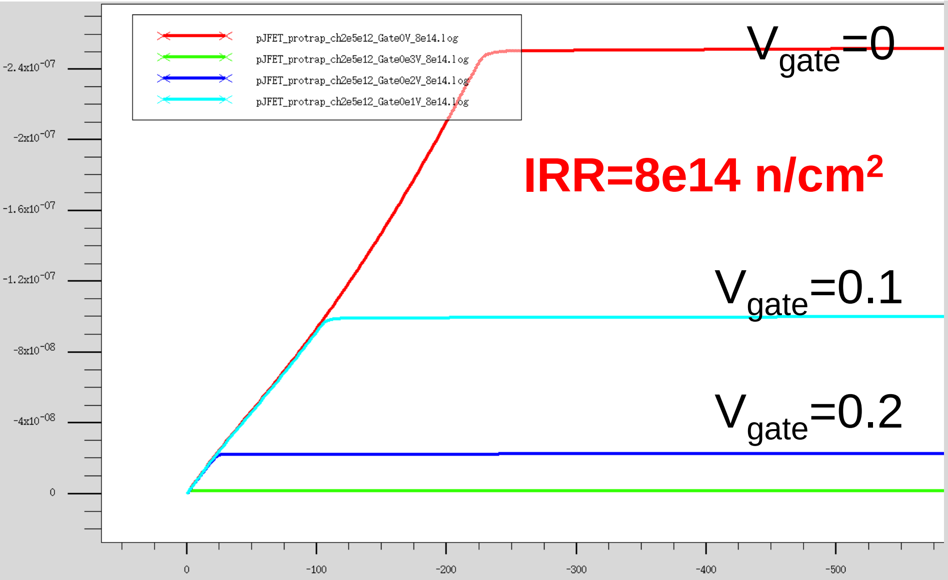

IRR=1.5e15 n/cm^2
V_{gate} Step=50mV

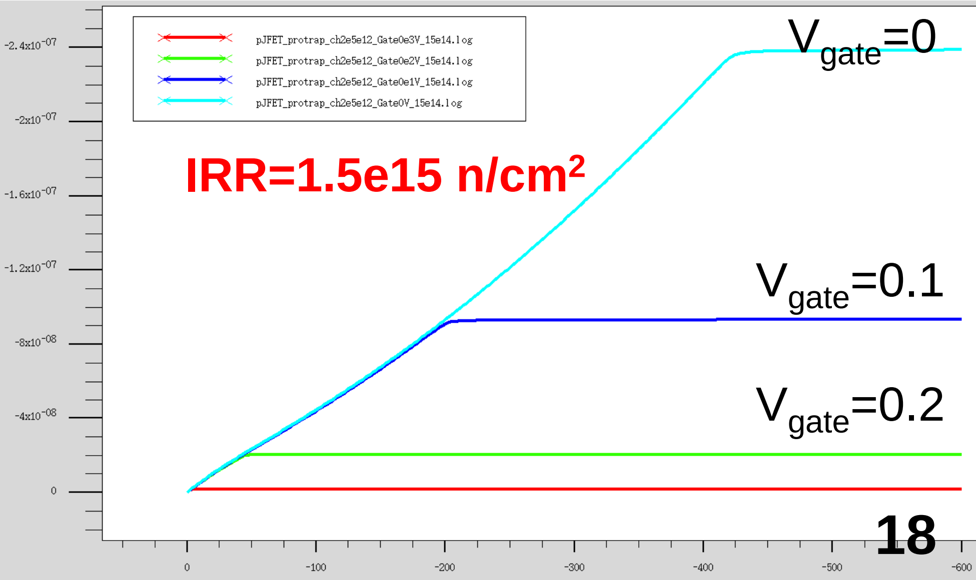
V_{gate}=1.5V

TCAD simulation of ideal irradiated HV-JFETs









Conclusions and Outlook

- Silicon Clean Room has fabricated LGAD with good performances
  - Still, some place for improvement (shallower implants, ..)
- Silicon lab testing capabilities to be expanded (cold probe station, beta scope)
  - X-ray gain measurements to be closely investigated

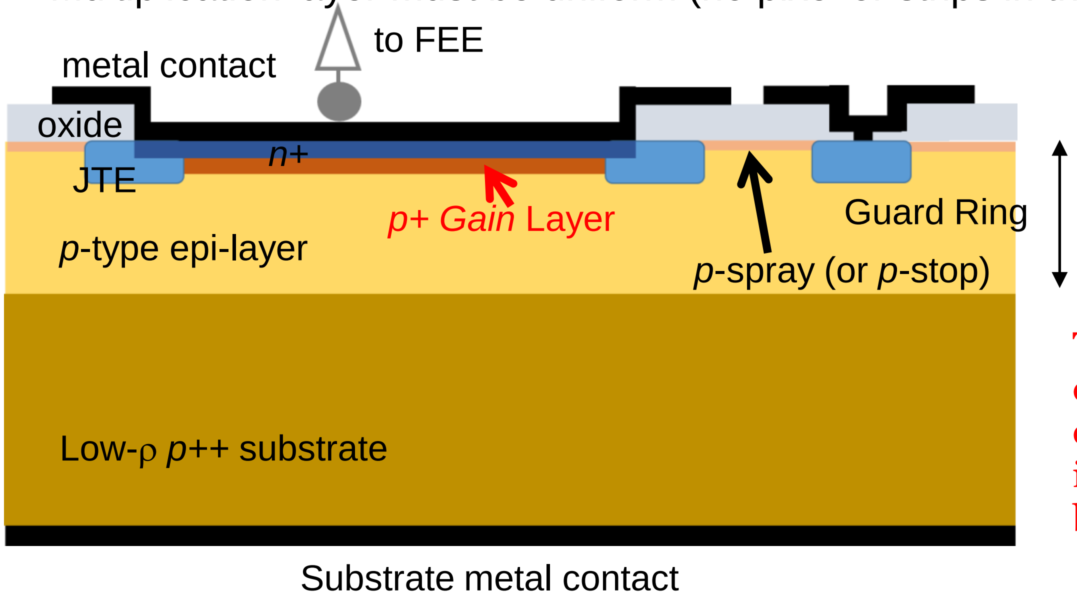
- HV-JFET fabricated tested and irradiated.
  - irradiation results to be understood by means of TCAD

BACK-UP

LGAD structure

LGAD are intended to be used in HEP thanks to their fast-timing properties, (timing detectors for the upgrades of the ATLAS and CMS at the High Luminosity LHC) .

- Same principle of APD but lower gain, without breakdown
  - Electrons must initiate the avalanche, not holes → *p*-type substrates/gain layers
- Multiplication layer must be uniform (no pixel or strips in the multiplication region: only pads ~mm^2)



30-50 µm: the thin substrate of a few tens of microns allow fast carrier collection.

The main characteristic is a thin and highly-doped *p*+ gain layer under the pad that enhances the Electric Field and provides internal and moderate gain (~ 10-20), that boosts the signal.

G. Giacomini, et al. “Development of a technology for the fabrication of Low-Gain Avala

Type : S10938-6093-SMPL

Lot No. : EXX28995-WNo7

for ATLAS

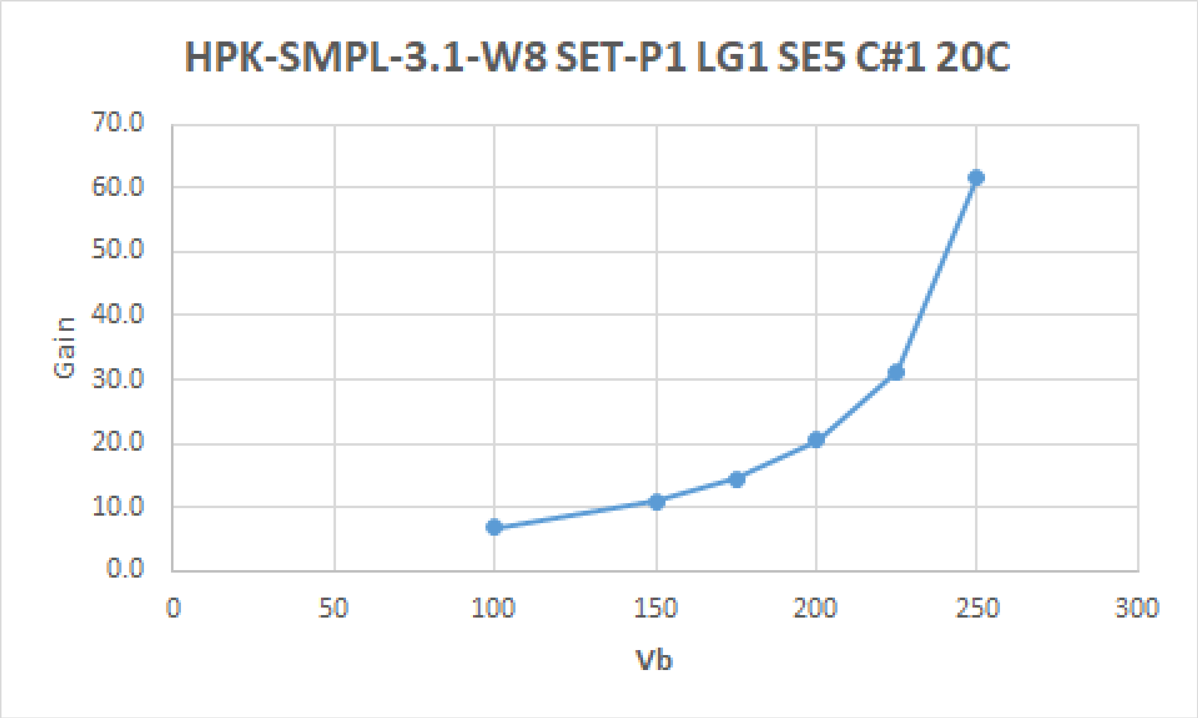
CHIP : Single SET-P5

NOTE : Type3-1 (with UBM)

MADE IN JAPAN

HAMAMATSU

PHOTON IS OUR BUSINESS



HPK-SMPL-3.1-W8 SET-P1 LG1 SE5 C#1 20C