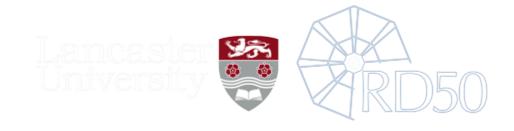
34th RD50 Workshop (Lancaster)



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Status of LGAD development at BNL (and other silicon R&D activities)

Wednesday, 12 June 2019 13:00 (20 minutes)

Profiting from our internal silicon-dedicated clean-room facility, we developed an LGAD technology in-house. We fabricated single pads and arrays of pads on several 50-um thick p-type epitaxial wafers. The wafers differ for the implantation parameters (i.e., energy and dose) of the gain-layer, resulting in the achievement of gains in a wide range. We attain maximum gains in the order of 25, measured with an 55Fe source, while signals are very fast, due to the thin substrates. We report the performance of our devices, from probe station measurements to functional tests with radioactive sources. At BNL we are also involved, within the ATLAS HGTD collaboration, in the characterization of LGADs fabricated by several vendors, which allows us to compare performance of LGADs in a broader range of technologies. We also update on the performance after neutron irradiation of a High-Voltage silicon vertical JFET, a new device initially conceived as a candidate for the High-Voltage Multiplexing switch in the ATLAS upgrade of the silicon microstrip Inner Tracker (ITk).

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