Development of a modular DAQ to characterize the RD50 depleted monolithic active pixel sensors

Ricardo Marco Hernández
IFIC (CSIC-UV)
on behalf of:
HEPHY (Vienna, Austria)
University of Liverpool (Liverpool, UK)
IFIC (Valencia, Spain)

Outline

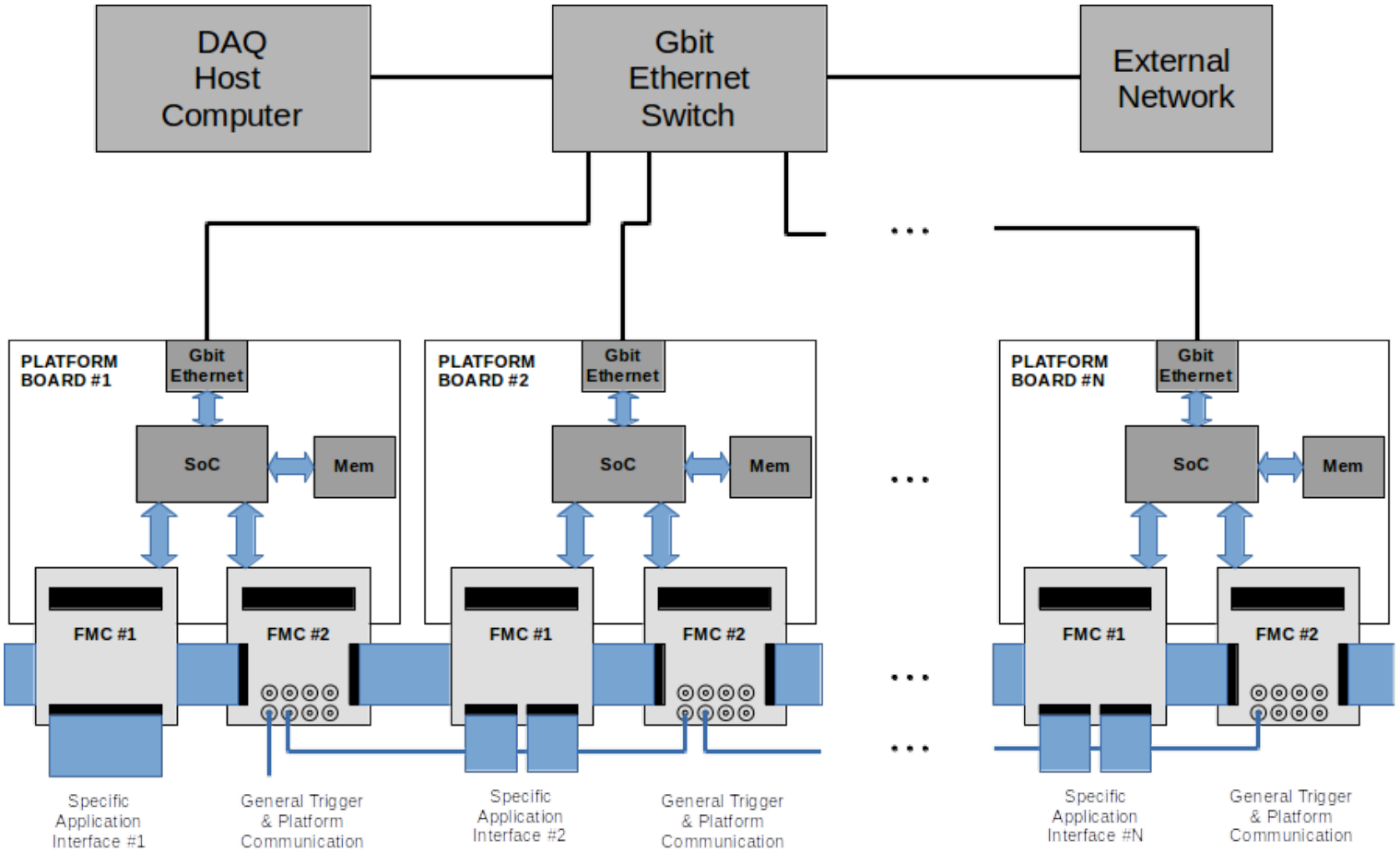
- Introduction.
- DAQ architecture.
- DAQ hardware.
  - Platform boards.
  - FMC CaR board.
  - FMC General Purpose Interface (GPI) board.
  - FMC Trigger and Communication board.
  - Chip board for the RD50-MPW1.
  - Chip board for the RD50-MPW2.
- DAQ firmware and software.
- Future plans.

Introduction

- We want a DAQ...
  - To read out and to control different DMAPS (HV-CMOS structures).
  - To be able to process external trigger input signals (e.g. signal derived from a radioactive source).
  - To be able to generate trigger output signal (e.g. for driving a laser system).
  - To work both in standalone mode (e.g. a basic laboratory test bench) and in a test beam environment (e.g. several read out planes are required with synchronization).
  - With user friendly DAQ software.
  - Easily scalable, configurable and modular to have flexibility for current and future applications.
- How we think we can develop it...
  - Combining FPGA resources with processor(s) to have more flexibility: System-on-chip (SoC).
  - Modularity and standardization: FMC connectors to connect function specific FMC modules to a common platform board.
  - Data storage capability: on-board volatile and non-volatile memory required.
  - Fast system control and bulk data transfer to host computer: Gigabit Ethernet communication.
  - Use a development board to shorten development time.

DAQ architecture

- Several platform boards can be used at the same time synchronized or not.
- Platform board has a SoC, on-board memory, Gigabit Ethernet communication and two FMC connectors.
- FMC board 1 is a custom board for a specific application (e.g. read-out/control HVCMOS devices): FMC CaR board is being used for RD50-MPW1. A new FMC GPI board is being developed as an alternative.
- FMC board 2 is a custom board used for trigger input/output processing and platform communication & synchronization (LVDS signals). This board is currently being developed.



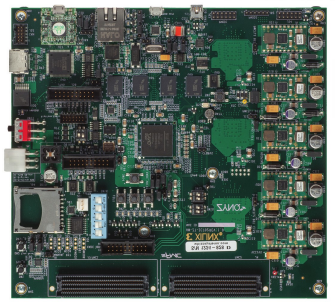
Block diagram of custom DAQ system

DAQ hardware: platform boards

- Application specfic chip board for different ASICs/detectors with minimum functionality and defined connector (SEAF type).
- FMC modules for interfacing close to the chip to provide commonly required resources: FMC CaR board/FMC GPI board.
- Other FMC modules for other purposes working in parallel: FMC Trigger and Communication board.
- SoC platform board can be placed in a safe distance (~ 50 cm) from the chip board using FMC cable assembly.
- Platform board: ZC702 or ZC706 development boards from Xilinx.
  - SoC is Zynq-7000 with a dual-core ARM Cortex-A9 and a mid-range Artix 7 FPGA.
  - Two FMC connectors: HPC/LPC or LPC/LPC.
  - Tri-mode Ethernet PHY (10/100/1000 Mbps).
  - 1 GB DDR3 SDRAM memory.
  - 128 Mb SPI flash memory.
  - SD card interface (8GB card included).
  - 12 V/5 A power input.
  - Other features (USB, HDMI, XADC, etc).

ZC706 board

or



ZC702 board

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FMC cable (optional)

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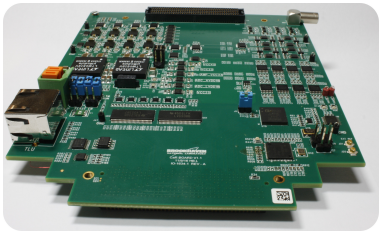

FMC CaR board or FMC GPI board

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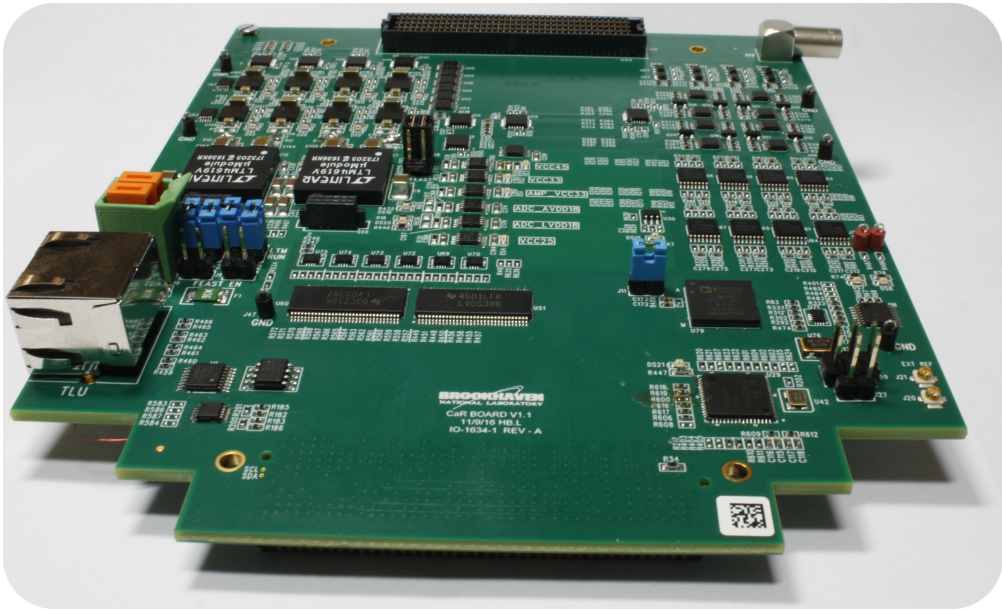
Application specific chip board

DAQ hardware: FMC CaR interface board

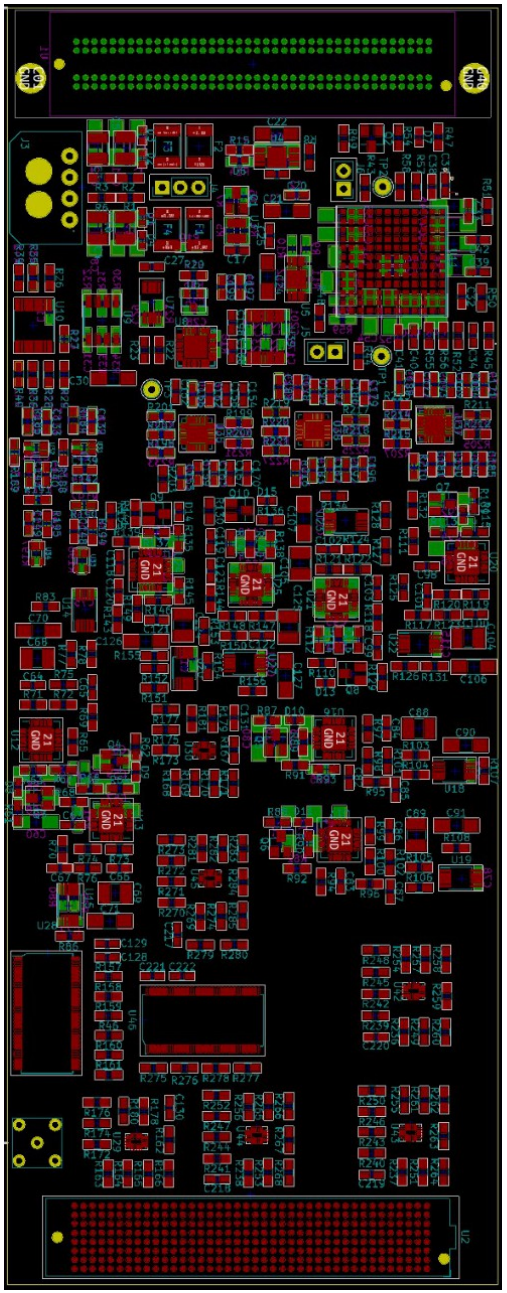
- FMC mezzanine board to interface multiple chip boards from Caribou DAQ.
- Very interesting board to be used as a generic FMC mezzanine in any DAQ.
- Support of many voltage levels and communication standards with local measurement and monitoring capabilities.
  - 8 power supplies (0.8 - 3.6 V/3 A).
  - 32 adjustable voltage outputs (0 - 4 V).
  - 8 current outputs (0 – 1 mA).
  - 8 voltage inputs (0 - 4 V).
  - 8 full-duplex SERDES links.
  - ADC (16 channels, 65 MSPS and 14-bit).
  - 4 injection pulser.
  - HV input.
  - I2C bus.
  - TLU RJ45 input
  - General CMOS signals (10 outputs and 14 inputs).
  - 17 LVDS pairs.
  - Output jitter attenuator and clock multiplier.



FMC CaR interface board

DAQ hardware: FMC GPI board

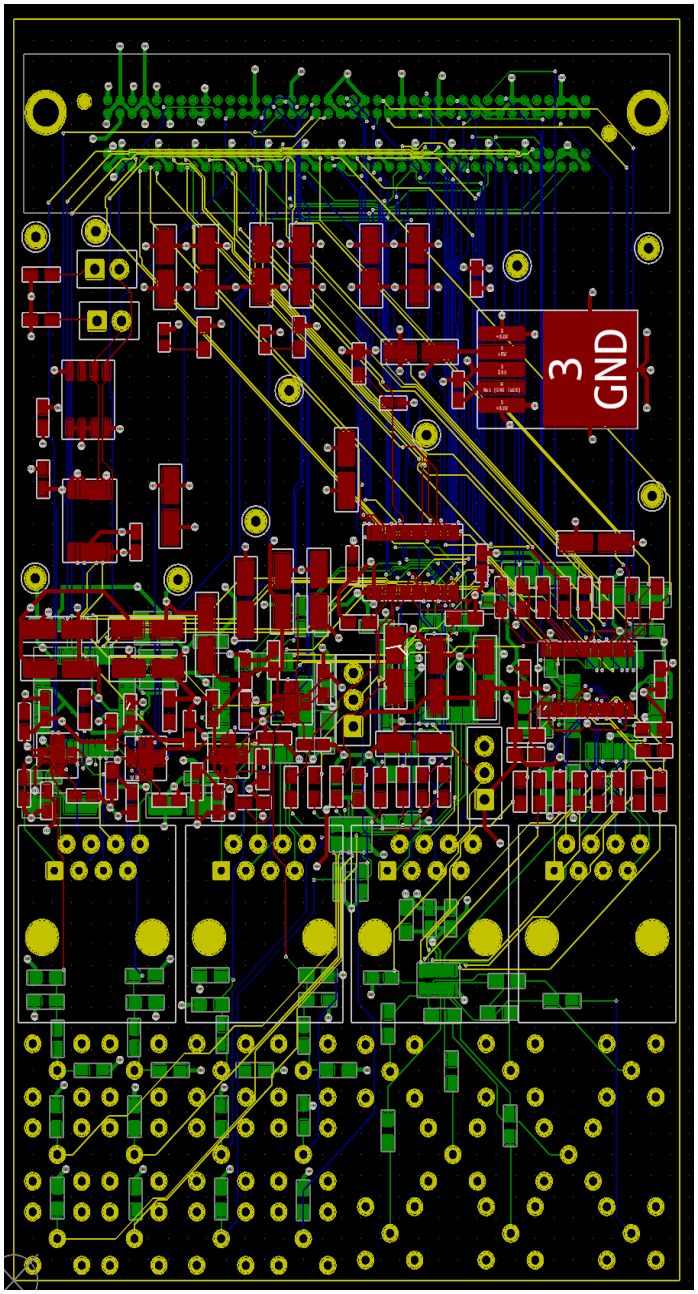
- FMC board which will be able to be used as an alternative to the FMC CaR board.
- Smaller size (69 x160 mm) and less components than CaR board. 8 layers stack-up.
- FMC-LPC and SEAF connectors compatible with FMC CaR board.
- No external power required: it uses FMC levels.
- Main features:
  - 10 output power supplies with monitoring capabilities.
    - 8 configurable (0-3.6V/0.55A, 0-3V/1A and 0-2.2V/1.5A).
    - 2 fixed:3.3V/0.5A and 2.5V/0.5A
  - 32 adjustable voltage outputs (0-4V).
  - ADC (12-bit, 50 ksps, 8 channels, I2C).
  - 2 injection pulsers.
  - General CMOS signals (10 outputs and 7 inputs) with adjustable voltage levels (0.8-3.6V).
  - 17 LVDS pairs.
- Currently being designed. PCB expected to be finished in July.



FMC GPI board preliminary layout

DAQ hardware: FMC Trigger and Communication board

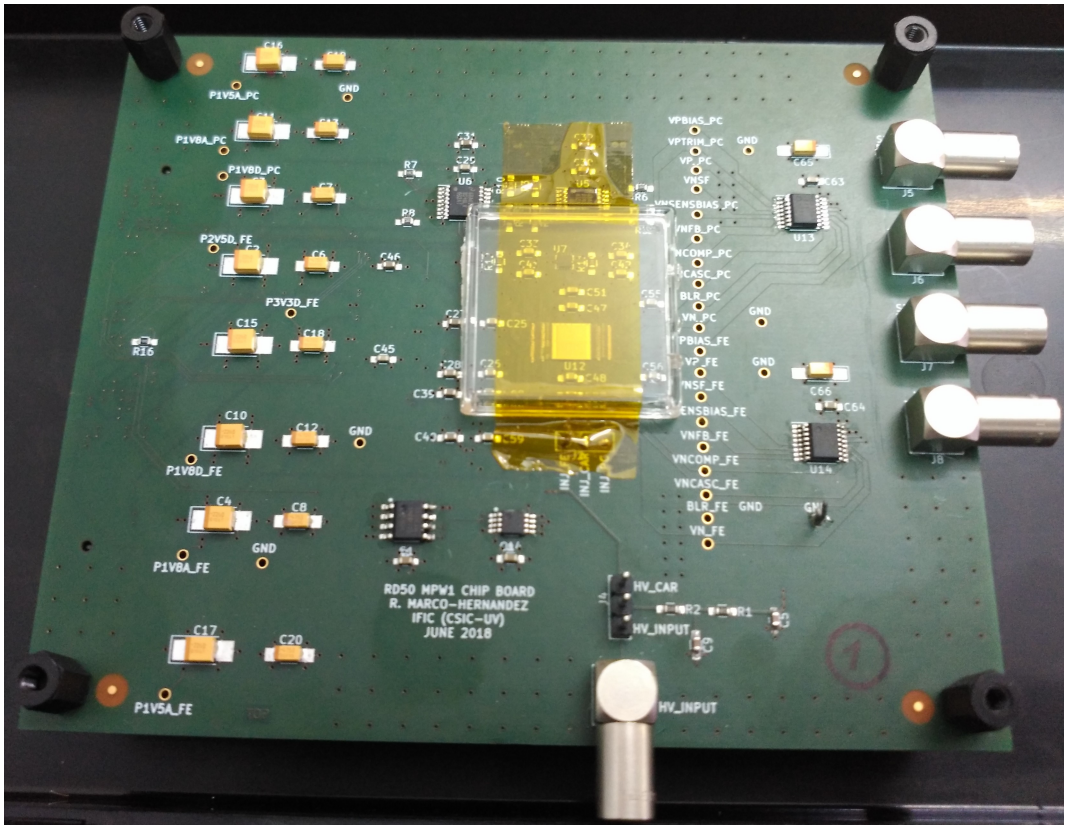
- FMC board which will be able to be used for different purposes.
  - Capture and generate trigger signals.
  - Implement synchronized communication among platform boards.
  - General purpose digital I/O.
- This module will allow us to use the DAQ as a telescope.
- Board size of 69 mm x 120 mm with a FMC-LPC connector. 8 layers stack-up.
- No external power required: it uses FMC levels.
- Main features:
  - 8 digital outputs with adjustable voltage levels (3.3V/5V) through lemo comnectors.
  - 8 digital inputs with adjustable voltage levels (3.3V/5V) through lemo connectors.
  - 4 analogue/digital discriminated AC coupled inputs (0-5V) through lemo connectors.
  - 8 LVDS inputs through 2 RJ45 connectors. TLU compatible.
  - 8 LVDS outputs through 2 RJ45 connectors.
  - I2C unique ID and 2k EEPROM.
- PCB layout being carried out. PCB expected to be finished in July.



FMC Trigger and Communication board preliminary layout

DAQ hardware: RD50-MPW1 chip board

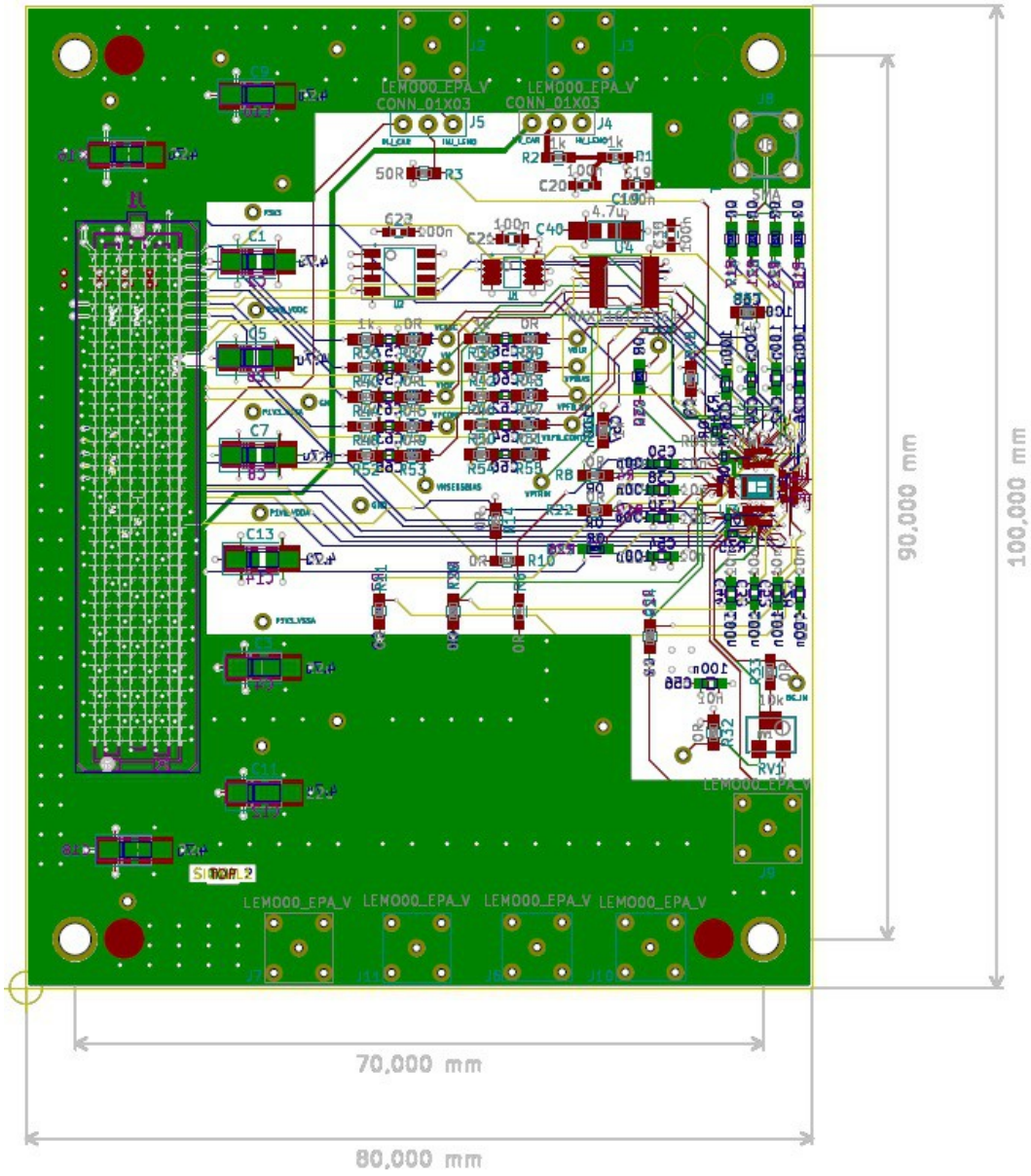
- Specific chip board which accomodates one RD50-MPW1 chip.
- Compatible with the CaR board and the FMC GPI board.
- 100 mm x120 mm size and 8 layers stack-up.
- LVDS-CML and CML-LVDS converters on board.
- I2C ADCs, I2C thermometer, unique ID and 2k EEPROM.
- Currently being used at HEPHY, Liverpool and IFIC for RD50-MPW1 measurements.
- 6 units produced by IFIC and 3 assembled at HEPHY. 2 unit sent to Liverpool. Last unit available at IFIC.



RD50-MPW1 chip board

•DAQ hardware: RD50-MPW2 chip board

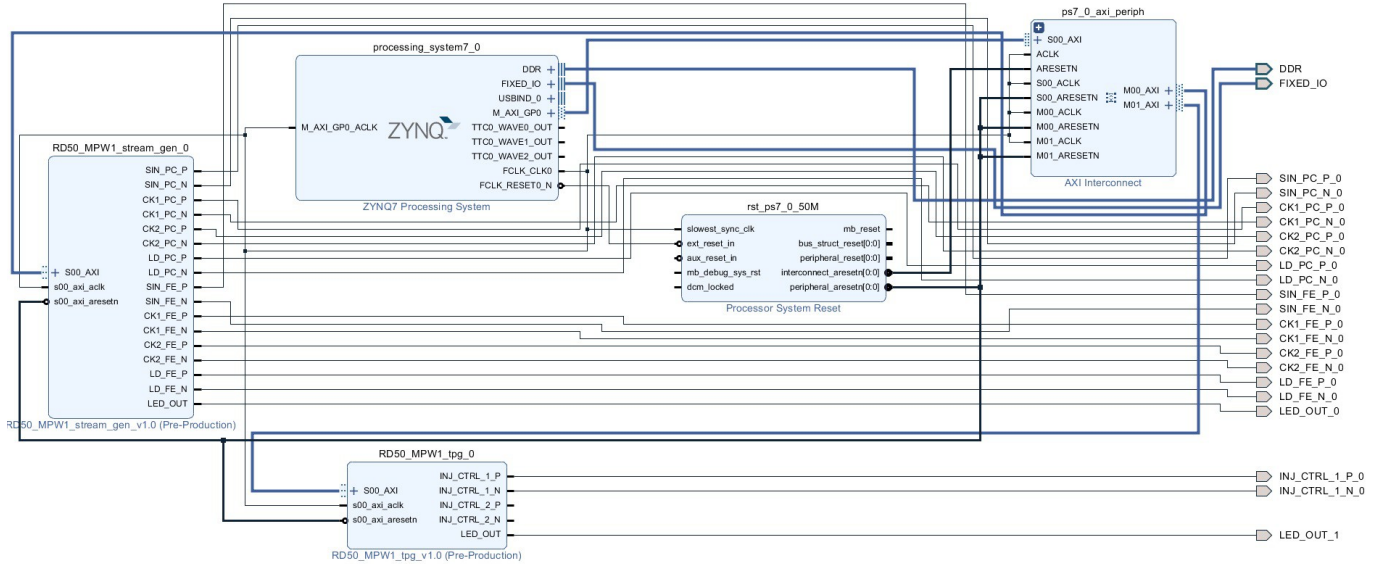
- Specific chip board to accomodate one RD50-MPW2 chip.
- Compatible with the FMC CaR board and the FMC GPI board.
- 100 mm x 80 mm size and 8 layers stack-up.
- It can be used both for MPW2 pixel matrix readout and E-TCT measurements of test structures.
- I2C ADC, I2C thermometer, unique ID and 2k EEPROM.
- PCB layout finished.
- Production and assembly planned during June/July.



RD50-MPW2 chip board (ground and power planes not showed)

DAQ firmware: Zynq SoC hardware

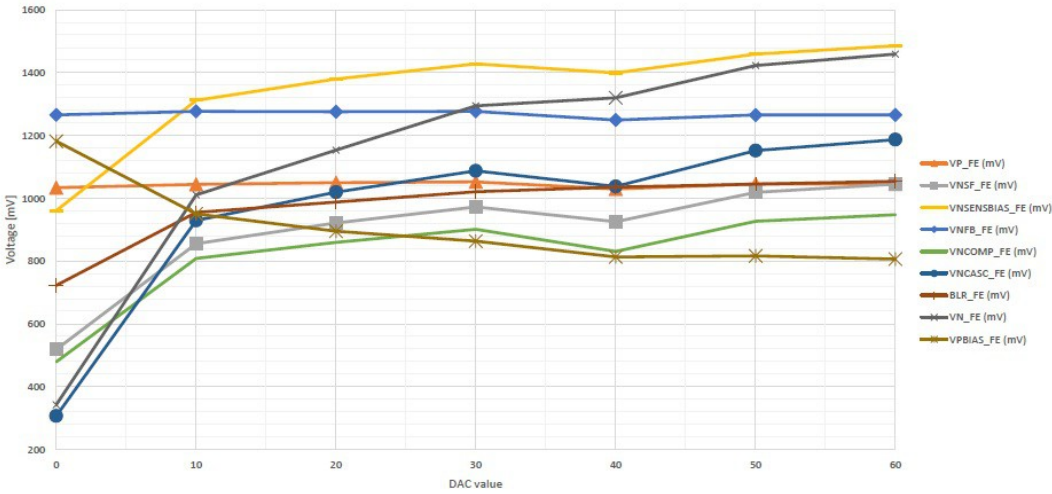
- Specific for each application, detector or device to readout.
- Zynq SoC device block diagram defined for RD50-MPW1.
- Processing System (PS).
  - Two ARM Cortex-A9 CPUs with DDR memory controller.
  - Peripherals: GPIO, I2C0, ENET0, USB0, SD0 and UART1.
- Programmable Logic (PL) with custom IP VHDL blocks using AXI bus slave interfaces.
  - RD50-MPW1 stream generator.
  - RD50-MPW1 test pulse generator.
  - RD50-MPW1 FE-I3 matrix control and readout.



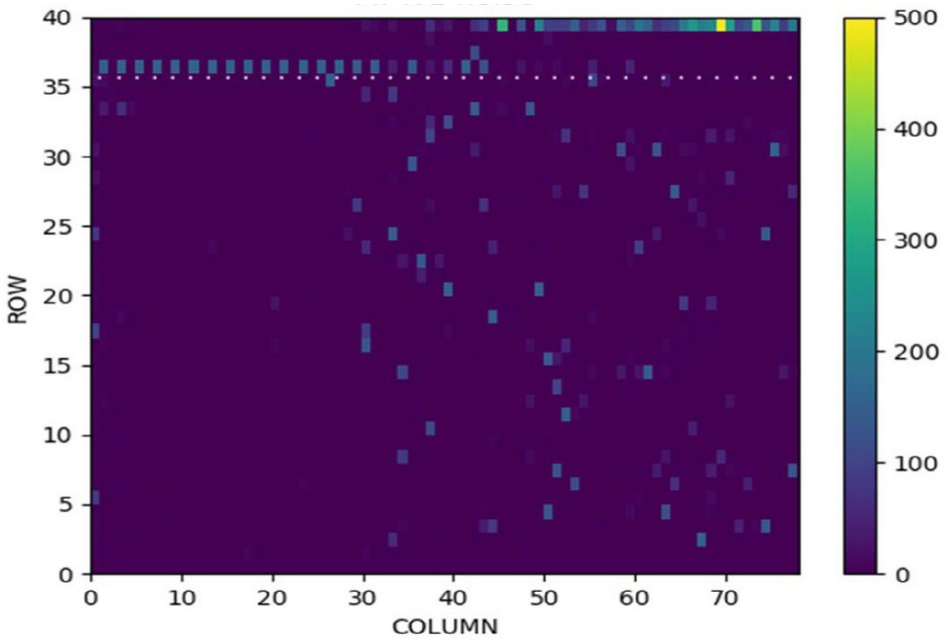
Zynq SoC block diagram for the RD50-MPW1 chip board

DAQ firmware/software: Zynq SoC firmware/software

- The PS of Zynq SoC with custom Linux distribution for the SoC hardware interfacing the RD50-MPW1.
  - Bootloader and root file system in the ZC702/ZC706 SD card (8 GB).
  - Standard i2c driver and i2c-tools package software included to interface the PS I2C0 controller.
  - Standard UIO driver and python interpreter also included to interface the PL custom AXI blocks.
  - SSH used for the communication via ethernet between the host PC and the ZC702/ZC706 development board.
- Collection of python classes, low-level scripts and C programs to perfom RD50-MPW1 configuration and measurement tasks.
  - Files stored in the own root file system.
  - FMC CaR configuration for interfacing the RD50-MPW1 chip.
  - RD50-MPW1 DAC programming.
  - RD50-MPW1 pulse injection.
  - RD50-MPW1 FE-I3 matrix readout.



RD50-MPW1 FE-I3 matrix bias voltages vs. DAC value measurement



Hit map of the RD50-MPW1 FE-I3 matrix

Conclusion and future plans

- DAQ development for RD50 DMAPS devices is progressing.
- We are able to interface the RD50-MPW1 chip to characterize it.
- We are already working in the hardware/firmware/software to interface the RD50-MPW2.
- Still a lot of things to do:
  - Hardware:
    - Production and assembly of the RD50-MPW2 chip board.
    - Finish layout of FMC GPI and FMC Trigger and Communication boards.
  - SoC hardware/firmware/software:
    - RD50-MPW1 PC matrix readout.
    - RD50-MPW2 device interface.
    - FMC Trigger and Communication board functionality for test beams.
  - Host PC control and monitorization common GUI software.

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