UNIVERSITY OF LIVERPOOL

Design work of depleted CMOS sensors within the CERN-RD50 collaboration

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RD50

RD50-MPW1 – Submission

2017 | 2018 | 2019

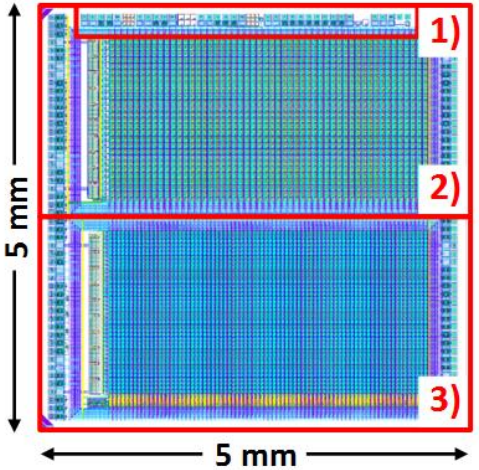
RD50-MPW1 - General design details

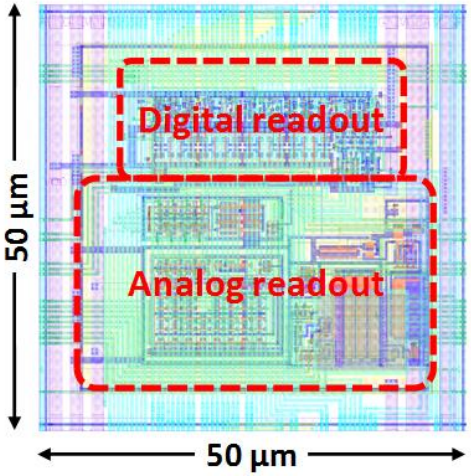
- MPW in the **150 nm HV-CMOS process from LFoundry**
- Submitted in November 2017
- To gain expertise, test the process and test novel designs
- Fabricated using 2 different substrate resistivities
  - ➔ 500 Ω·cm (40 samples) and 1.9k Ω·cm (80 samples)

RD50-MPW1 – Chip contents

1) Tests structures for e-TCT and C_{DET} measurements
2) Matrix of depleted CMOS pixels with 16-bit counter
   - ➔ 26 x 52 pixels
   - ➔ 75 µm x 75 µm pixel area
3) Matrix of depleted CMOS pixels with FE-I3 style readout
   - ➔ 40 x 78 pixels
   - ➔ 50 µm x 50 µm pixel area

- Analog and digital readout embedded in the sensing area
- Completely independent matrices

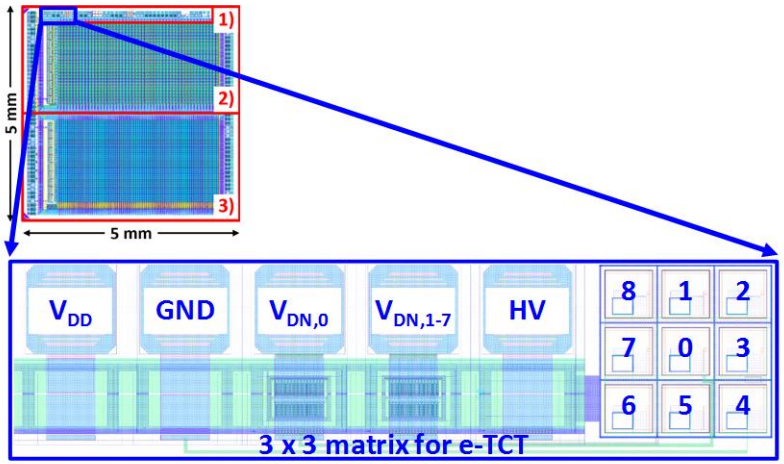


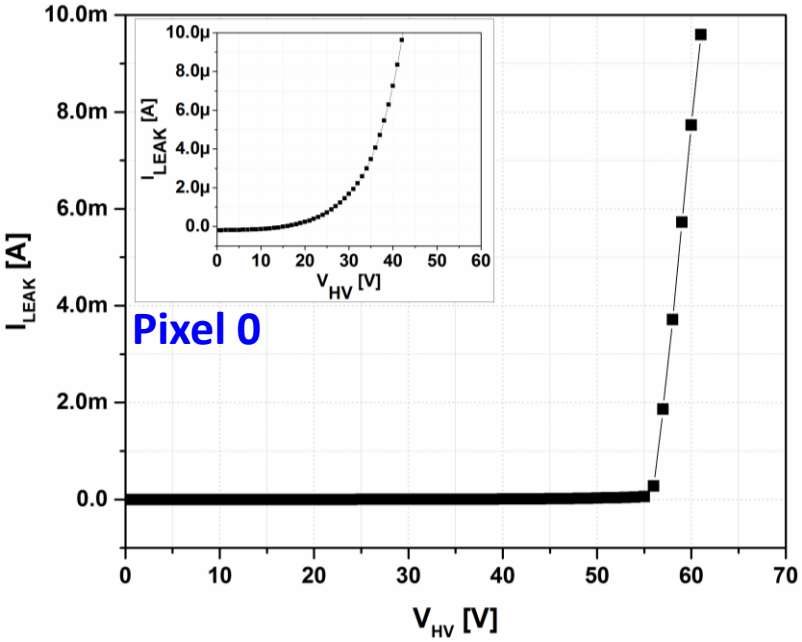


RD50-MPW1 – Measurements

2017 | 2018 | 2019

RD50-MPW1 - Measurements





- Chip received in April 2018
- I-V of central pixel (50 µm x 50 µm)
- Measurement done using a probe station with sensor in complete darkness
- **V_{BD}~55-60 V as expected from design, but I_{LEAK} is too high**
- **This issue has been extensively studied: TCAD + support from the foundry**
- **The chip is functional!** ***See presentations by*** ➔ ***I. Mandic in 33rd RD50 WS (sensors)***
  F. Forster in this RD50 WS (readout)

RD50-MPW2 – Submission

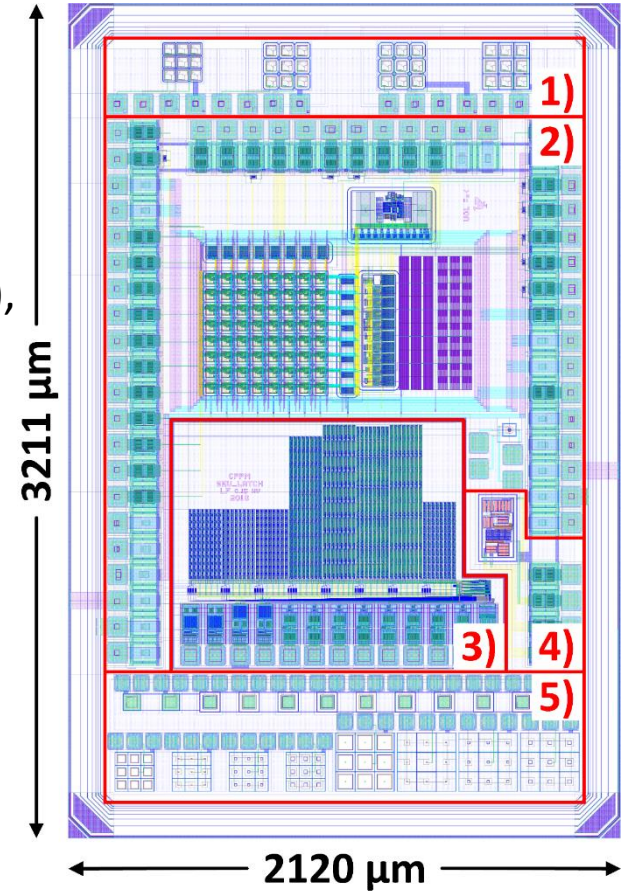
2017 | 2018 | 2019

RD50-MPW2 - General design details

- MPW in the **150 nm HV-CMOS process from LFoundry**
- Submitted in January 2019 (chips expected in July)
- To implement methods to minimize the leakage current
- Fabricated using 4 different substrate resistivities
  - ➔ 10 Ω·cm (80 samples), 100 Ω·cm (80 samples), 1.9k Ω·cm (80 samples) and 3k Ω·cm (80 samples)

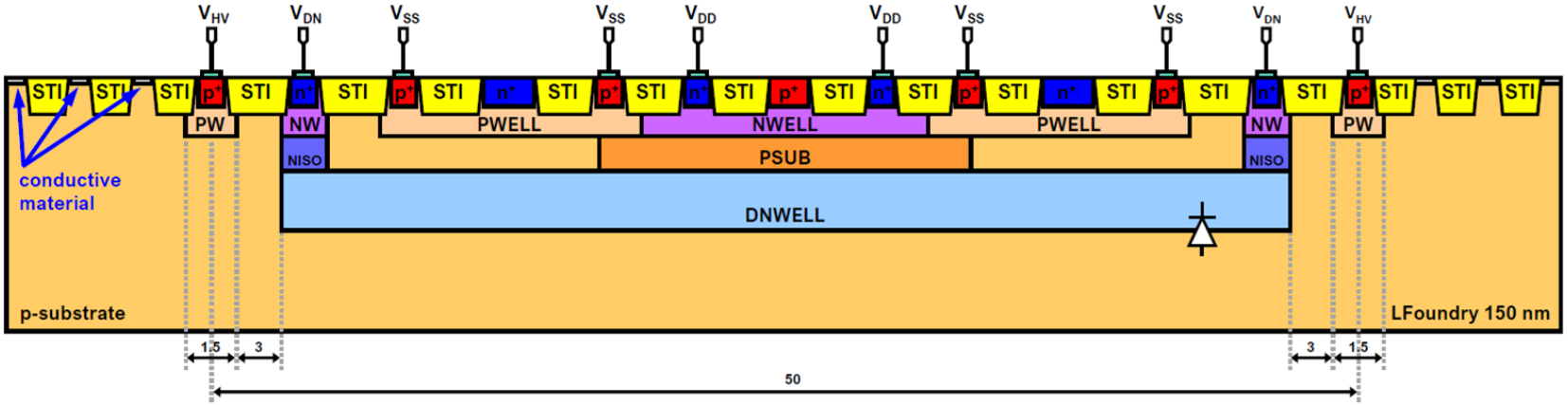
RD50-MPW2 – Chip contents

1) Tests structures with depleted CMOS pixels
2) Matrix of depleted CMOS pixels with analog readout
   - ➔ 8 x 8 pixels
   - ➔ 60 µm x 60 µm pixel area
   - ➔ Analog readout embedded in the sensing area
3) SEU tolerant memory array
4) Bandgap reference voltage
5) Test structures with SPADs and depleted CMOS pixels

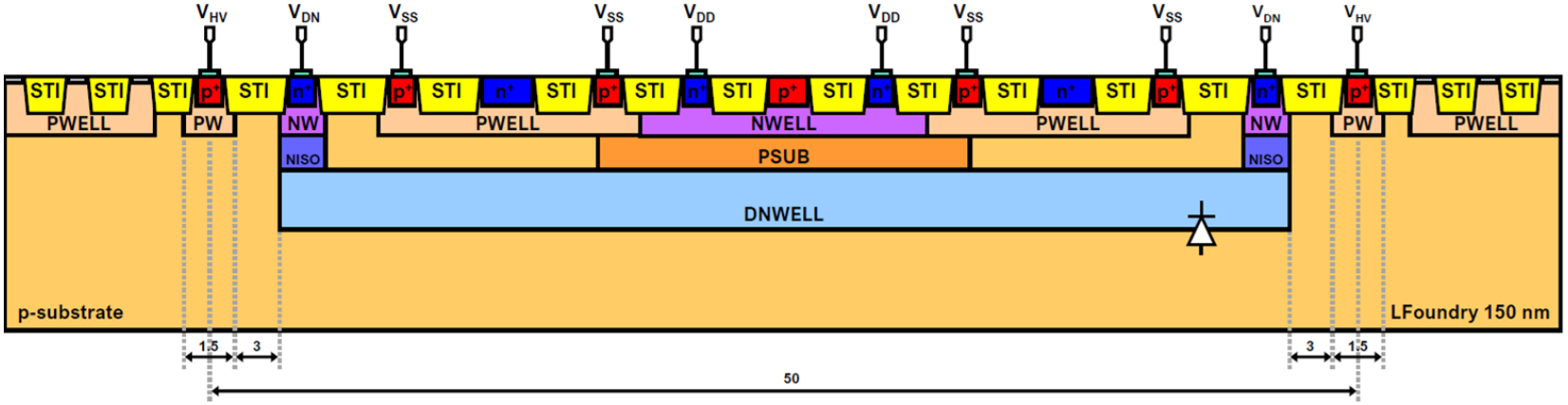


Things we have learnt – Post-processing

- LFoundry adds structures to the design files people submit before starting fabrication.
- LFoundry confirmed this process **involves conductive material**.
- We believe these structures contribute quite significantly to the high I_{LEAK} we measured in RD50-MPW1. They can be **in the pixels**, **peripheral readout electronics**, **I/O pads**, etc.



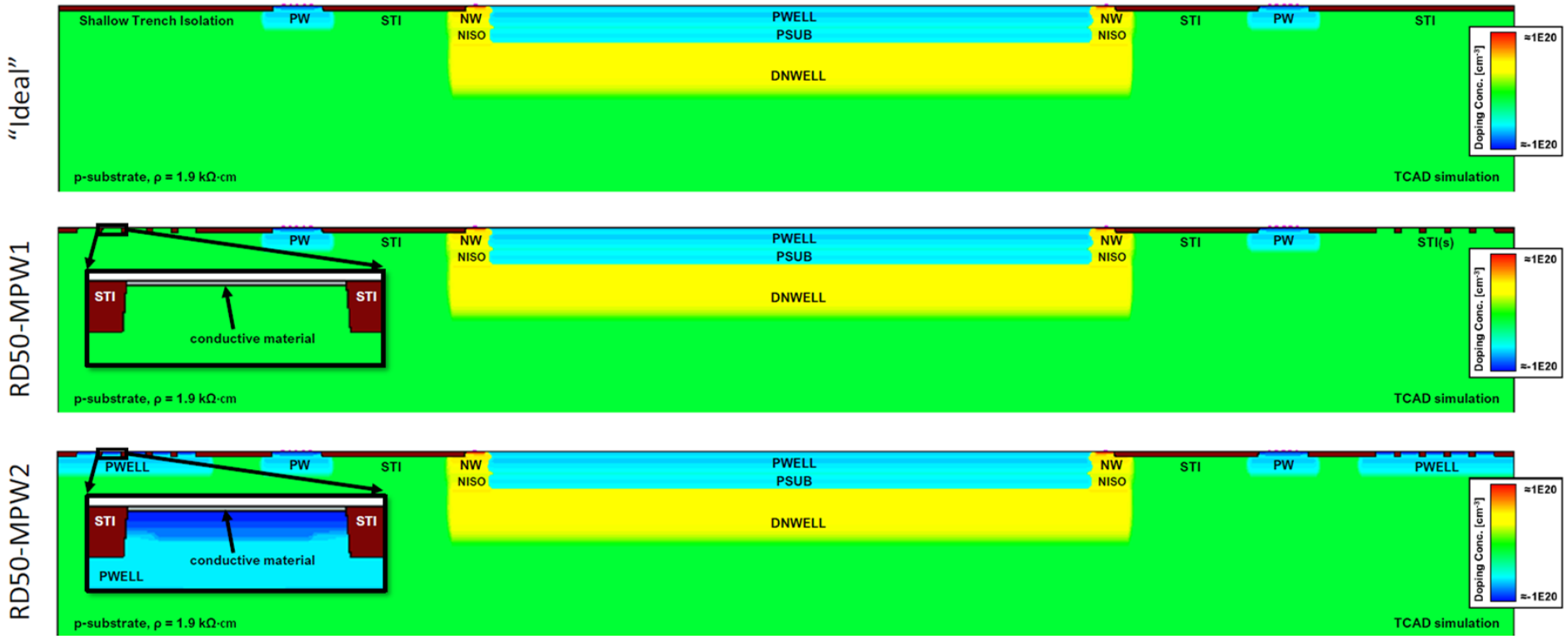
- LFoundry suggested placing the **conductive material in a PWELL** to reduce I_{LEAK}.



TCAD – Post-processing

RD50-MPW1 – Pad diode simulations

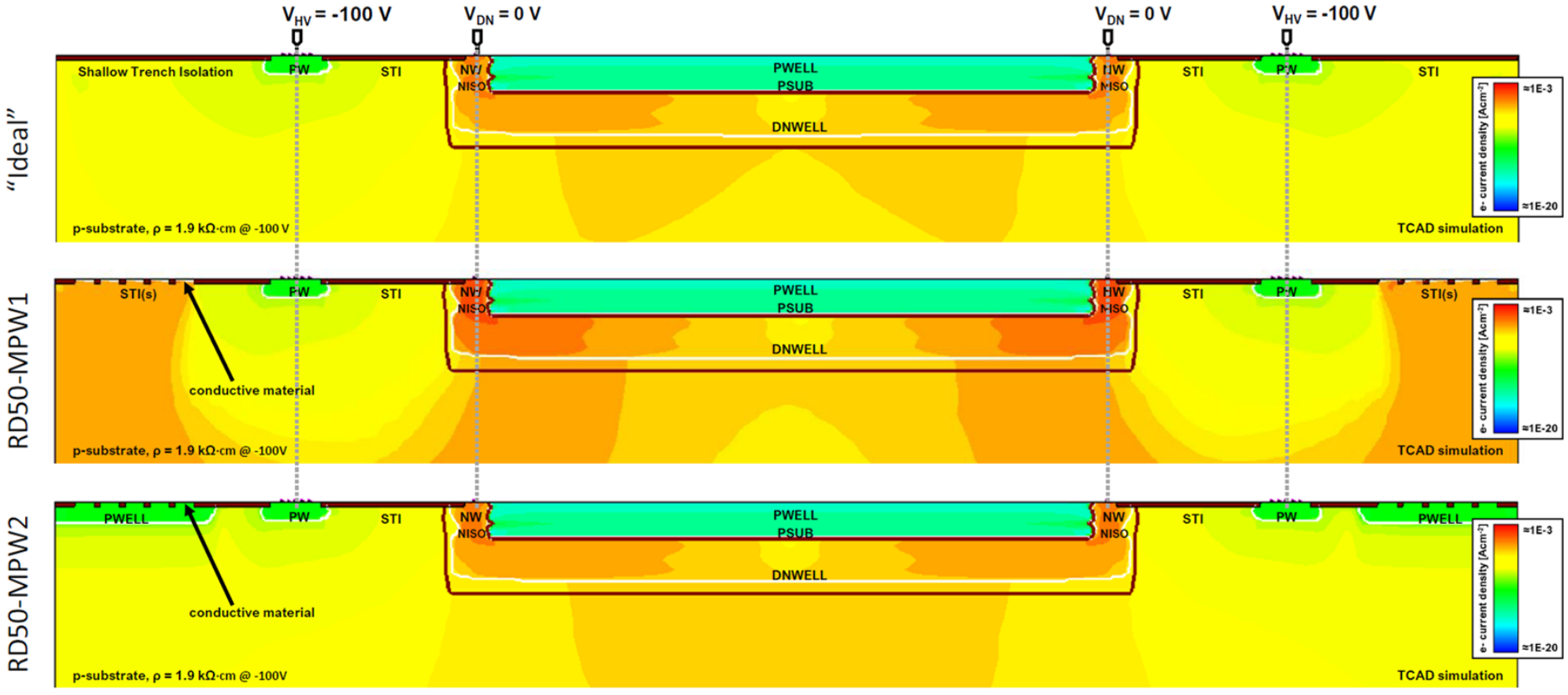
- Doping concentration



TCAD – Post-processing

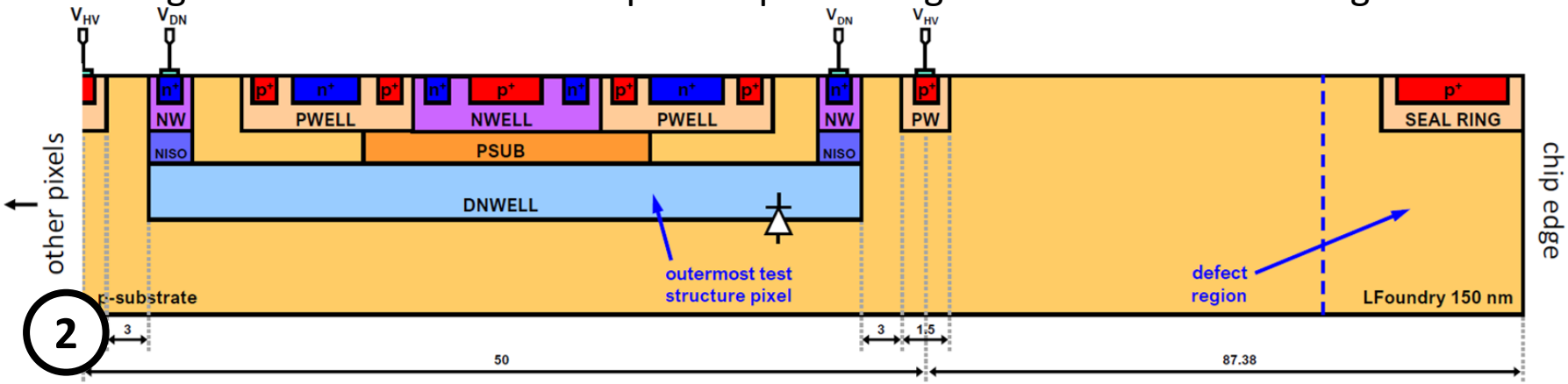
RD50-MPW1 – Pad diode simulations

- Electron current density

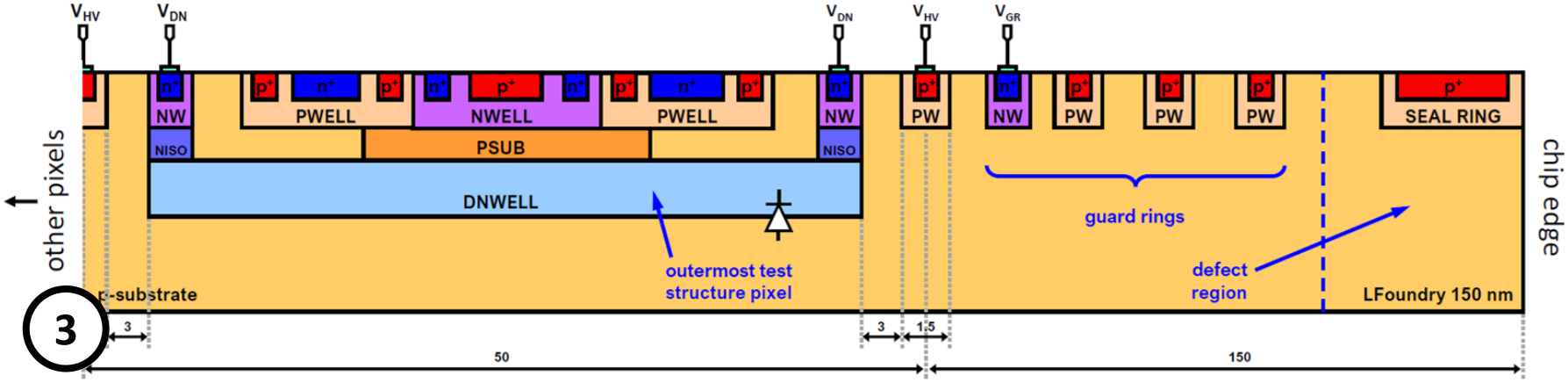


TCAD – Edge defects

- Some pixels can be quite close to the edge of the chip.
- Defects in silicon lattice due to dicing can become significant.
- Leakage current increases when pixel depletion region is near the defect region.



- **N-type guard ring added as safeguard to "collect" leakage current.**
- **P-type guard rings added to reduce "lateral" depletion.**



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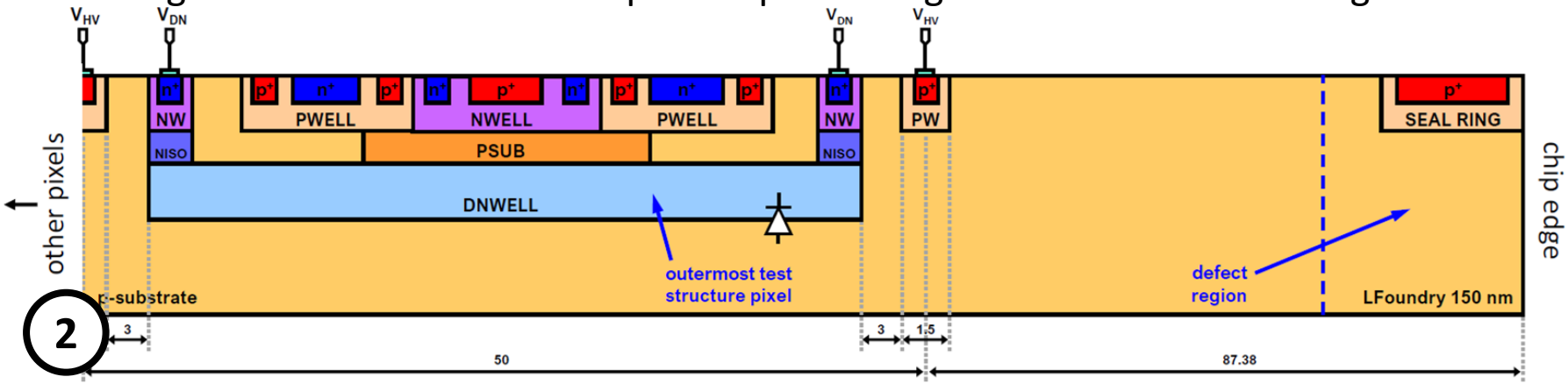
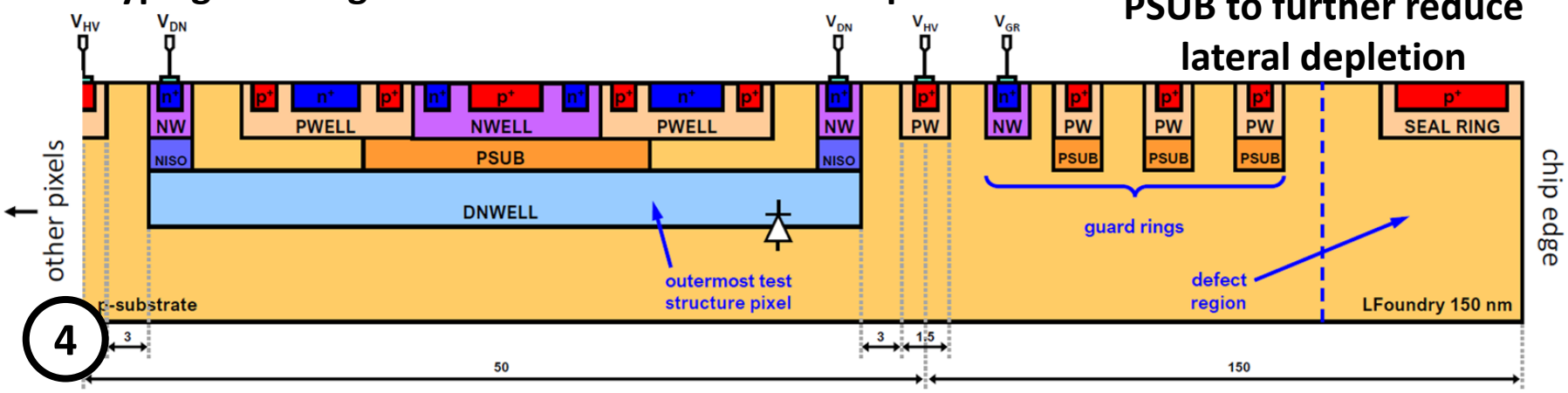
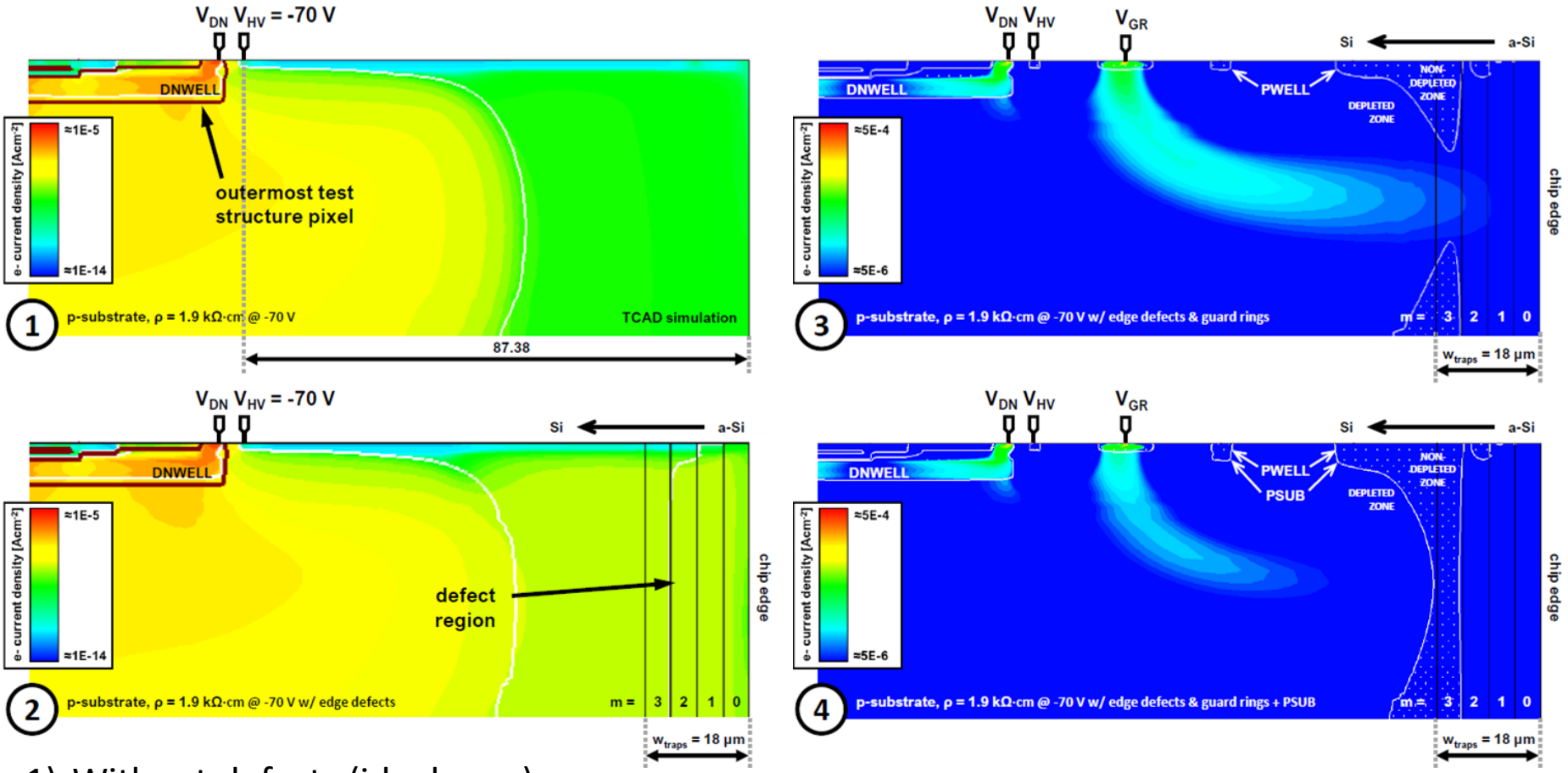


- **N-type guard ring added as safeguard to "collect" leakage current.**
- **P-type guard rings added to reduce "lateral" depletion.**

PSUB to further reduce lateral depletion



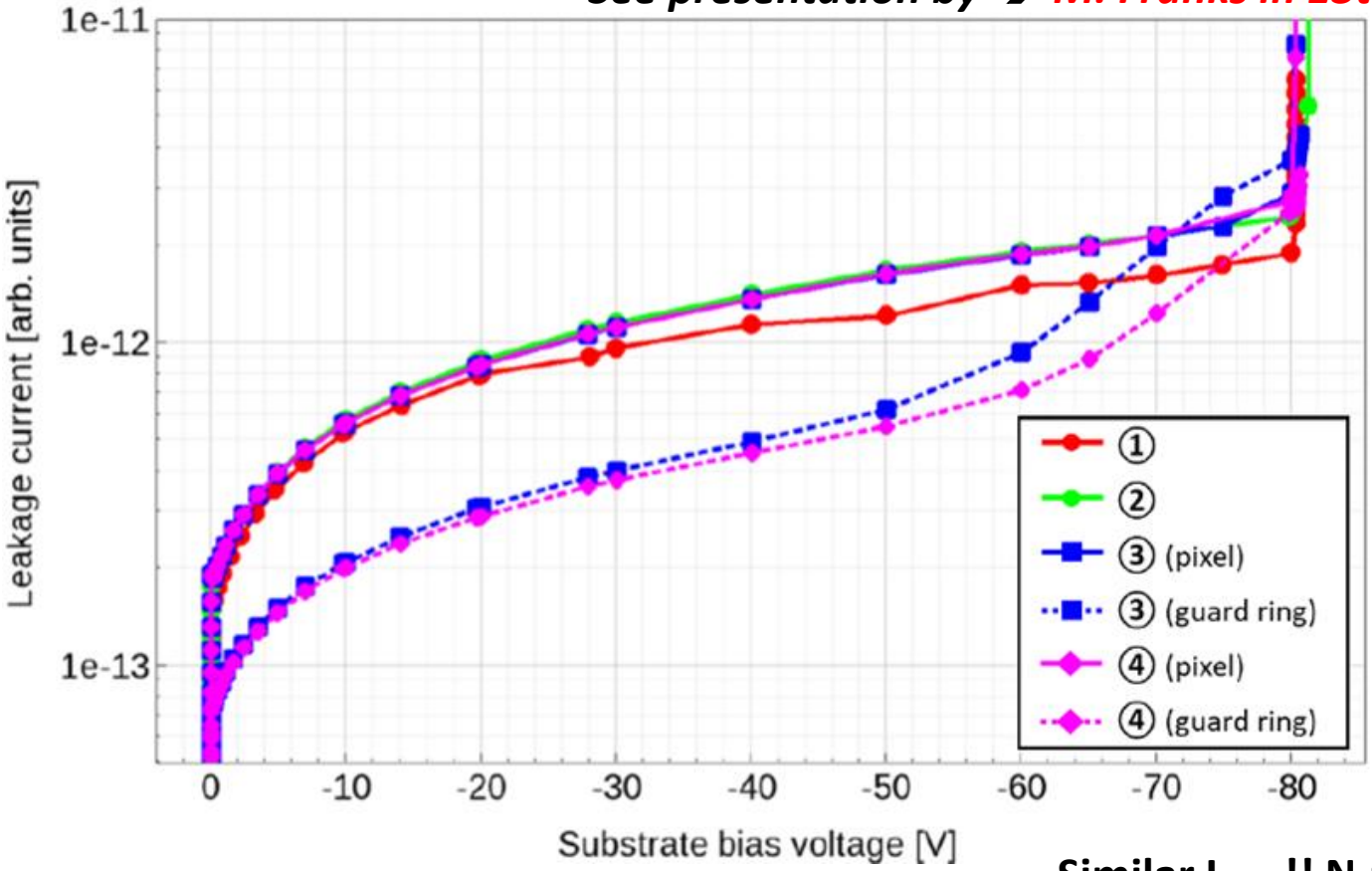
TCAD – Edge defects



1) Without defects (ideal case).
2) With defects and no guard rings.
3) With defects, and NWELL and PWELL guard rings.
4) With defects, and NWELL and PWELL with PSUB guard rings.

TCAD – Edge defects

See presentation by ➔ M. Franks in 13th Trento WS

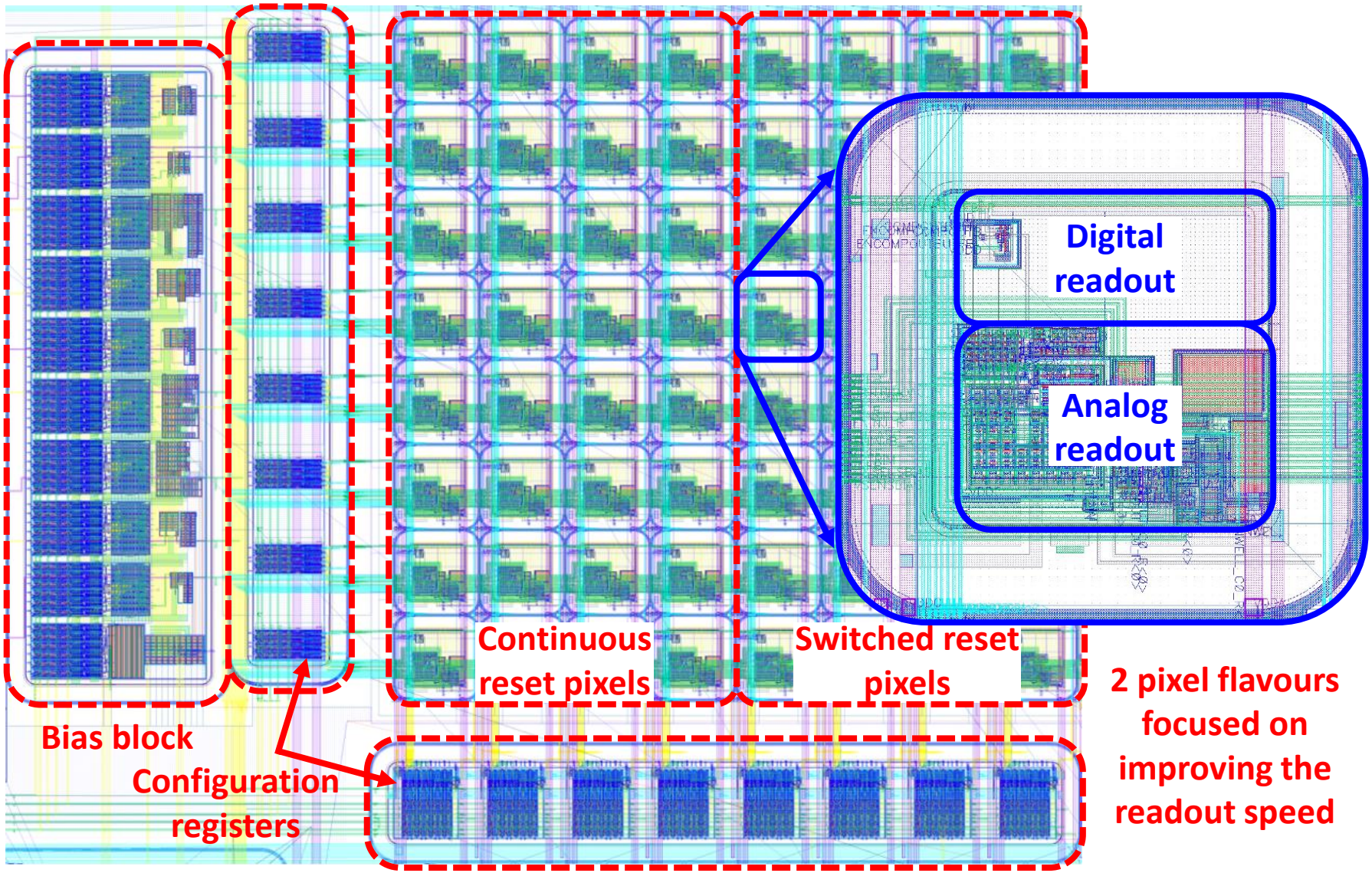


1) Without defects (ideal case).
2) With defects and no guard rings.
3) With defects, and NWELL and PWELL guard rings.
4) With defects, and NWELL and PWELL with PSUB guard rings.

Similar I_{LEAK}!! N-type guard ring acts as a diode increasing lateral depletion into defect region.

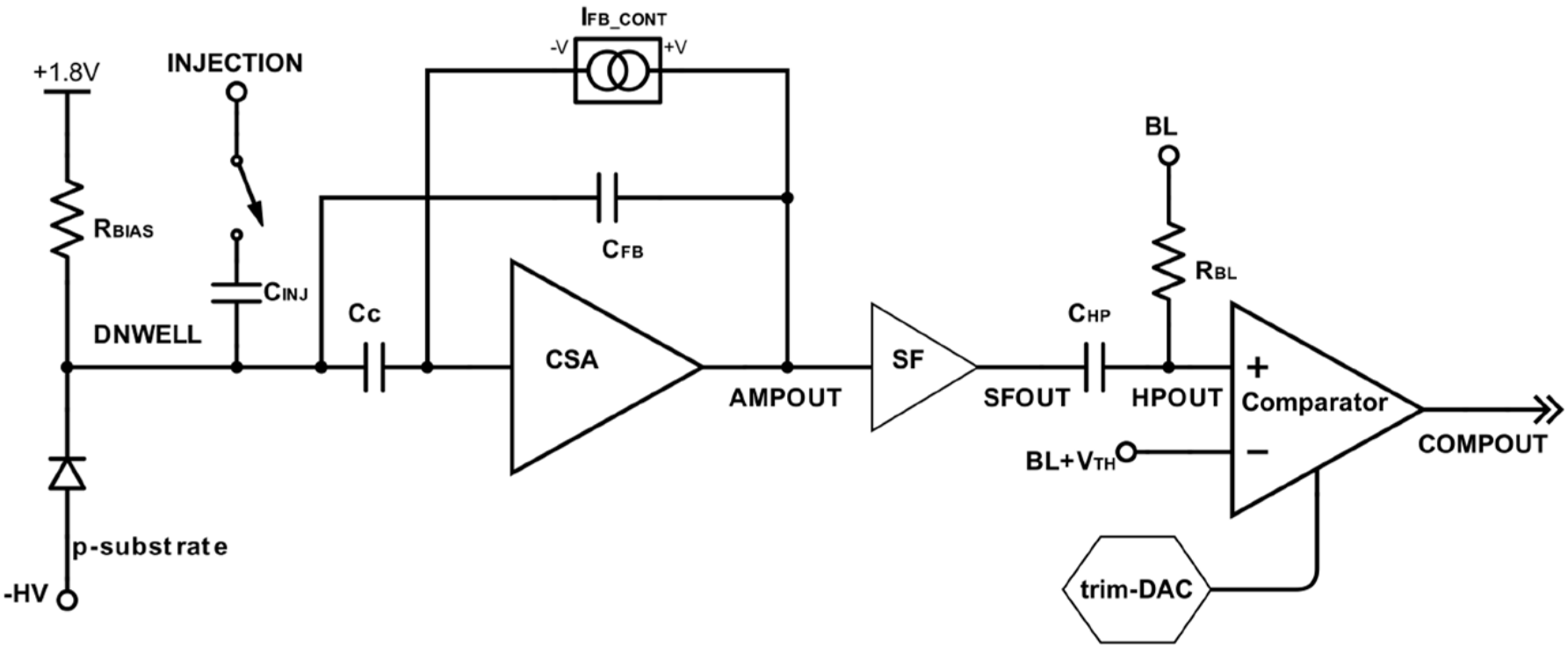
PSUB reduces I_{LEAK} ☺

RD50-MPW2 – Matrix of depleted CMOS pixels



2 pixel flavours focused on improving the readout speed

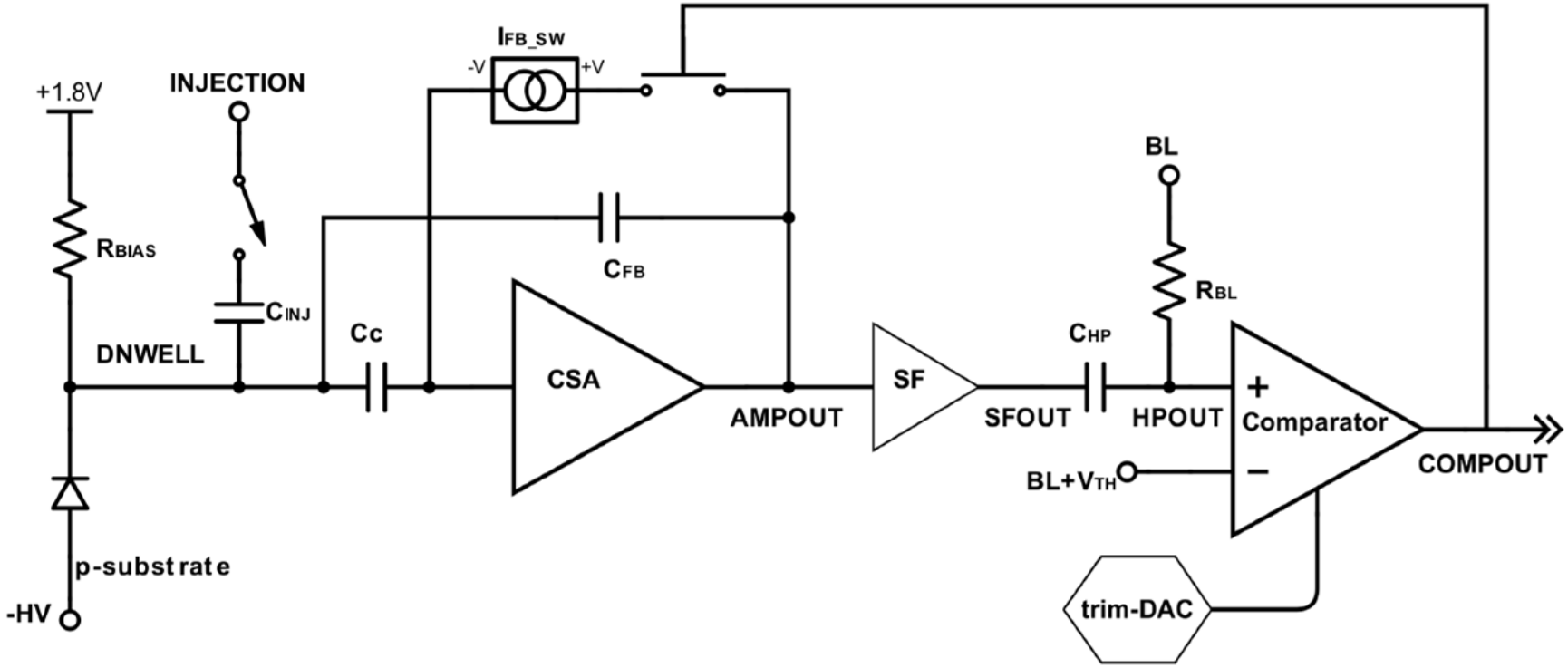
RD50-MPW2 – Continuous reset pixel



Traditional approach - Details

- Shorter rising and falling edges of AMPOUT and SFOUT
- Rising edge → controlled by speed of CSA (transistor capacitances, current)
  very detailed design to minimize transistor capacitances
- Falling edge → controlled by C_{FB} and I_{FB_CONT} **(constant current in this flavour)**
  linear discharge

RD50-MPW2 – Switched reset pixel



Non-traditional approach - Details

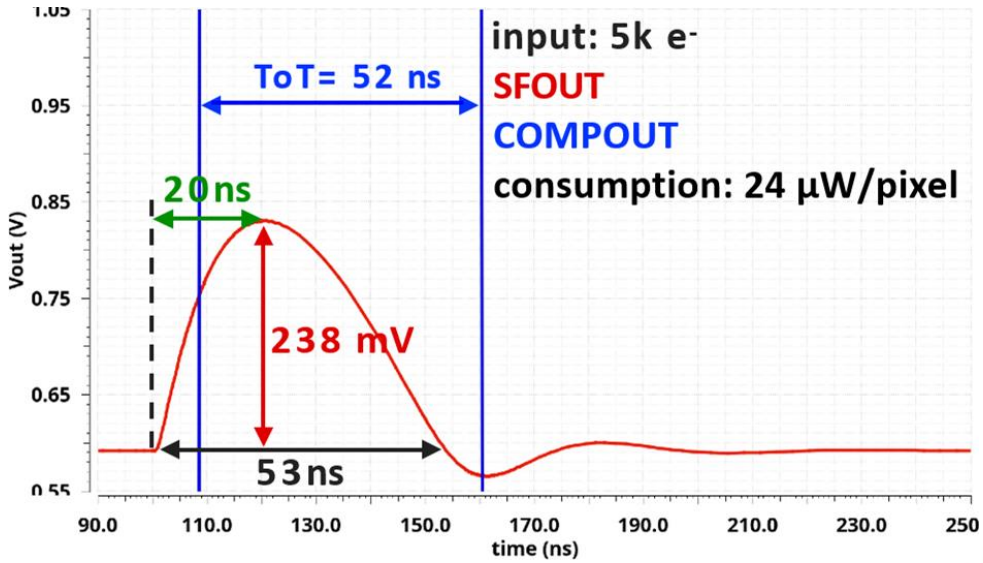
- Shorter readout time
- Rising edge → same as in continuous reset pixel
- Falling edge → controlled by C_{FB} and I_{FB_SW} **(switched current in this flavour)**

  $I_{FB_SW} = I_{FB_CONT}$ + additional current when there is an event

  additional current controlled by COMPOUT (it closes the switch)

  the additional current resets the pixel immediately (non-linear)

RD50-MPW2 – Matrix of depleted CMOS pixels

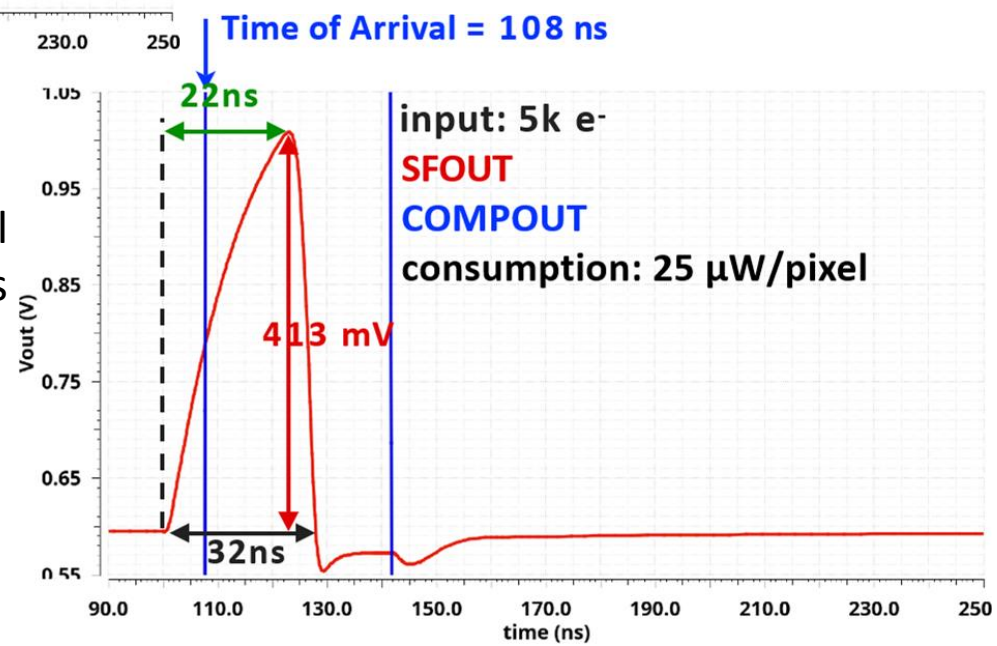


→ **Continuous reset pixel**

- Linear discharge
- Fall time is proportional to the number of electrons collected by the sensor

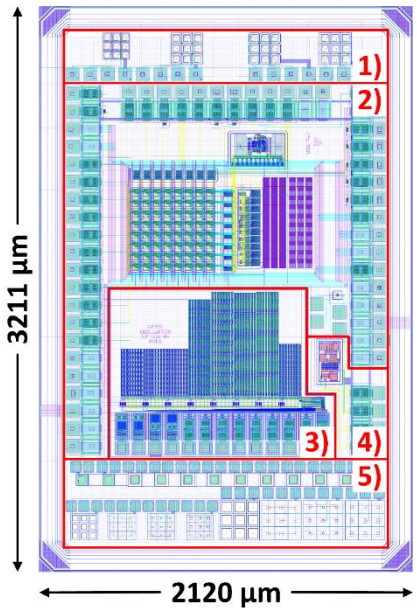
→ **Switched reset pixel**

- Non-linear discharge
- Fall time is NOT proportional to the number of electrons collected by the sensor



See presentation by → C. Zhang in 13th Trento WS

RD50-MPW2 – SEU tolerant memory array



To study the SEU tolerance of several memory cells by comparing them to the standard cell. The array has 8 different flavours:

3.1) Standard cell from the LFoundry library (latch cell)
- It uses 8 transistors

3.2) DICE cell (Dual Interlocked Storage Cell, full custom)
- Special cell based on 2 cross-coupled inverters
- It uses 12 transistors
- Immunity against SEUs (non-simultaneous)

3.3) Enhanced DICE cell (full custom)
- DICE cell with larger spacing between sensitive nodes
- Immunity against simultaneous SEUs

3.4) Standard cell with TRL (Triple Redundancy Logic)
- With feedback correction driven by error detection

3.5) DICE cell (full custom) with TRL

3.6) Standard cell with TRL and split latch
- TRL split between 2 bits to separate sensitive nodes further

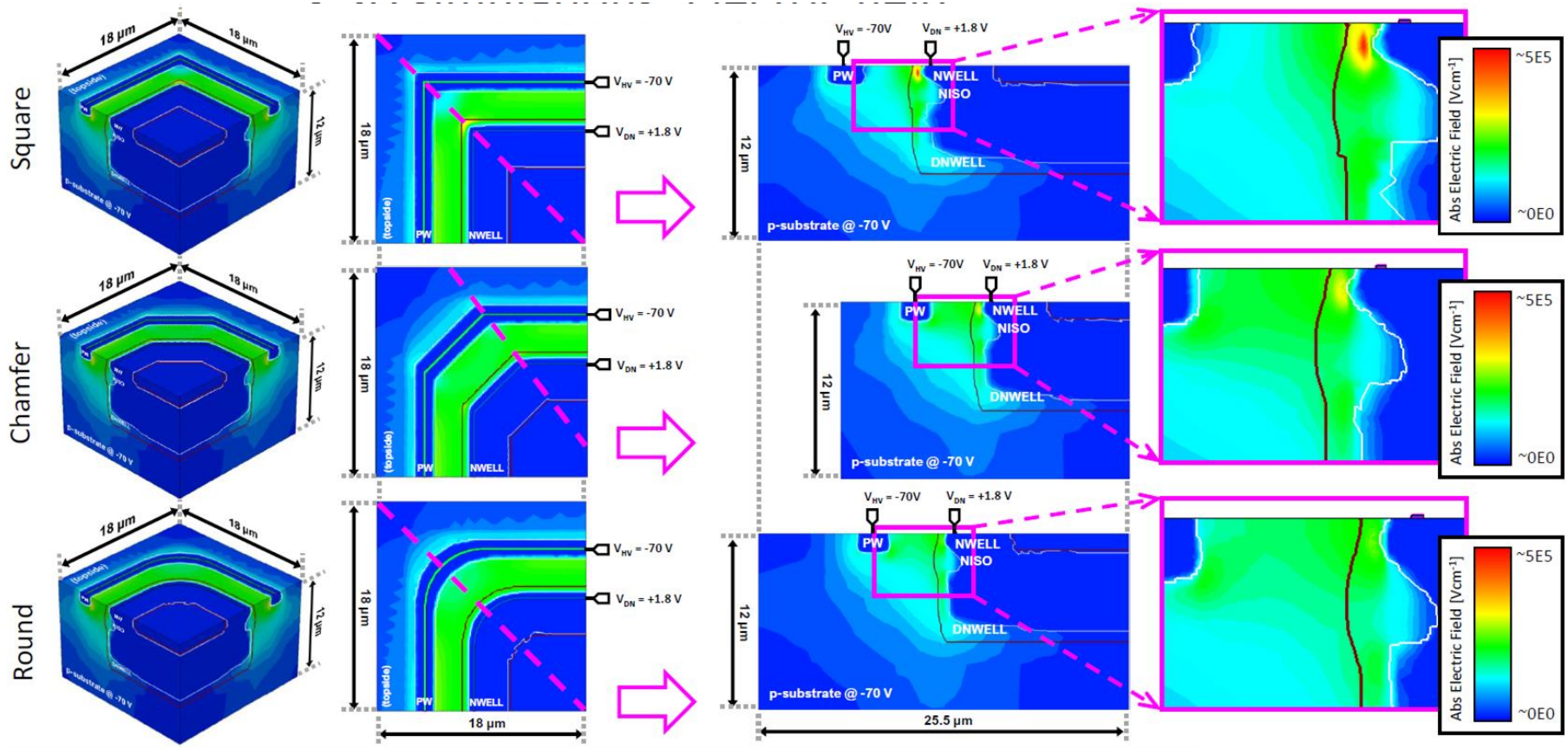
3.7) DICE cell (full custom) with TRL and split latch

3.8) SRAM cell
- It uses 6 transistors

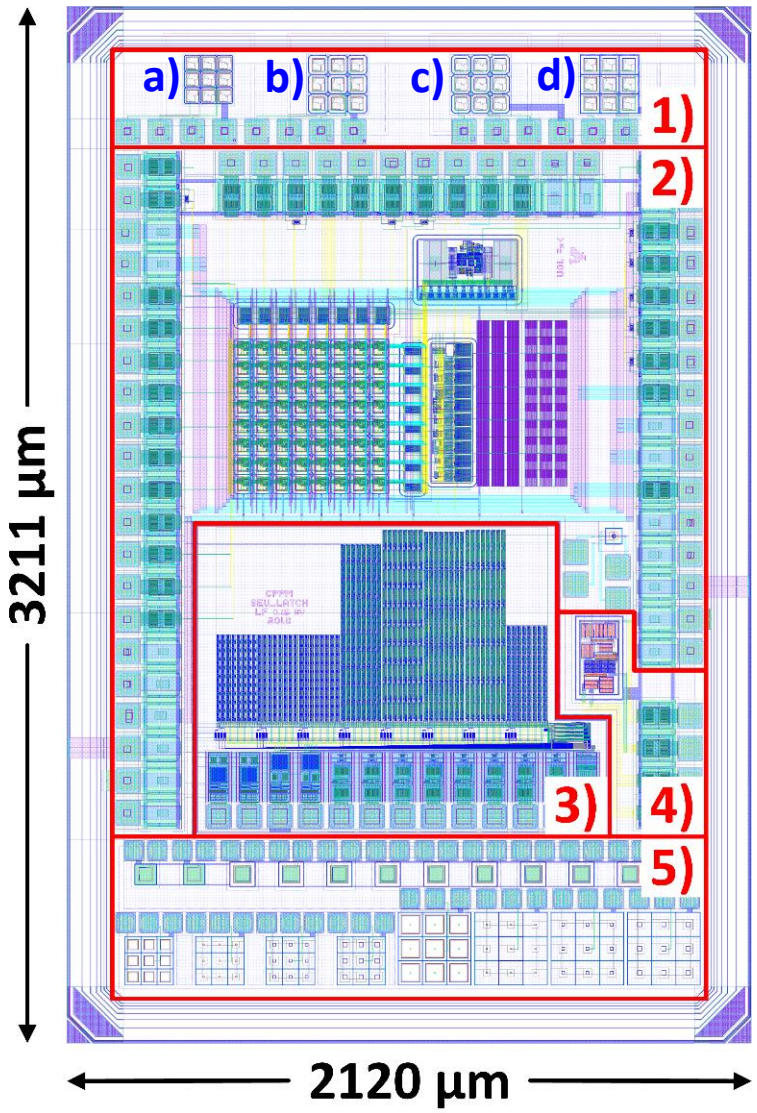
The memory array will be tested in sites like Leuven, Jyväskylä and Groningen.

RD50-MPW2 – Test structures 1)

3D simulations – Electric field as a function of corner geometry in pixel



RD50-MPW2 – Test structures 1)



Matrices of 3 x 3 depleted CMOS pixels

- For I-V and e-TCT measurements
- Very similar to other test structures used in the past
- 8 external pixels are shorted together
- I/O pads for central and external pixels
- No electronics in the pixels
- No electronics in the I/O pads

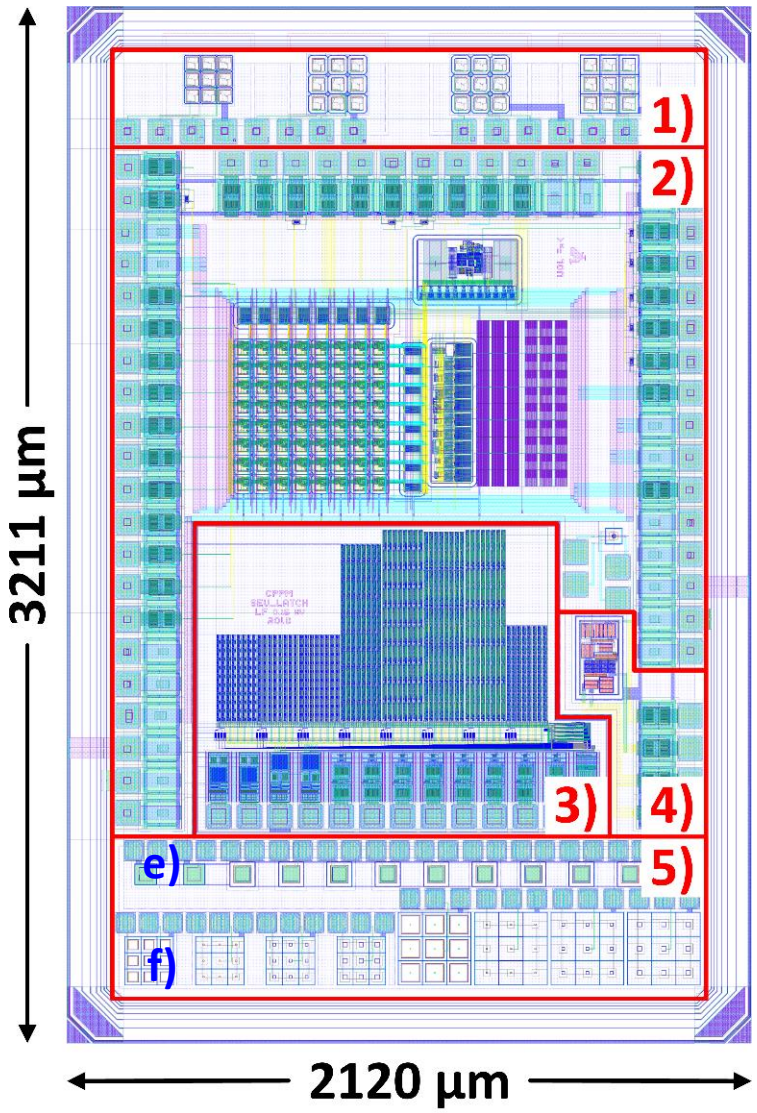
a) Pixel size → 50 µm x 50 µm
P-substrate/deep n-well spacing → 3 µm
Corners → rounded

b) Pixel size → 60 µm x 60 µm
P-substrate/deep n-well spacing → 8 µm
Corners → rounded

c) Pixel size → 60 µm x 60 µm
P-substrate/deep n-well spacing → 8 µm
Corners → chamfered

d) Pixel size → 60 µm x 60 µm
P-substrate/deep n-well spacing → 8 µm
Corners → squared

RD50-MPW2 – Test structures 5)

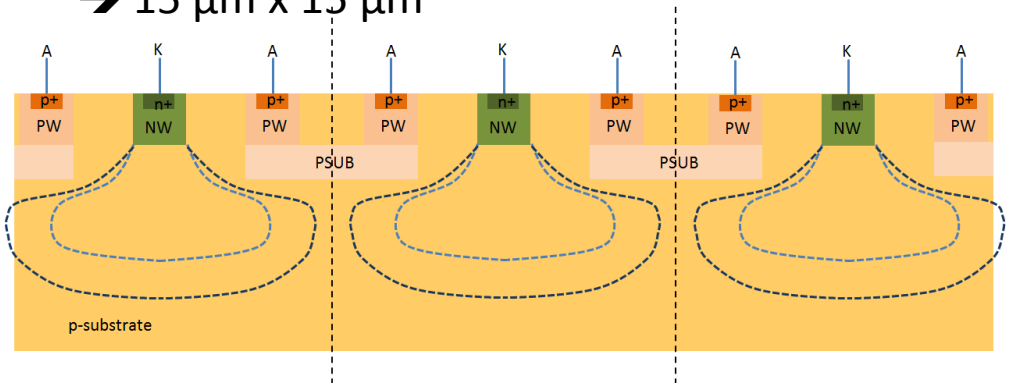


e) SPADs

- 12 single diodes
- Different cross-sections
- *Problematic* layers have been prevented

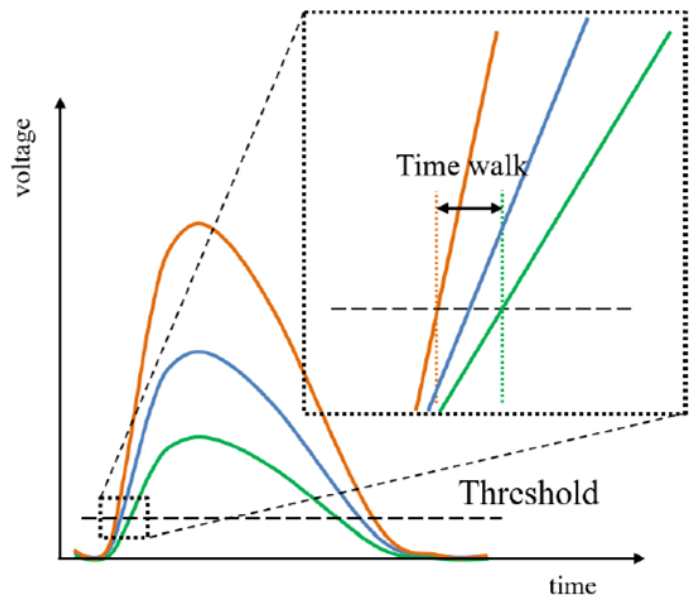
f) Matrices of 3 x 3 depleted CMOS pixels

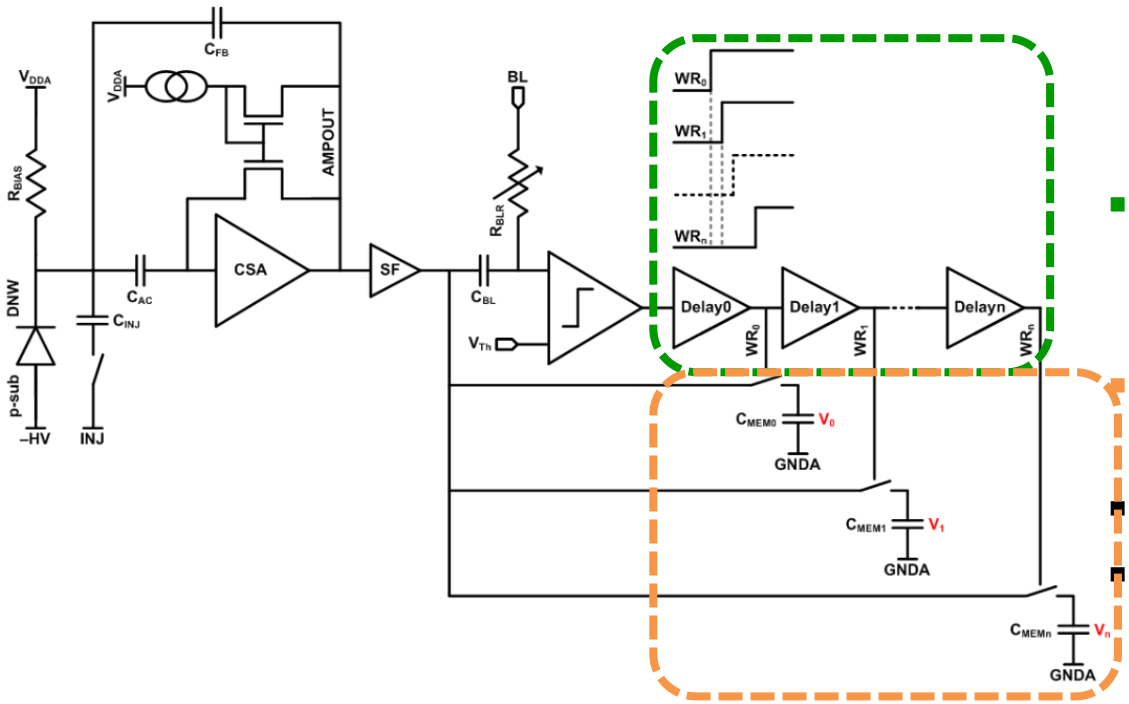
- To compare large and small FF pixels
- Large and small FF pixels with different size:
  - ➔ 50 µm x 50 µm
  - ➔ 75 µm x 75 µm
- To study the depletion region as a function of the collecting electrode size:
  - ➔ 5 µm x 5 µm
  - ➔ 10 µm x 10 µm
  - ➔ 15 µm x 15 µm



New pixel flavour – Sampling pixel

- Aim → Minimize the time-walk.
- Time-walk → Time difference in the detection of hits that generate smaller or larger signals.
- A few methods for on-chip time-walk correction for depleted CMOS sensors (compensated comparator, 2-thresholds, etc.).
- Best result so far found in the literature is ~6 ns.
- **Schematic of sampling pixel:**

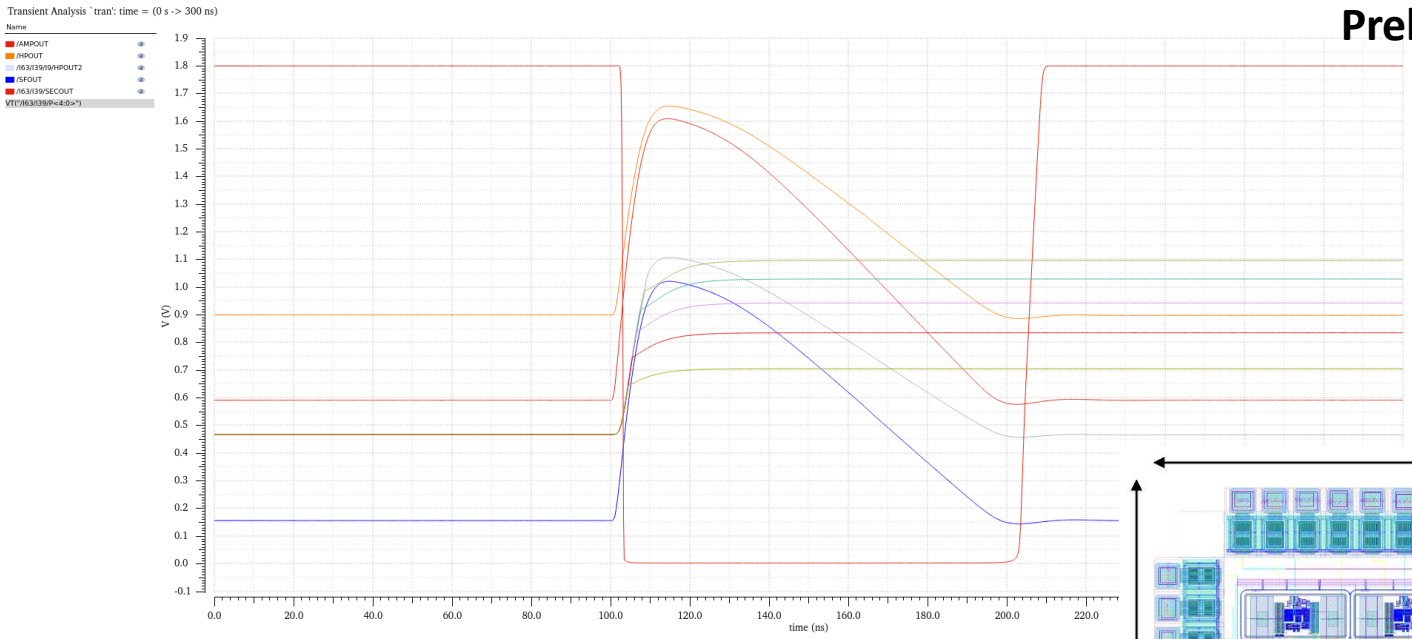


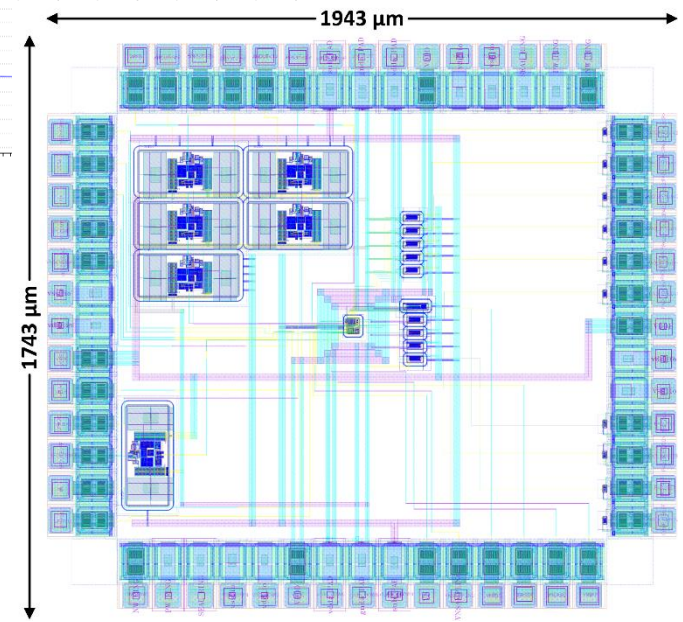


- Programmable chain delay to sample a few points of SF signal (i.e. 5)
- Analog memories to store the voltage values
- Off-chip ADCs
- Off-chip processing to determine t_0 (time of event)

New pixel flavour – Sampling pixel

Preliminary simulation and layout





- Best achieved time resolution with the sampling pixel is ~2 ns.
- Proof-of-concept pixel being submitted this month as part of a chip for other things.

See presentation by ➔ O. Alonso in 2018 LCWS

Conclusion

- Measurements of RD50-MPW1 have revealed some unexpected results
  - Too high leakage current
- This has motivated the need for further studies
  - **TCAD simulations**
  - **Conversations with the foundry**
  - **Design and submission of RD50-MPW2**
- RD50-MPW2 includes
  - Methods to minimize the leakage current by adding PWELLs/preventing the generation of certain filling layers plus guard rings around the device
  - Several circuits that include these methods
  - A matrix of depleted CMOS pixels that also improves the readout speed
- Fabricated chip is expected in late July 2019
- We are preparing the DAQ *(see presentations by ➔ R. Marco-Hernandez in this RD50 WS)*
- We are about to submit a **proof-of-concept sampling pixel** to improve the time-walk

Thank you for your attention !