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Design work of depleted CMOS sensors within the CERN-RD50 collaboration

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This contribution describes design work within the CERN-RD50 collaboration to develop depleted CMOS sensors in the 150 nm HV-CMOS (High Voltage-CMOS) process from LFoundry. In particular, we will present the design details of a test chip, named RD50-MPW2, which was submitted for fabrication in January 2019. We will also present the design towards a new pixel flavour, known as a sampling pixel, to improve the time resolution of depleted CMOS pixels and which will be included in the large area submission RD50-ENGRUN1 planned by the collaboration.

The main objective of the RD50-MPW2 submission is to implement new methodologies and test their efficiency in minimizing the large leakage currents measured in the previous test chip developed by the collaboration. Two different design methodologies have been implemented. The first one blocks the generation of certain filling layers added by the foundry during the post-processing stage, while the second one includes a series of guard rings around the design to prevent the sensor depletion region from coming into contact with the edge of the chip. Both have been extensively simulated with TCAD.

RD50-MPW2 also includes a small matrix of depleted CMOS pixels with analog readout electronics embedded in the sensing area of the pixels, a bandgap reference circuit, an SEU (Single Event Upset) tolerant memory array and several test structures with depleted CMOS pixels for e-TCT (edge-Transient Current Technique) measurements and with avalanche photodiodes. A small leakage current is expected from these circuits as a result of the new design methodologies implemented in the chip. In addition, the matrix of depleted CMOS pixels includes two different flavours of readout electronics focused on improving the readout speed of the sensor. RD50-MPW2, which is being manufactured on 10, 100, 1.9k and 3k Ω·cm resistivity substrates, is expected to be back from the foundry during the summer of 2019.

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