OpenMP to FPGA Offloading Prototype Using the Intel FPGA SDK for OpenCL

An IXPUG Success Story

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orka

High Performance Computing

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Introduction

IXPUG Annual Fall Conference 2018

- Presented plan for OpenMP to FPGA offloading
- Asked for feedback

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PyGA: a Python to FPGA compiler prototype

- Python to FPGA offloading
- Using Intel FPGA SDK for OpenCL

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High-level synthesis (HLS) opens FPGA world to Software Developers

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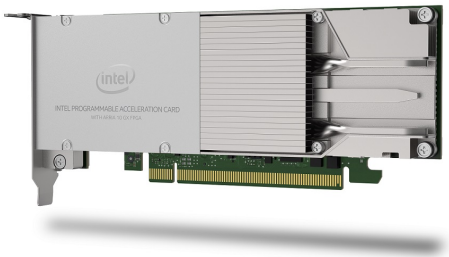
OpenMP

- Used in many legacy code bases
- Version 4 introduced `target` pragma

Agenda

- OpenCL SDK
- Implementation
  - Code Generation for the FPGA Target
  - Code Generation for the Host
  - Current Limitations
- Evaluation of the Prototype
- Future work



OpenCL SDK

OpenMP `target` Offloading Vision

In a perfect world ...

```
// ...

int A[n][m], B[m][p], C[n][p];

// ...

#pragma omp target map(to: A, B) map(from: C)
for (int i = 0; i < n; i++)
    for (int j = 0; j < p; j++)
    {
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        for (int k = 0; k < m; k++)
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Problem

- IR not (officially) supported as an input to the HLS Tools

Advantages of Using the OpenCL SDK

	Intel		Xilinx	
	HLS	OpenCL	OpenCL	HLS
LLVM based	X	X	X	X

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- Across both big vendors (Intel & Xilinx)
- Implementation for Intel PAC
- Should be possible with Xilinx SDAccel as well

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LLVM based	X	X	X	X
Standard API		X	X	
Transfer & Low Level Platform	X	X	X	

Standard API

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- Implementation for Intel PAC
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Low Level Platform

- Provided by the vendor tools
- Handy for a first prototype
- Might limit optimizations later on

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No official support for IR as input to HLS

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Problems

- *clang* OpenMP `target` offloading
  - Starting LLVM 3.8
- Requires mixed version approach
  - Adjust outlined function from up to date LLVM IR to old IR
  - Could become obsolete with newer versions (or standardized IR like SPIR-V)

Runtime Tracing Results (Intel)

```
aocl-clang -cc1 -O3 -emit-llvm-bc -Wuninitialized -triple fpga64 -mllvm -board
        -mllvm $AOCL_BOARD_PACKAGE_ROOT/hardware/pac_a10/board_spec.xml
        -DACL_BOARD_pac_a10=1 -DAOCL_BOARD_pac_a10=1 "$name.cl"
        -o "$name.pre.bc" -g

aocl-link "$name.pre.bc" $ALTERAOCLSDKROOT/share/lib/acl/acl_early.bc -o "$name.1.bc"

aocl-opt --acle $acle_key -board $board_spec -dbg-info-enabled --grif
    --soft-elementary-math=false --fas=false --wiicm-disable=true "$name.1.bc"
    -o "$name.kwgid.bc"
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    --fas=false --wiicm-disable=true "$name.kwgid.bc" -o "$name.lowered.bc"

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aocl-opt -board $board_spec -always-inline -add-inline-tag -instcombine -adjust-sizes -dce
    -stripnk -rename-basic-blocks -dbg-info-enabled --grif --soft-elementary-math=false
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aocl-llc -march=griffin -board $board_spec -dbg-info-enabled "$name.bc" -o "$name.v"

system_integrator --bsp-flow green_top $board_spec $name.bc.xml system.tcl kernel_system.tcl
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# TODO: Modify IR here

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Implementation

Rough Implementation Idea

1. Use *clang* to outline OpenMP `target` pragma
   - Misuse *x86-64* OpenMP target
   - Results in *pure* IR of outlined function

```
; ...

define dso_local i32 @main() #0
{
    ; ...
}

define internal void @__omp_offloading_main_t1(i64) #0
{
    ; ...

    ret void
}

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3. Host related
   - Replace outlined function body by OpenCL API calls

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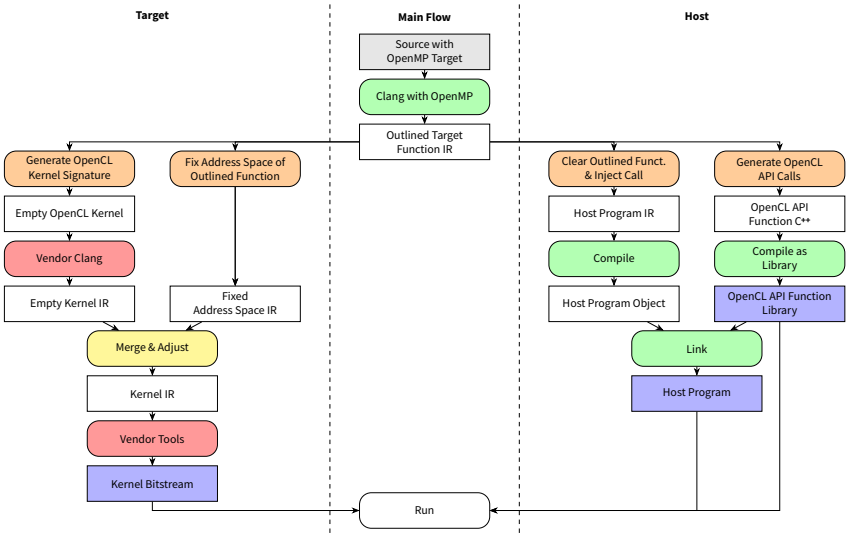
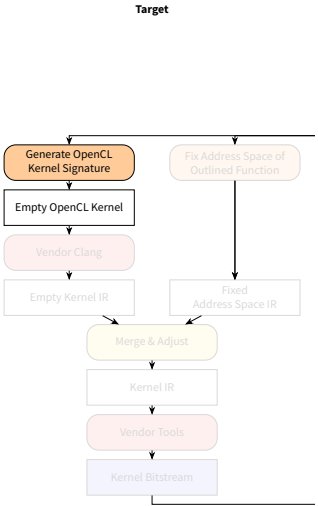
Flowchart of tool invocation



Code Generation for the FPGA Target

Target side

1. Generate *empty* OpenCL kernel source code from signature[1]
   - By LLVM pass



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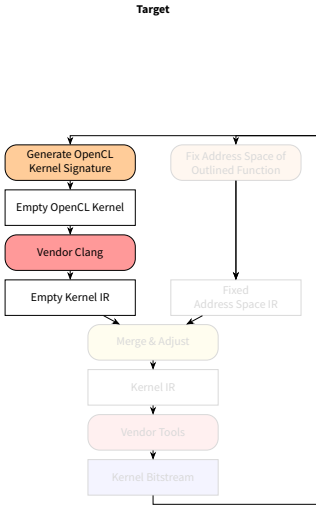

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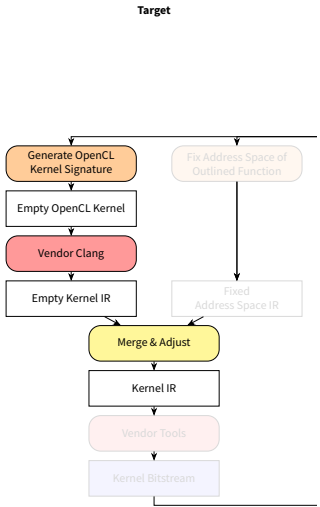

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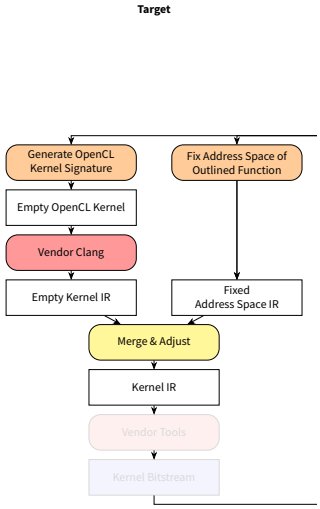

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     - loop unrolling annotations
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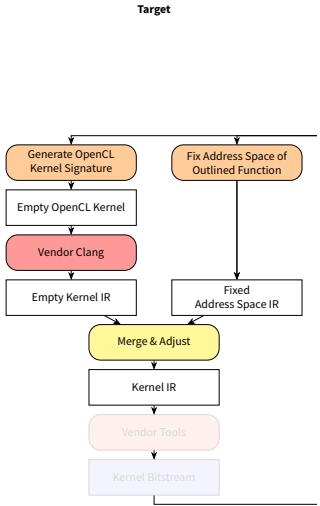

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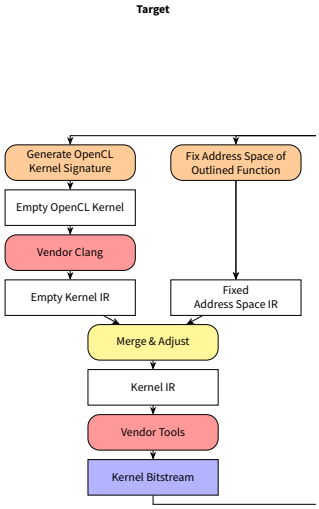
4. Use Vendor tools for HLS



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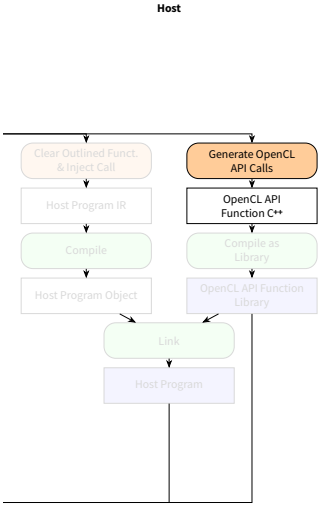
Code Generation for the Host

Host side



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   - Based on the arguments
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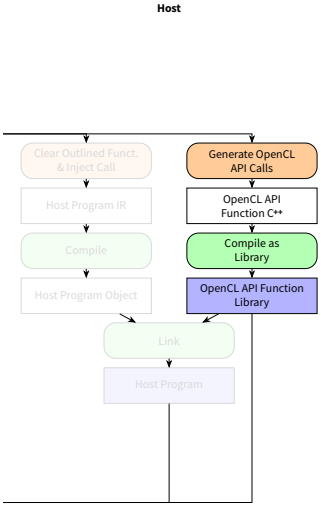

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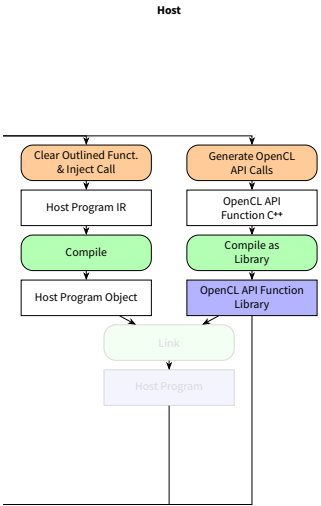

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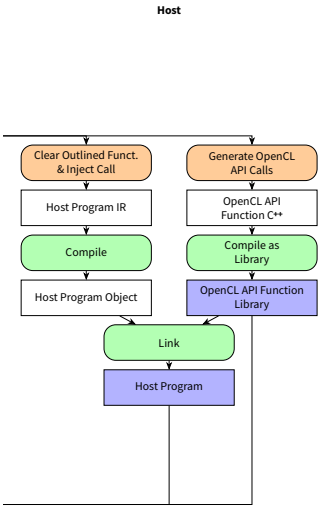

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4. Link to host program

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- But quick & easy (prototype)
- Better directly as LLVM IR
- Or even better …

Tighter compiler framework integration

- *libomptarget*
- Dedicated transfer infrastructure
- But requires *clang* modification

Evaluation of the Prototype

Workload

Sobel filter

- 4k integer RGB image

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Two implementations

- Naïve version
- FPGA optimized version

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    - `unroll` pragma
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    - structured to employ shift register

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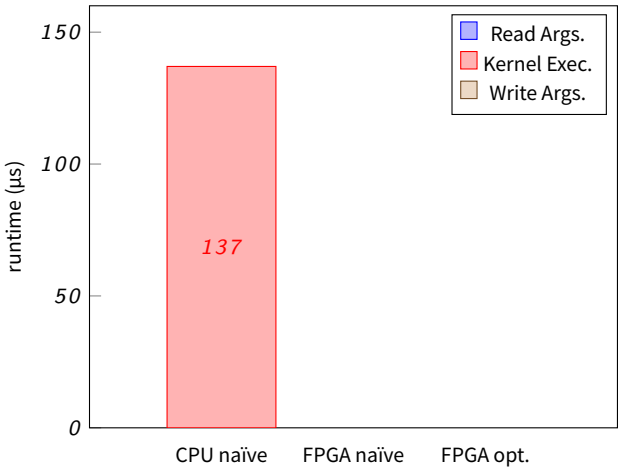
Hardware

- Intel PAC with a Arria 10 GX
- Intel Xeon W-2125 Skylake (Host & Reference)
- KVM virtual machine with PCI passthrough
  - Might have a small performance penalty

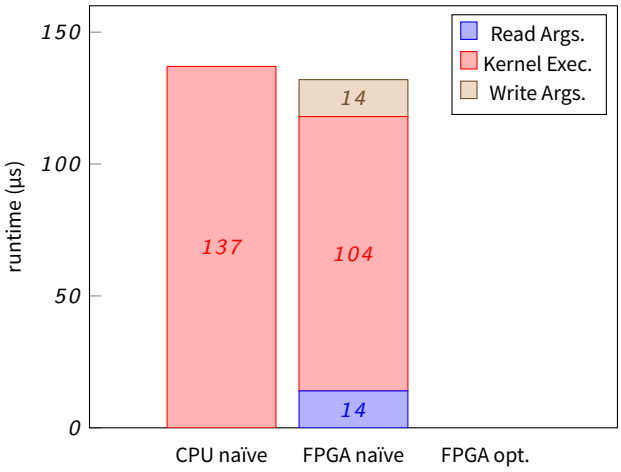
Baseline



Naïve CPU version

- Serves as a baseline
- No manual optimizations
  - Single threaded
  - No SIMD
  - ...

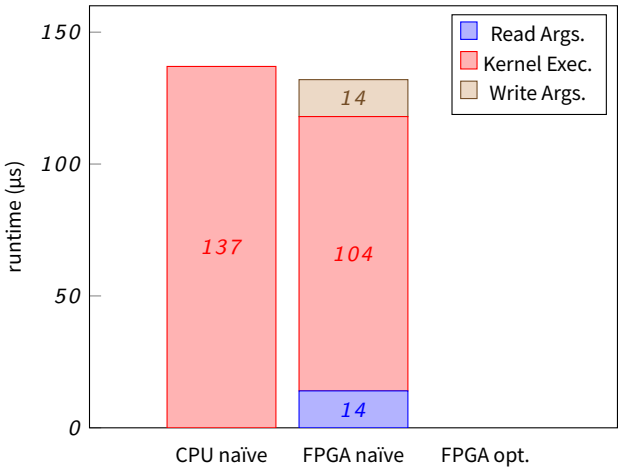
Naïve FPGA Version



Naïve FPGA version has equal runtime

- Actual Kernel is *slightly* faster

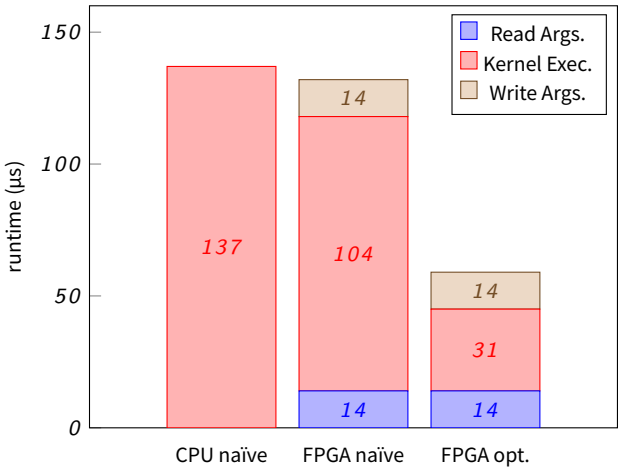
Naïve FPGA Version



Naïve FPGA version has equal runtime

- Actual Kernel is *slightly* faster
- Transfer Overhead
  - `map` clause not considered
    - `to` & `from` handled equal to `tofrom`
    - When considered, decrease by half

Optimized FPGA Version



Kernel of FPGA optimized version way better

- Shows simple annotation not enough (as expected)
- Requires code adaption

Future work

Outlook

- *libomptarget* integration
  - More elegant and powerful host code
  - `map` clause support
    - Map-type
    - Array sections

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- *libomptarget* integration
  - More elegant and powerful host code
  - `map` clause support
    - Map-type
    - Array sections
- Integration into Intel LLVM (Sycl) toolchain
  - Spir-V supported as an input
    - Khronos SPIRV-LLVM Translator
    - Intels new OpenCL FPGA Tools (`aoc -sycl kernel.spv`)