PASSIVE CMOS SENSORS FOR THE FUTURE
ATLAS HYBRID PIXEL DETECTOR

15. TRENTO WORKSHOP

Yannick Dieter\textsuperscript{a}, Jochen Dingfelder\textsuperscript{a}, Tomasz Hemperek\textsuperscript{a}, Fabian Hügging\textsuperscript{a}, Evelyn Kimmerle\textsuperscript{a}, Hans Krüger\textsuperscript{a}, Anna Macchiolo\textsuperscript{b}, Daniel Münstermann\textsuperscript{c}, David-Leon Pohl\textsuperscript{a}, Tianyang Wang\textsuperscript{a}, Norbert Wermes\textsuperscript{a}

\textsuperscript{a} Physikalisches Institut der Universität Bonn
\textsuperscript{b} Physik-Institut der Universität Zürich
\textsuperscript{c} Physics Department, Lancaster University
PASSIVE CMOS SENSORS

- Use commercial high-voltage/high-resistive CMOS process for planar sensor production, no active components:
  - Large wafers (200 mm)
  - High production throughput, low costs
  - Poly-silicon resistors → connection to bias grid
  - MIM capacitors for AC-coupling → no leakage into readout
  - Many metal layers for redistribution
  - Sub-pixel coding feasible?
    https://indico.cern.ch/event/855994/contributions/3637113/
  - Candidate for the outer barrel layers of the future ATLAS hybrid pixel detector
  - Moderate irradiation levels \(10^{15} \, n_{eq}/cm^2\), but large area to cover \(2 \, m^2 \rightarrow 14 \, m^2\)

LFoundry 150 nm 1.8V CMOS process
http://www.nanoitaly.it/nanoitaly/images/presentazioni/PS_2_1-Fama.pdf

- MIM capacitor: 1 fF/µm², 2 fF/µm²
- Polysilicon resistor: \(~ 2.2 \, k\Omega/\square\)
- 4 – 6 metal option, thick metal
- Back-side processing: thinning and implantation
- Lithographic stitching
HISTORY PASSIVE CMOS SENSORS USING LFOUNDRY PROCESS

Large pixel prototype
- 50 x 250 um² pixels, ATLAS IBL planar sensor geometry
- Performance comparable to ATLAS IBL sensors after irradiation > 1 \times 10^{15} \text{neq/cm}^2
- Investigation of AC-coupling schema, fill-factor, pixel biasing schemes (bias dot vs. resistor biasing),

Test structures
- Many structures produced (> 15)
- Varying designs: guard rings, pixel isolation, implantation geometries
- Investigations of break down with TID (2 master theses)
  → Identified enhanced guard ring structure
- Investigation of sensor capacitances (2 bachelor theses)

Small pixel prototype
- 50 x 50 um² pixels, ATLAS ITk pixel geometry

Sensor for ATLAS ITk modules
- 50 x 50 um² pixels, 25 x 100 um² pixels
- Full-size ATLAS ITk pixel modules
- Participation in ATLAS ITk pixel sensor market survey
- RD53A and RD53B compatible

Byproducts of DMAPS efforts (see previous talk)
LARGE PIXEL PROTOTYPE

- High resistive 4-5 kΩ cm p-type CZ wafer
- 50 um x 250 um pixels in 36 x 16 matrix
- 100 um / 300 um thickness, backside implant + metal
- Thinning in TAIKO process
- No backside etching after thinning → large current when depletion zone touches back side → full-depletion impossible
- AC coupled pixels:
  - 3 pF MIM capacitor in each pixel
  - Resistor biasing (15 MΩ poly-res. in each pixel)
- DC coupled pixels:
  - IBL planar silicon-sensor geometry
  - Punch-through biasing
  - Variation of implantation width 15 μm - 30 μm
- Pixel isolation: 4 μm p-stop with field plates
- More info: https://doi.org/10.1088/1748-0221/12/06/P06020
LARGE PIXEL PROTOTYPE: EFFICIENCY AFTER IRRADIATION

- **Requirement:** > 97% in-time hit-detection efficiency fulfilled at $1.1 \cdot 10^{15} \text{neq/cm}^2$
- **Efficiency loss at bias dot** for perpendicular tracks, due to competing charge collection electrode → **Resistor biasing** is attractive option for future small pixel

![Bias dot pattern](image)

**Efficiency map for unirradiated device, 120 GeV pions**

![Efficiency map](image)

**Mean efficiency at different levels of irradiation, ~ 3000 e threshold**

![Efficiency graph](image)
LARGE PIXEL PROTOTYPE: INPUT CAPACITANCE

- Input capacitance $C_d$ from sensor:
  - Gain: $g \sim \frac{1}{C_d}$, noise: $\sigma_{ENC} \sim C_d$, rise-time: $\tau \sim C_d$
  - Primarily defined by readout implantation geometry
- 28% reduction of the input capacitance
- $\sim 1\%$ reduction of detection efficiency at $1 \cdot 10^{15}$ neq/cm$^2$, perpendicular tracks

Capacitance vs. bias Voltage

Efficiency vs. Bias voltage

Data from M. Loepke

105 fF ($\sim$ IBL planar sensor)

28% decrease

75 fF
SMALL PIXEL PROTOTYPE

- High resistive 4-5 kΩ cm p-type CZ wafer
- 50 μm x 50 μm pixels in 64 × 64 matrix
- 100 μm / 200 um thickness, backside implant, etching + metallization
- Enhanced guard ring structure
- Bump bonded to RD53A
- DC coupled pixels only:
  - No biasing structure
  - Variation of n-well width: 15 μm - 30 μm
  - Variation of n-well depth: n-well and deep n-well
- More info: https://indico.cern.ch/event/803258/contributions/3582872/ (proceeding pending)
- Measured with RD53A @ 750 e threshold
- Fully efficient at 5V only
- Mean efficiency: 99.67% @ 100 V
- No difference in pixel flavors
- Efficiency measurement at $5 \cdot 10^{15}$neq/cm$^2$ pending
SMALL PIXEL PROTOTYPE: INPUT CAPACITANCE

- **New capacitance measurement chip** in TSMC 65 nm: PixCap65
  - Similar to large pixel design: [https://doi.org/10.1016/j.nima.2013.02.038](https://doi.org/10.1016/j.nima.2013.02.038)
  - < 1 fF precision
  - Ability to measure different contributions to input capacitance (inter-pixel, bump bonds, backplane)

**Input capacitance < 25 fF at full depletion**

**Goal:** also measure other ITk pixel sensor candidates

**Publication in preparation**
SMALL PIXEL PROTOTYPE: CHARGE MEASURED WITH RD53A

- Charge resolution is minor design goal for fast pixel readout chips
  - Challenging absolute calibration of pixel detector
  - Difficult to characterize sensors
- RD53A: access to unclocked charge signal
  - ORed output of pixels to “HitBus”
  - 4 HitBus networks → measurement of cluster charge
- Also very useful for timewalk measurements
- Implemented in BDAQ53 readout system: https://gitlab.cern.ch/silab/bdaq53

RD53A charge calibration with X-Ray sources

Charge deposited in 100 um LFoundry sensors, 3.2 GeV e- measured at the accelerator facility ELSA in Bonn

Network 1
Network 2
Network 3
Network 4

Network 1
Network 2
Network 3
Network 4
SMALL PIXEL PROTOTYPE: MAXIMUM BIAS VOLTAGE

- Observation:
  - Expected from test structures > 300 V, but many LFoundry sensors have lower break-down after flip chip; reversible after de-soldering
  - Already observed for large pixel design
- Finally understood:
  - Larger readout chip than prototype sensors → bump bonds touch sensor edge
  - Mitigation: remove not connected bump bonds, no issue for full-size sensors
• Design (mainly by Tianyang Wang)
  • Different sizes for modules:
    • RD53A single and dual chip modules
    • RD53A/B quad module
  • Different pixel flavors:
    • 50 x 50 \( \text{um}^2 \) and 25 x 100 \( \text{um}^2 \)
    • AC or DC coupled
  • Float-zone wafer material (first time...)
  • Thinning to 150 \( \text{um} \) + handling wafer and backside implantation already at LFoundry
  • Status: Submitted end of 2019, 10 wafers available since 3 weeks, currently at IZM Berlin for backside metallization, dicing, flip-chip
ATLAS ITK PASSIVE CMOS SENSOR: STITCHING AND BIASING

- Sensor size > reticle size → reticle stitching needed
- Different reticles (~ 1 cm x 1 cm):
  - Sensor edge guard ring reticles
  - Sensor center pixel reticles

- Repeat them for different designs:
  - Sensor edge guard ring reticles
  - Sensor center pixel reticles

- Resistor biasing of all pixel flavors:
  - Former large pixel sensor prototype: 15 MΩ
  - Full-size design: > 2.5 MΩ

- AC coupled pixels using MIM capacitor in each pixel:
  - Former large pixel sensor prototype: ~ 3 pF MIM capacitor
  - Full-size design: 0.56 pF

15. Trento Workshop
David-Leon Pohl
ATLAS ITK PASSIVE CMOS SENSOR: GUARD RINGS

- Guard ring of test structure with highest break down
- Very similar guard ring implemented in this design
- Already used in previous monolithic design

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**Foundry designs: IV curves before irradiation**

*Test structure*

*Large pixel sensor*

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- Similar break down > 300 V expected in this design
- To be measured...
• Many passive CMOS sensors and test structures produced and measured in the last 5 years

• Similar performance to other planar silicon sensors (at $1 \cdot 10^{15}$ $n_{eq}$/cm$^2$)

• Lessons learned: backside etching needed, for sensors < readout chip edge passivation needed

• Improvement of guard rings: 160 V $\rightarrow$ $>300$ V break down before irradiation

• No break down after irradiation (measured up to 700 V)

• Measurements at $5 \cdot 10^{15}$ $n_{eq}$/cm$^2$ prepared

• Full-size sensor, for up to four RDS3B chips, recently available

• To be measured soon...
\[
\frac{V_{\text{out}}}{V_{\text{noise}}} = \frac{C_{\text{det}} + C_{\text{in}} + C_f}{C_f}
\]

\[
\langle C_D^\text{Si} \rangle = (117 \pm 2) fF \quad \text{planar electrodes, sample A}
\]

\[
\langle C_D^\text{Si} \rangle = (123 \pm 4) fF \quad \text{planar electrodes, sample B}
\]

\[
\langle C_D^\text{Si} \rangle = (181 \pm 2) fF \quad \text{3D electrodes}
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