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Passive CMOS sensors for the future ATLAS hybrid pixel detector

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With the upgrade of the inner tracking detector of the ATLAS experiment in 2026, the surface covered by hybrid pixel detectors increases from less than 2 m² at present to approximately 13 m². This makes sensor designs that utilize cost-effective, high-throughput CMOS processing lines with large and high-resistive wafers an attractive option. In addition, CMOS process features can be used to enhance the sensor design, for example by the implementation of bias resistors or AC coupling capacitors in every pixel.

Multiple sensors in the LFoundry 150 nm process technology were produced and characterized with the ATLAS FE-I4 and RD53A readout chips. Important properties like hit detection-efficiency, breakdown behavior, and input capacitance are presented for various pixels designs. A method for cluster-charge measurement using the RD53A is depicted and the recent full-size sensor production, covering up to four RD53Bs, is introduced.

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