Module Development for the ATLAS ITk Pixel Detector

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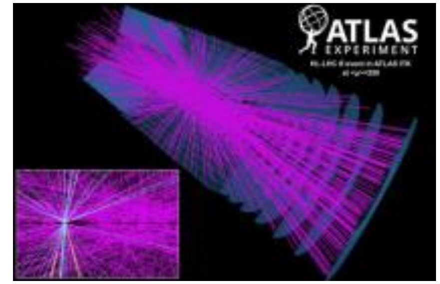
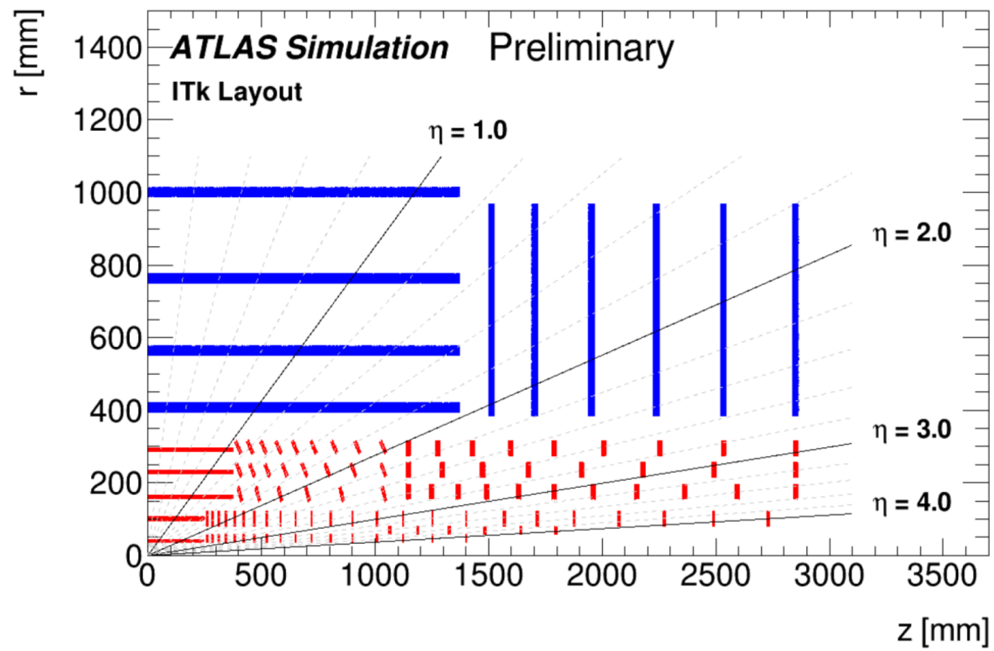
ATLAS ITk Upgrade

- HL-LHC upgrade 2025-2027:
  - 5-7.5x instantaneous luminosity
  - 200 collisions per bunch crossing
  - Increased particle density
  - Higher radiation levels
  - 4,000 fb^{-1} over ~10 years

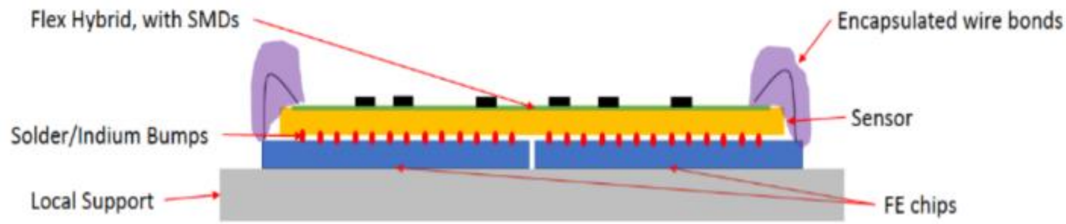


- ATLAS replaces Inner Detector (ID) with all-Si Inner Tracker (ITk)
  - 4 strips and 5 pixel layers
  - Focus here on pixel part:
    13 m² area, 10,000 hybrid modules
  - Higher granularity
  - Faster readout
  - Increased radiation hardness

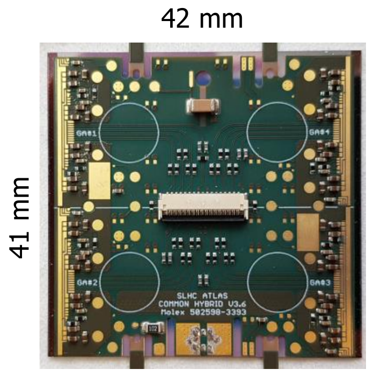


ITk Pixel Modules

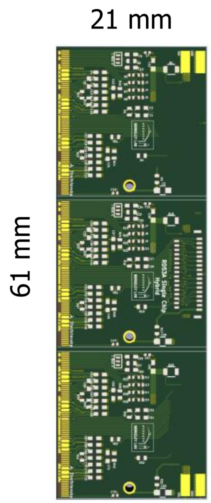
- Silicon sensors for signal creation
  - Different technologies and geometries
  - Pixel size 50x50 µm² **and** 25x100 µm²
  - Parylene coating for HV protection
- ITkPix frontend (FE) chip for readout
  - Developed with RD53 collaboration
  - 400x384 pixels of 50x50 µm² → 20x21 mm²
  - Half-size RD53A prototype available:
    400x192 pixels of 50x50 µm² → 20x12 mm²
- Bump-bond interconnection (SnAg or In)
- Flexible PCB ("flex") + wire bonds
- Different module hybrid configurations
  - Common quads (L1-L4)
  - Triplets (L0)
- Serial powering
  (see talk by Q. Buat)



Quad
4 FEs + 1 sensor



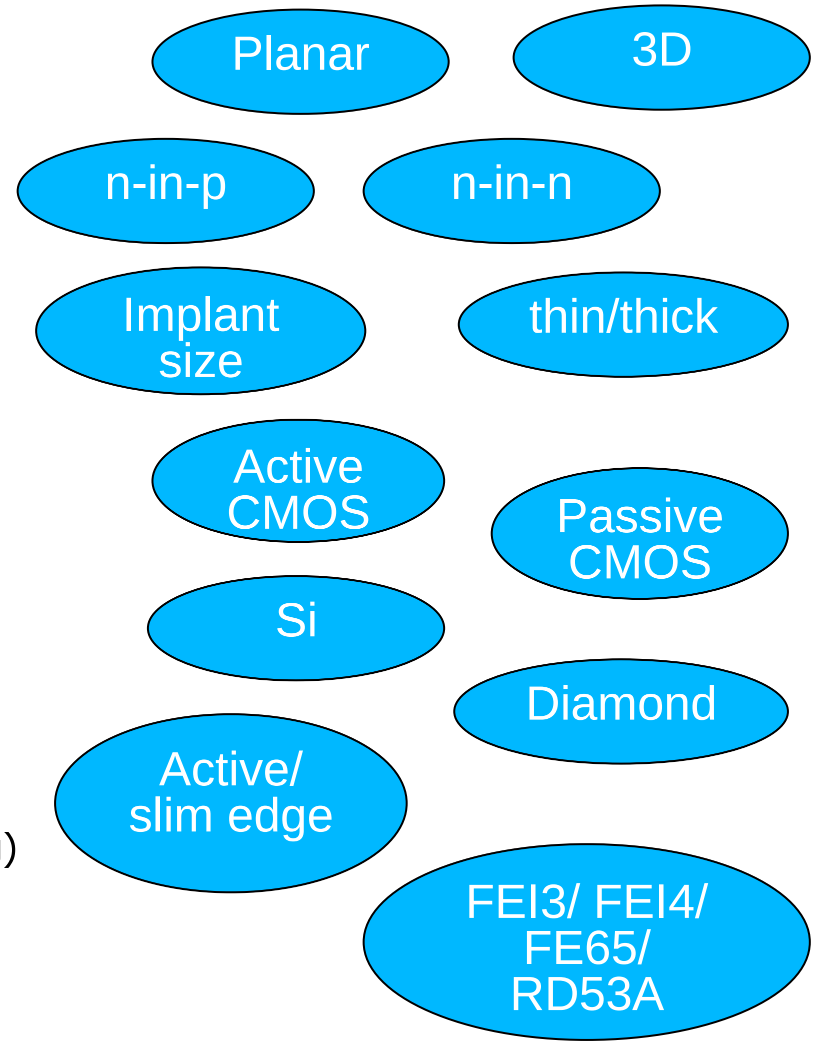
Barrel Triplet
3 FEs + 3 sensors



Sensors: R&D → Production

- Decade of extensive sensor R&D…
  - Many different materials, technologies, geometries, vendors, FEs etc. studied
  - Collaboration of ITk institutes, typically driven by individual groups with close contact to vendors
  - Activities still on-going:
    see talks by M. Bomben, N. Wermes, R. Cardella, D.-L. Pohl, M. Samy, M. Povoli

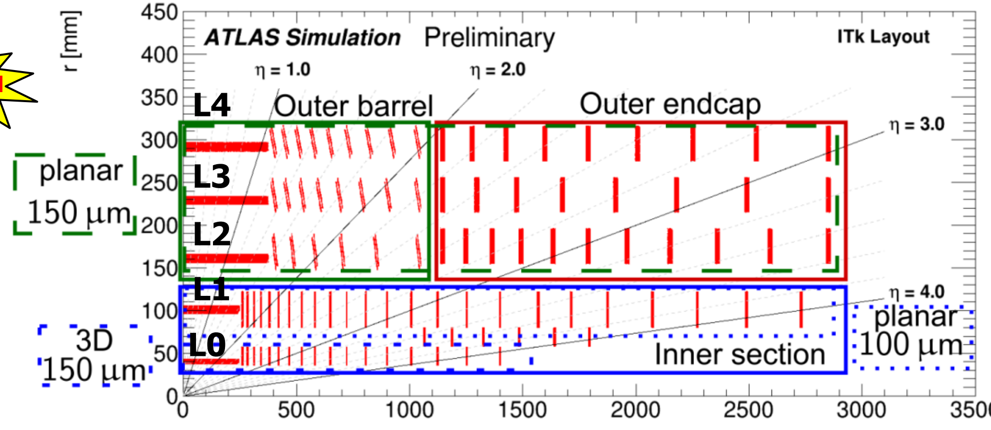
→ **successful qualification of radiation-hard sensors for ITk Pixel**



- … going over to production mode
  - Selected baseline technologies + geometry
  - Finalised layout
  - Selecting vendors now (market survey + tendering)
  - ITk-central qualification and production

Final Sensors and Layout

- Different conditions for different radii
- Inner layer radius revised to 3.4 cm Reviewed
  - Improved vertexing + b-tagging
  - Increased radiation levels
- Exchange 2 inner layers at least once to mitigate radiation levels
  - Exact strategy depends on review of sensor radiation hardness
- Use of optimised sensor technology and geometry



Caveat: L0 still at 3.9 cm (not yet updated)

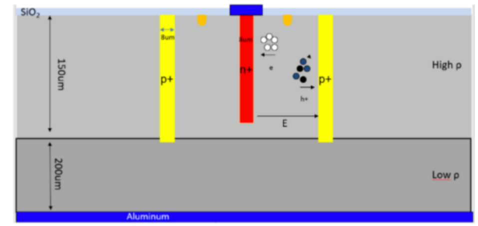
Layer	Sensor Type	Thickn. [µm]	Sensor Size [µm²]	Module Type	Replace-ment	Fluence [1e15 n_{eq}/cm²]
L0 barrel	3D n-in-p	150	25x100 1E	Triplet	Yes	18 (2 ab^{-1})
L0 rings	3D n-in-p	150	50x50 1E	Triplet	Yes	18 (2 ab^{-1})
L1	Planar n-in-p	100	50x50	Quad	Yes	4 (2 ab^{-1})
L2-4	Planar n-in-p	150	50x50	Quad	No	1-4 (4 ab^{-1})

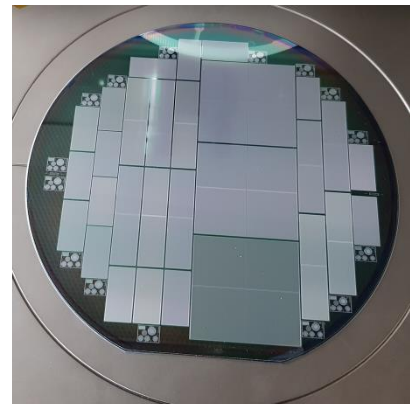
Reviewed

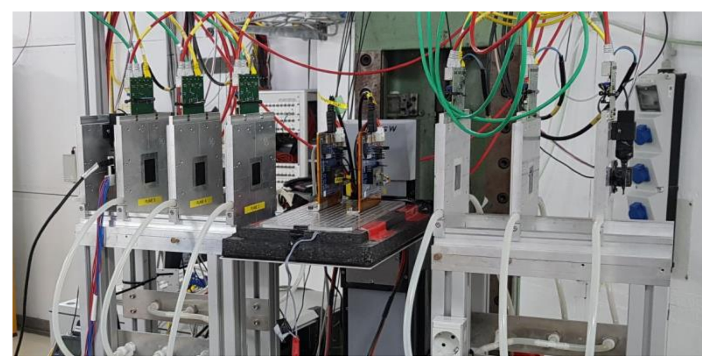
Incl. 1.5x safety factor

Towards Sensor Procurement

- Different strategies for 3D and planar
- 3D
  - Market survey based on existing prototype runs with proven published performance
  - Passed Final Design Review Nov 2019
  - Pre-production starting Q1/2020
- Planar
  - Market survey based on extensive qualification of newly ordered sensors from N vendors
  - Measurements performed by collaboration of ITk institutes cross-checking each other
  - Metrology, electrical characterisations (CV/IV/It), efficiency in test beam; all before+after irradiation
  - Need to fulfill documented requirements
  - Final Design Review Q2/2020 → tender
  - Pre-production starting Q2/2020

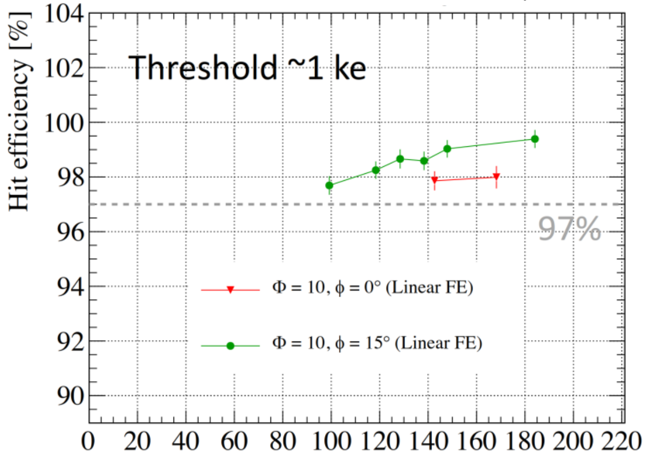






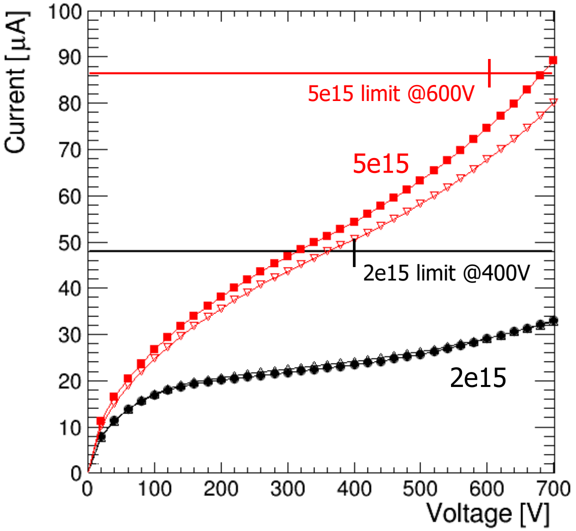
Sensor Market Survey - Examples

3D 25x100 µm² 1E, 1e16 n_{eq}/cm²

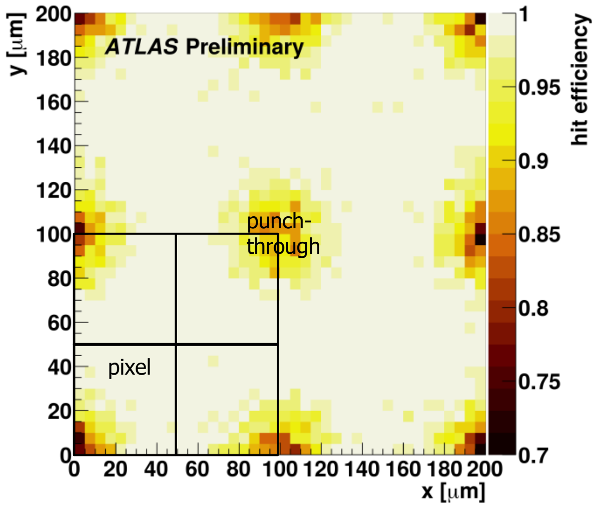


S. Terzo, HSTD 2019

Planar IV after irradiation at -25°C



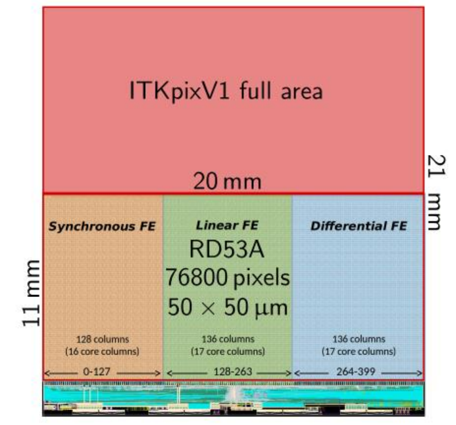
Planar hit efficiency, unirradiated, V_{dep}+50 V



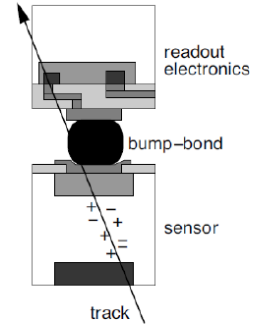
- 3D efficiency >97% at 1e16 n_{eq}/cm²
  - Campaigns to 2e16 n_{eq}/cm² ongoing
- Planar IV after irradiation below limits
- Planar hit efficiency
  - Before irradiation
    - >97% overall
    - >99% outside punch-through dots
  - After irradiation: Test beam in March

Readout Chip and Hybridisation

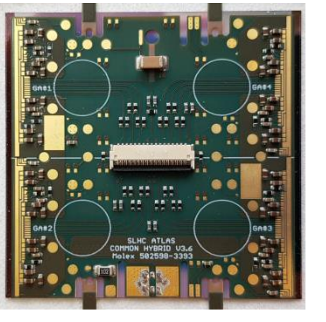
- ITkPix frontend (FE) chip for readout
  - Half-size RD53A prototype extensively studied by ATLAS and CMS
  - 3 FEs tested → selected differential FE (low noise) for ITk
  - Passed Final Design Review Sep 2019
  - Submission of full-size ITkPix_v1 soon



- Bump bonding
  - Demonstration of fine-pitch bump-bonding on RD53A successful
  - Market survey of vendors for different process steps:
    chip bumping, UBM, flip-chip
  - Important aspect: bump connection strength and thermal stress



- Flex hybrid
  - Designs for common flex hybrids finished (RD53A)/ongoing (ITkPix)
  - Reduced Cu content to 2 layers of 25 µm to mitigate CTE mismatch
    with Si → expect less stress on bumps



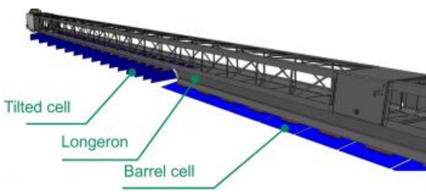
Towards Module Production

Several module prototype stages:

1) General module design explored on FEI4 prototypes
   - FEI4 demonstrator → module and system aspects (see talk by Q. Buat)

Functional FEI4 Quad

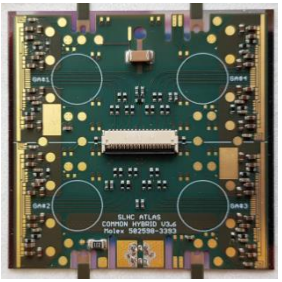
FEI4 Demonstrator



2) Now next phase with RD53A module prototypes
   - About 250 RD53A modules to be built in next months
     - Planar + 3D
     - 100 + 150 µm sensors
     - 150 + 400 µm FE chip
     - Quads + triplets
   - Extensive studies: thermal cycling, serial powering, new demonstrator to explore system aspects, …

   → Thorough design validation phase

RD53A Quad Dummy



RD53A Triplet Flex

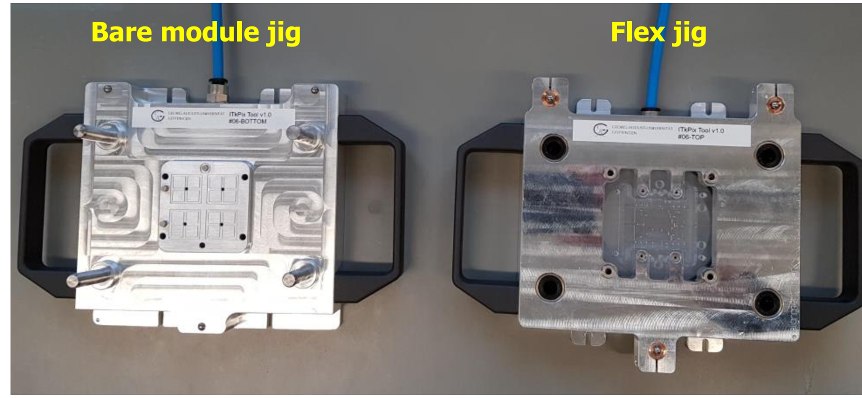
3) ITkPix_v1 modules in second half of 2020

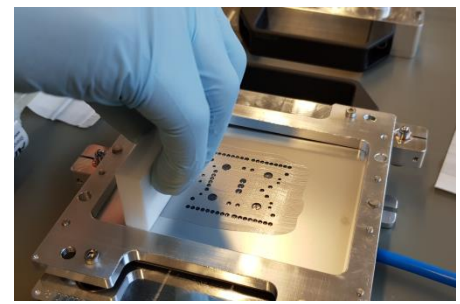
4) Module pre-production starting 2021

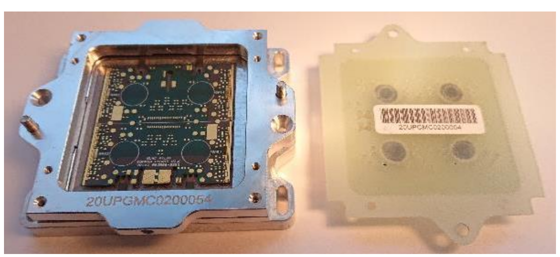
Module Building

- Developed common method for flex-to-bare-module attachment
  - In total ~20 module building institutes
- Based on tool with jigs incl. vacuum suction and dowel pin alignment
  - Edge of bare module
  - Holes in flex frame or body

  → 50 μm alignment precision
- Glue height (40±15 μm) adjusted with spacers and precision adjustment screws
- Glue dispensing with stencil (Araldite2011)
- Wire bonding
- Storage and shipment in module carrier





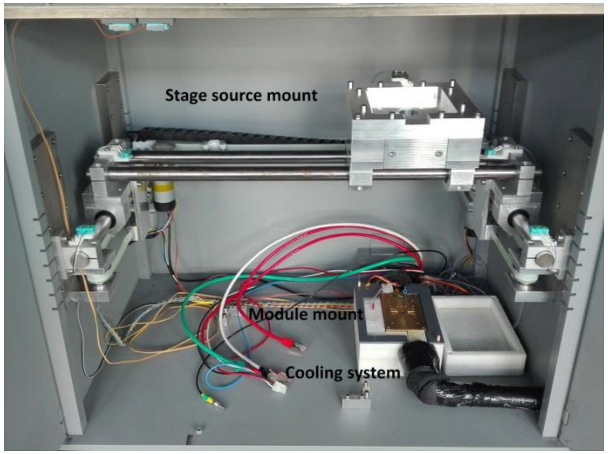


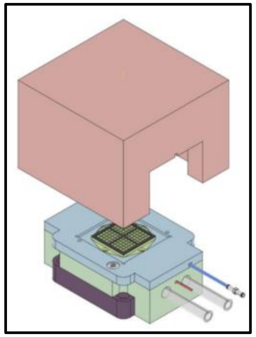
Module Testing

- 2 different testing categories
  - Design validation (DV) during prototyping and pre-production
    → very detailed testing beyond design specifications
  - Quality control (QC) on each module built during production
    → assure installation of good modules
- Metrology/visual inspection
- Electrical connectivity testing
- Tuning of chip parameters
  - E.g. threshold, ToT, …
- Radioactive source scans
- Burn-in/operation at low temperatures
- Thermal cycling

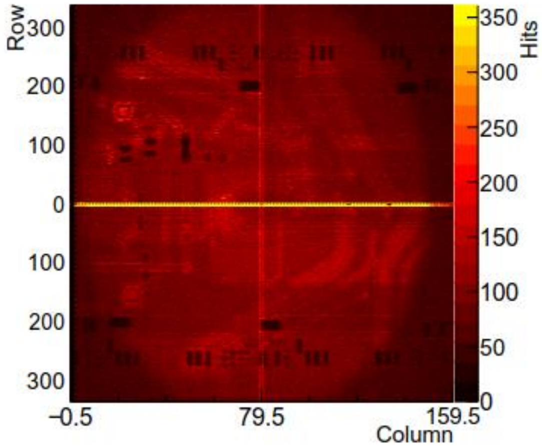
→ Goal: parallelisation of ~4-8 modules

Test Box with Cooling Unit



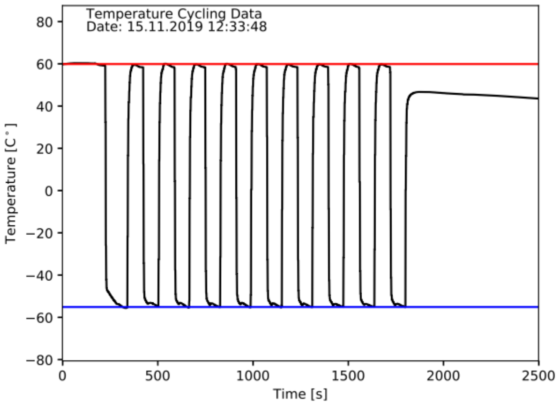


Source Scan on FEI4 Quad



Thermal Cycling and Bump Stress

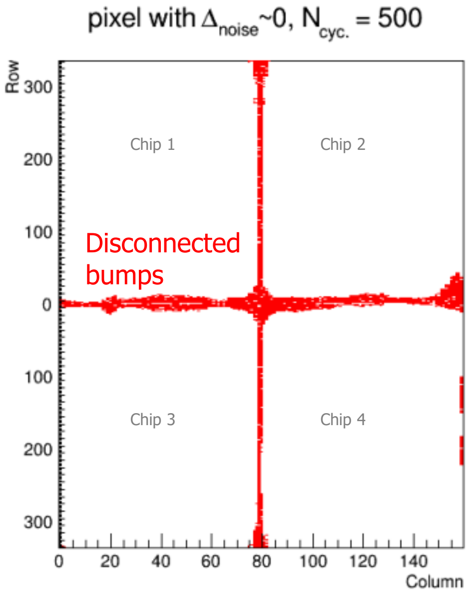
- Thermal cycling causes bump stress, in particular in case of large CTE mismatch between flex (Cu) and Si



- Consider different T ranges
  - Operational T range -45°C to +40°C
    → About 100 cycles during lifetime
  - Failure T range -55°C to +60°C
    → About 1 cycle during lifetime

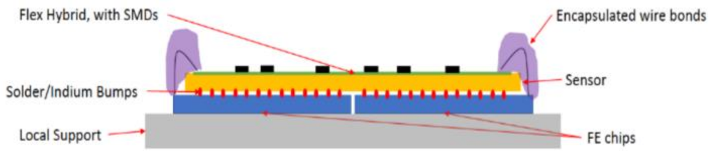
- Disconnection in inter-chip region seen on ~20 FEI4 quads
  - Measured from noise difference: sensor biased vs. not biased
  - With flex (2x35 μm Cu), no carbon cell, no parylene
  - Improves with parylene coating

Cycling on FEI4 Quad

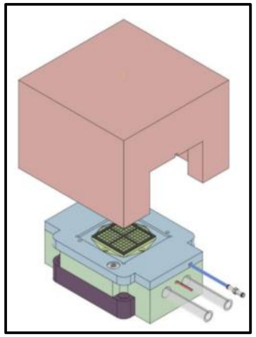


- Launched extensive campaign on daisy chains and RD53A prototypes
  - Different flex material and Cu content (2x 18-36 μm); with and w/o parylene; on Carbon cell structures

Conclusions and Outlook



- ITk pixel module development
  in transition to production phase
- Sensors
  - 3D for inner layer: 25x100 and 50x50 µm², 150 µm
  - Planar for outer layers: 50x50 µm², 100 µm (L1) and 150 µm (L2-L4)
  - In procurement process
- FE chip
  - RD53A prototype tested
    → differential FE selected
  - ITkPix_v1 to be submitted soon
- Module building and testing
  - FEI4 prototype phase completed
  - Extensive RD53A module phase starting
  - Design validation of module and system aspects
- Module pre-production starting in 2021



Backup