Serial Powering in the CMS silicon tracker detector for High-Luminosity LHC

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Outline

- Motivation for serial powering
- Implementation for the CMS pixel tracker upgrade
- The Shunt-LDO regulator on RD53A
- Main challenges of the system
- Improvements after RD53A

Motivation for Serial Powering

Inner tracker challenges at high luminosity

Increased radiation levels

- Innermost layer at 3 cm from beam
- Up to $2.3 \times 10^{16}\ \mathrm{n_{eq}cm^{-2}}$ fluence
- Total dose of 1.25 Grad max

→ **Radiation hard components**

Higher granularity

- More pixels to read out

Increased hit rate

- Higher bandwidth

65 nm CMOS technology

- 1.2V operating voltage $\Longrightarrow$ higher current

→ **High current consumption**

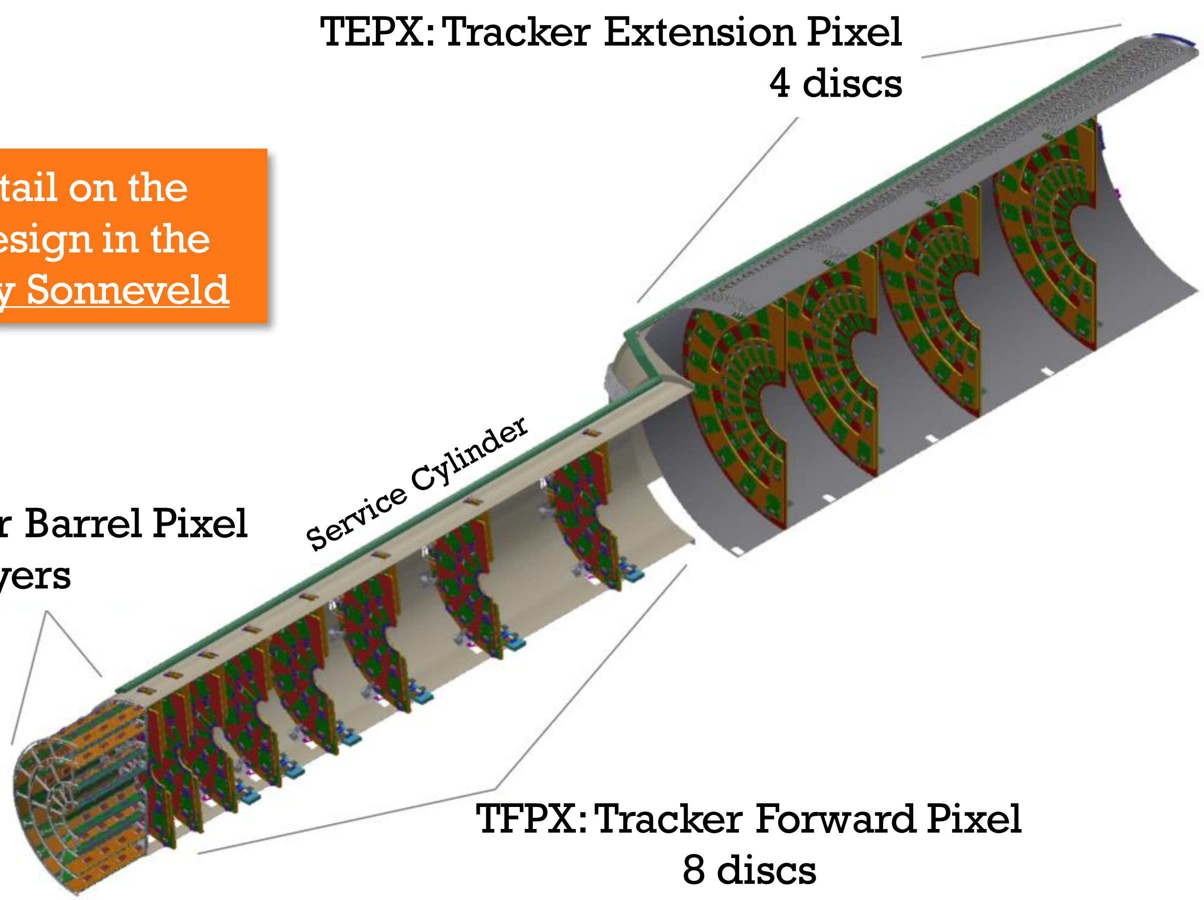
Low material budget

- Low mass cabling
- Avoid substantial power loss/voltage drop on cables

→ **Limit current on cables**

CMS IT upgrade – powering requirements

More detail on the overall design in the talk by Jory Sonneveld



Powering specific requirements

- 50 kW on detector power
- High current required by ROCs
- 3900 readout modules

\+

Low material budget

Serial Powering only viable solution

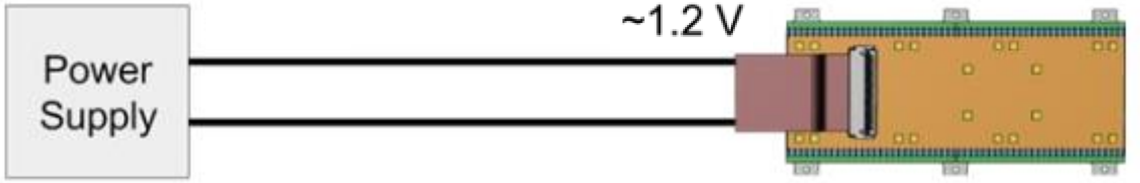
Advantages of serial powering

✗ Direct parallel powering

- 2 cables per module
- Total power consumption:

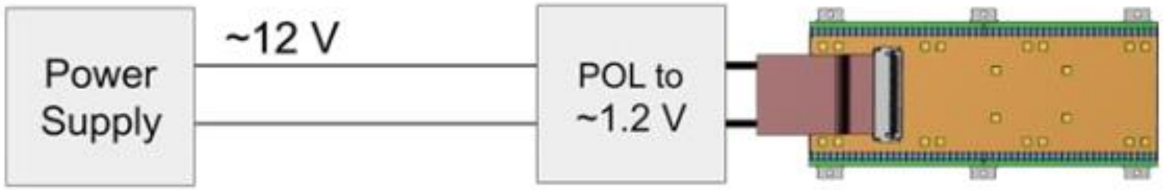
$$nIV + \boxed{n^2 I^2 R}$$

High power/voltage loss on cables



✗ POL conversion with DC/DC converters

- 12V ⟶ 1.2V conversion
- Not radiation hard enough (150 Mrad max)
- Component size, hefty material addition

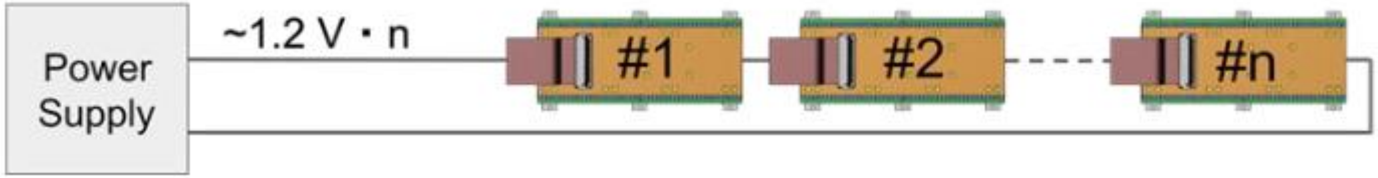


✓ Serial Powering

- 2 cables per chain
- 1.5V ⟶ 1.2V POL conversion
- Total power consumption:

$$nIV + \boxed{I^2 R}$$

Lower power loss on cables



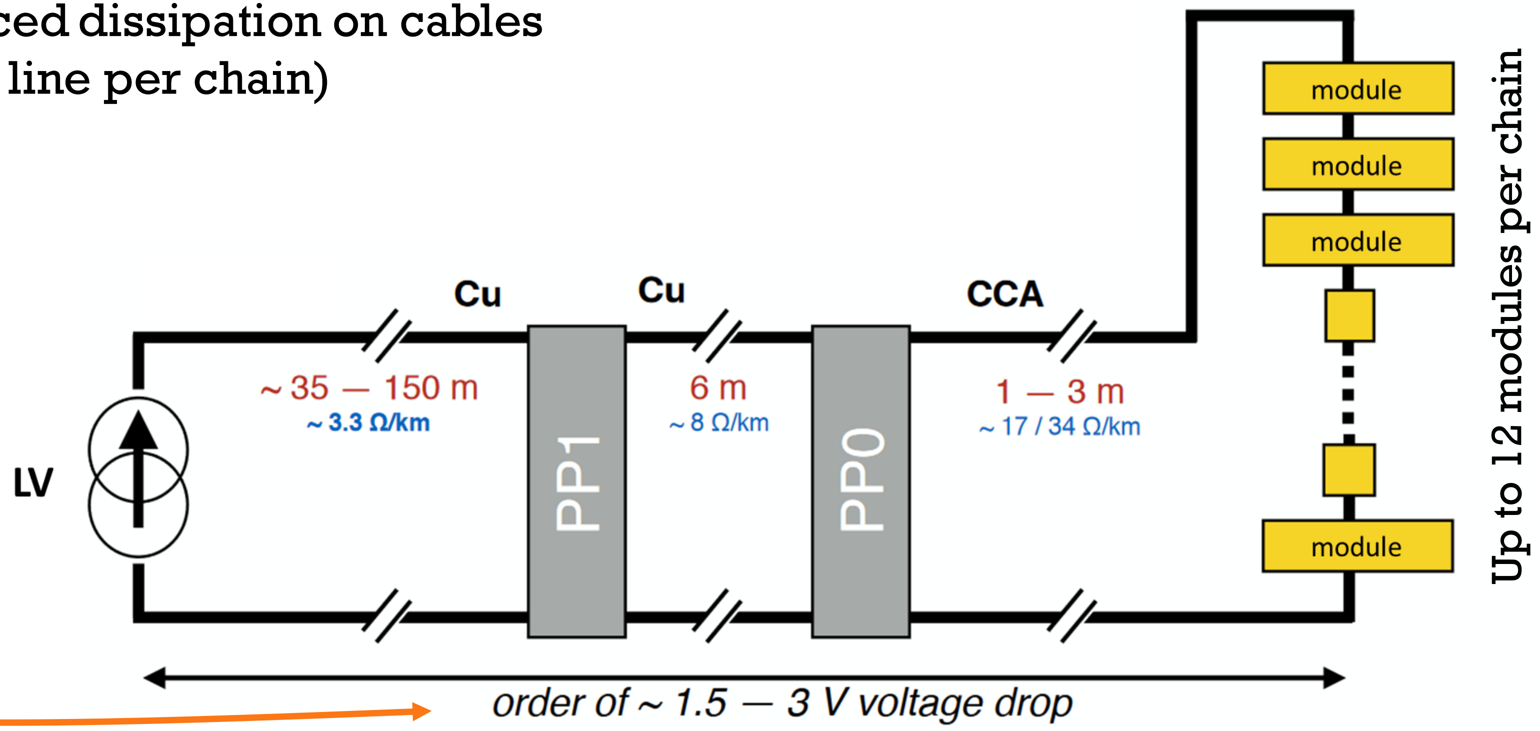
Serial Powering implementation

CMS IT Phase II

Chain layout – low voltage distribution

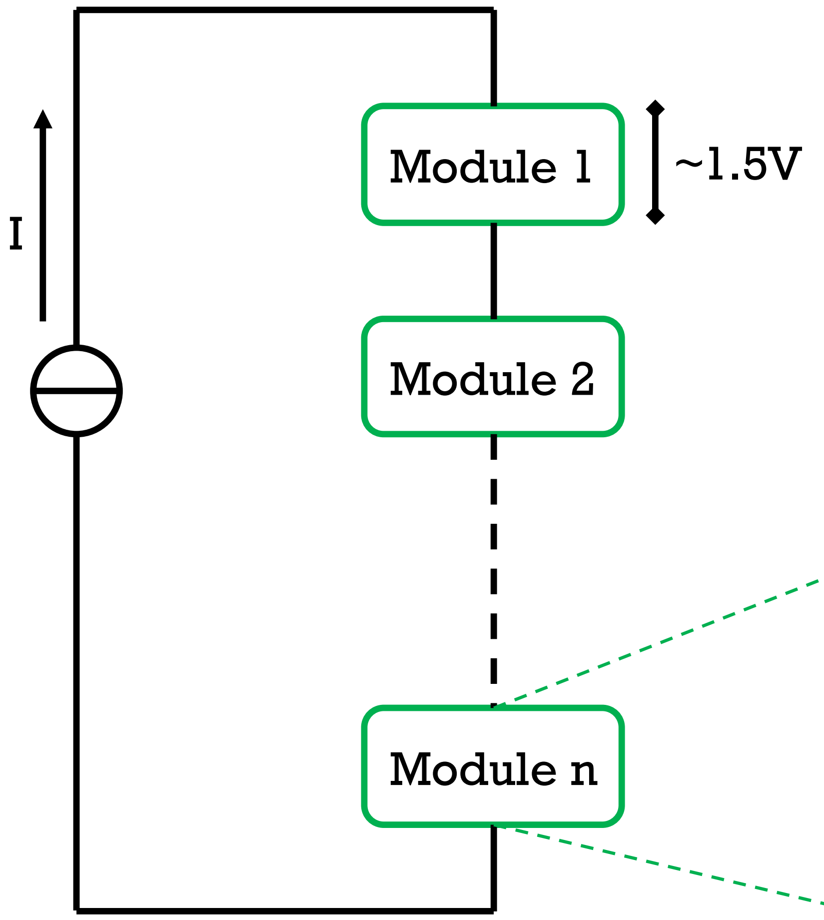
- Constant current supplied to readout chips
- Voltage conversion on ROC, no additional power electronics on modules
- Lower supplied current ⟹ reduced dissipation on cables
- Allows for reduced cabling (one line per chain)

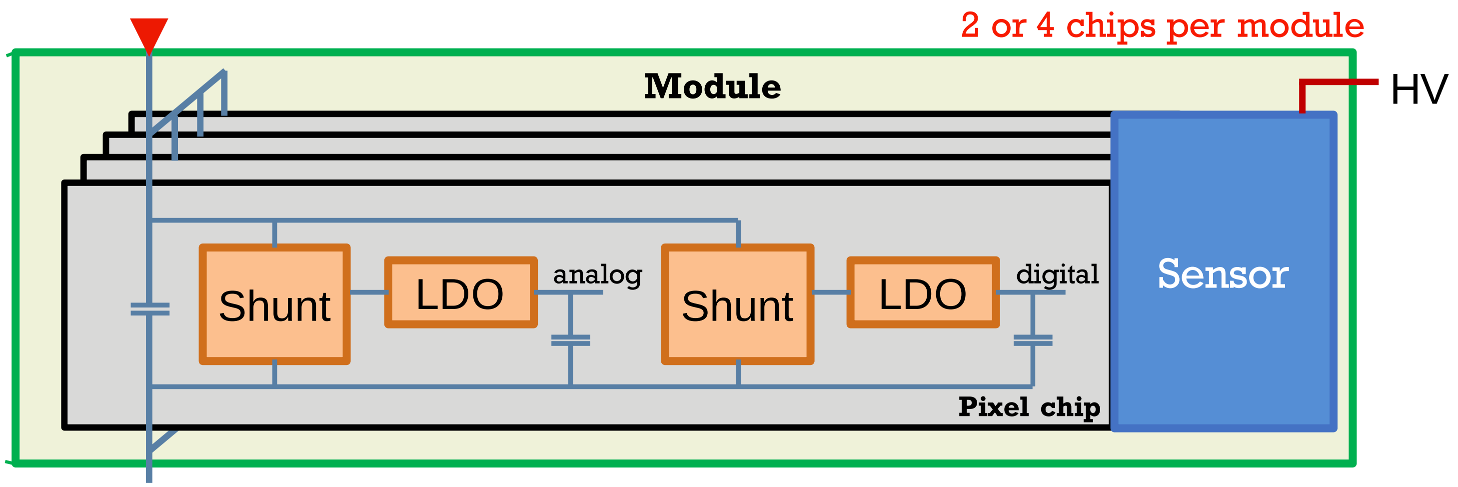
Voltage drop on cables not an issue in constant current mode



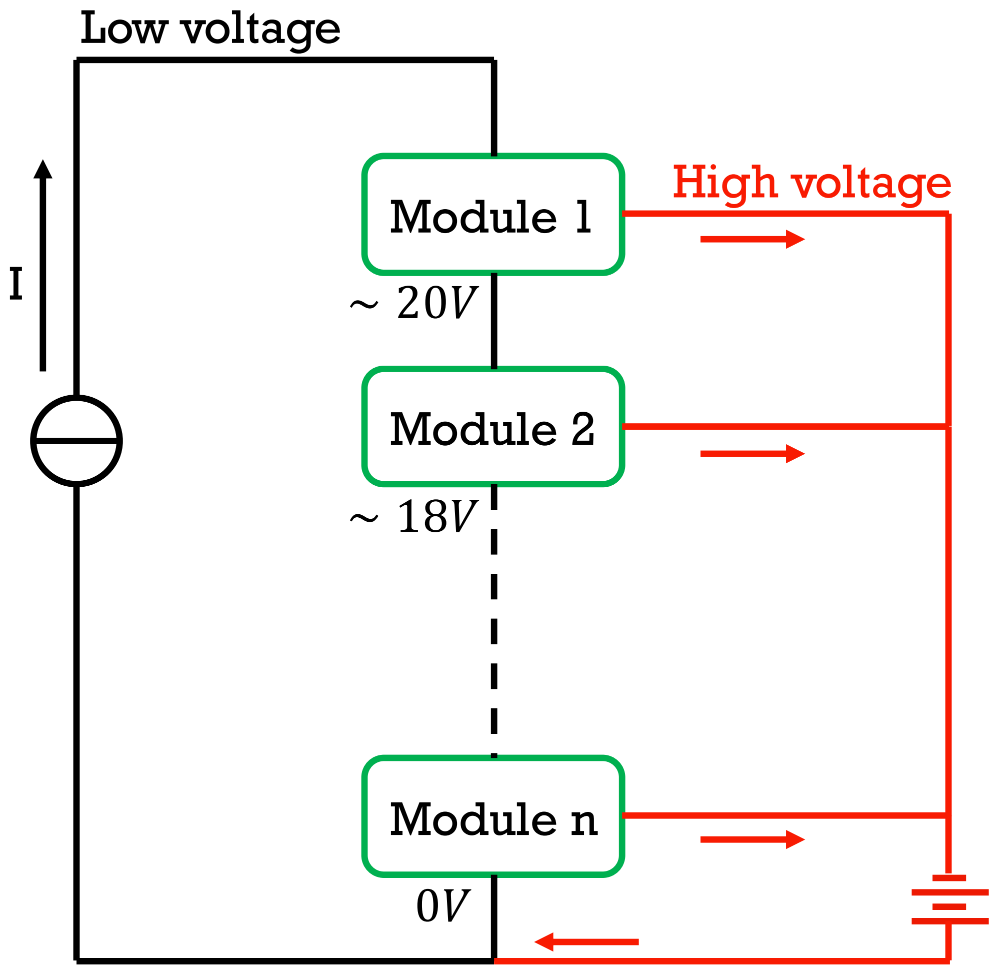
Chain layout – low voltage distribution

- Local GND reference changes along the chain
- Each module comprised of 2 or 4 chips powered in parallel and bump-bonded to a single sensor
- Variations in digital power consumption compensated by shunt
- Separate regulators for analog and digital domains to keep analog part immune from digital activity





Chain layout – high voltage distribution



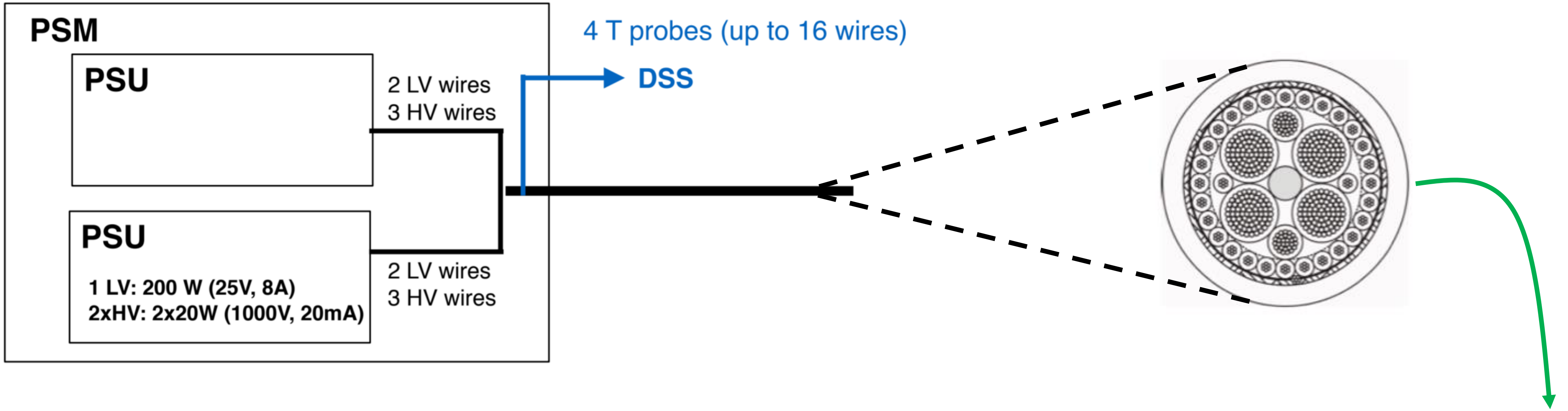
- High voltage for sensor biasing provided in parallel
- Common return with low voltage line

HV referenced to local chip ground potential

Effective bias voltage changes by up to ~20V between upstream and downstream modules

- Mitigated with 2 separate HV lines per chain

Power supply layout



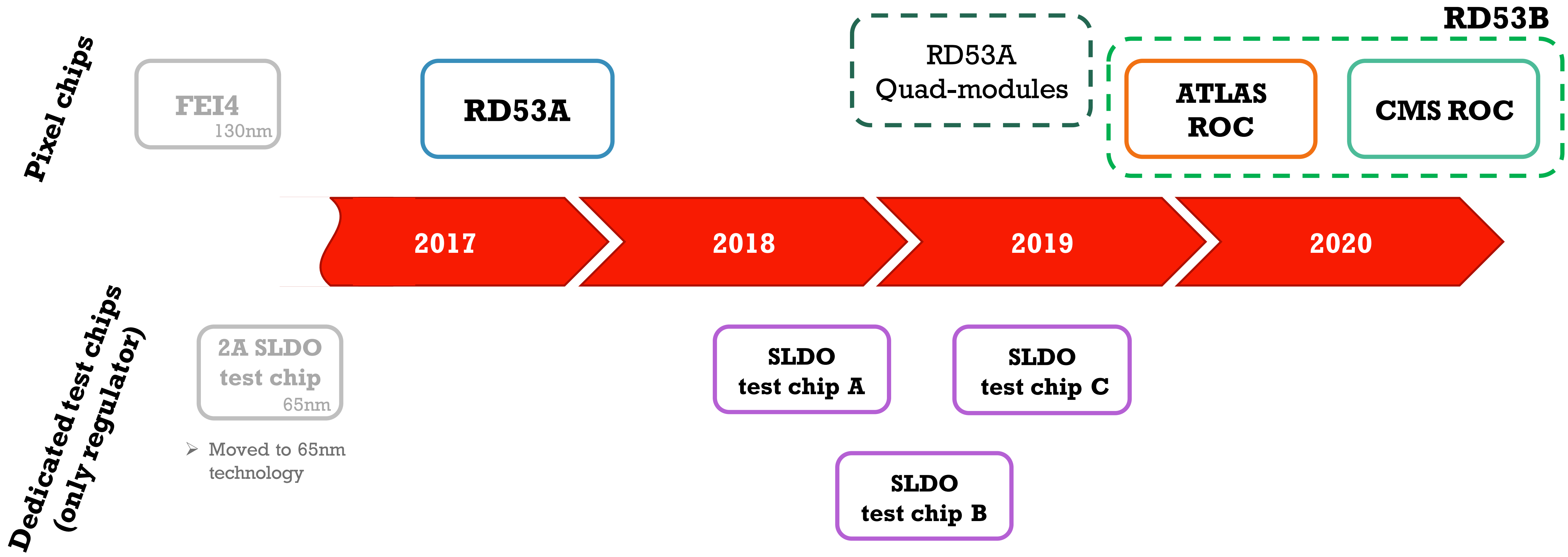
- Grand total of 500 serial lines
- 164 “4A” lines for double modules
- 336 “8A” lines for quad modules

- LV: 200W power at ~25V
  - $1.5V \times 12$ modules $+7V$ (MAX) drop on cables
- HV: 1000V, ~20mA (TBD)

4 LV lines
6 HV lines
TBD { Environmental probes
Drain wires

The Shunt-LDO on RD53A

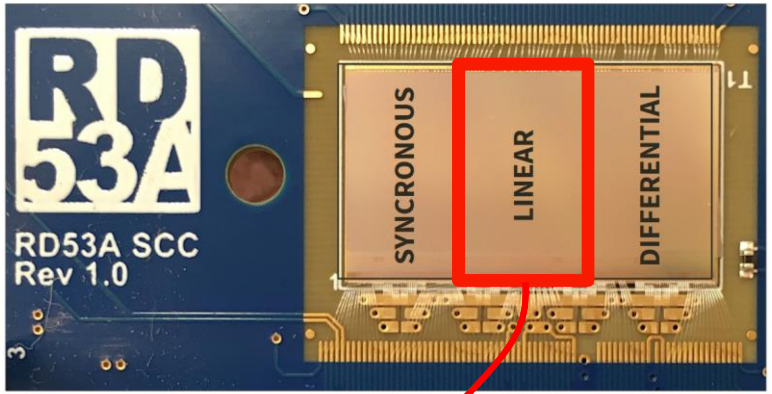
ROC and SLDO roadmap



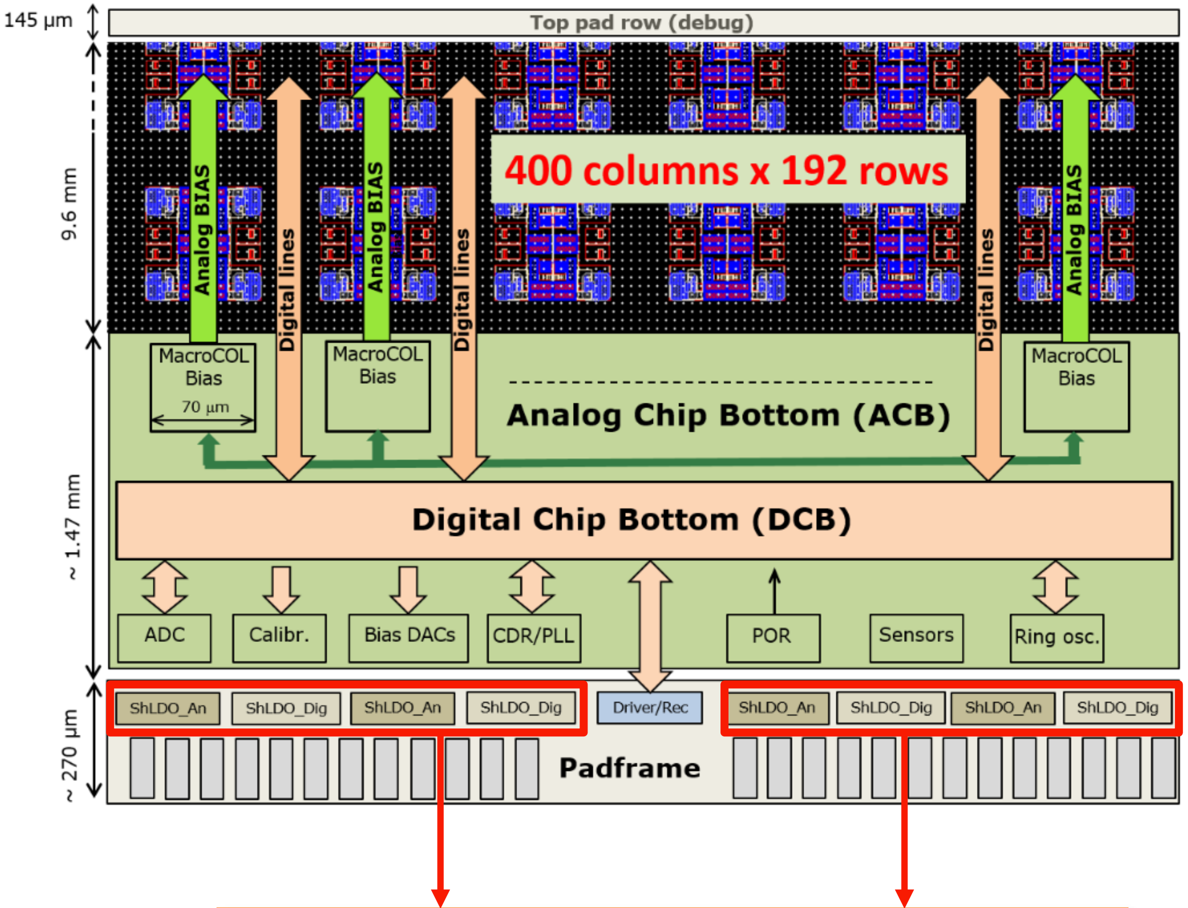
Improved performance (Startup, voltage accuracy, ..)
New features (Overvoltage/overload protection, ..)

The RD53A readout chip

- Designed by the RD53 collaboration
- RD53A: 3 different front ends for prototyping
- Built in 65nm CMOS technology
- Half size w.r.t. final CMS ROC
- 400x192 pixels (50x50 μm^2 each)
- Highly radiation resistant (above 500 Mrad)



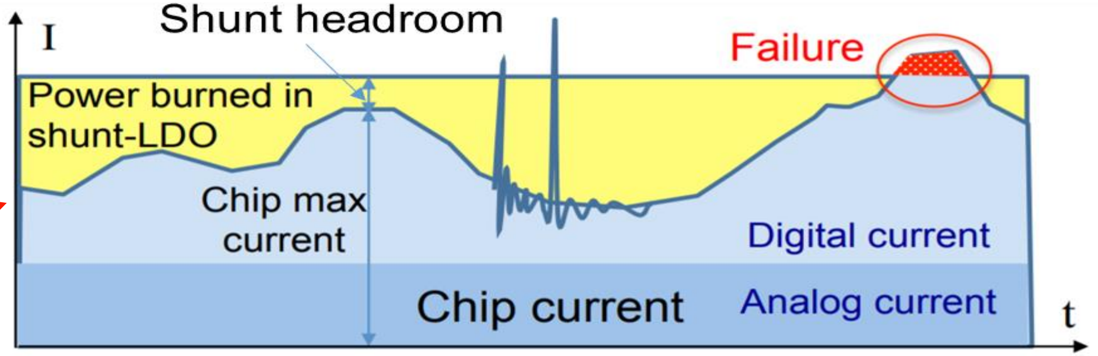
Linear front end chosen by CMS



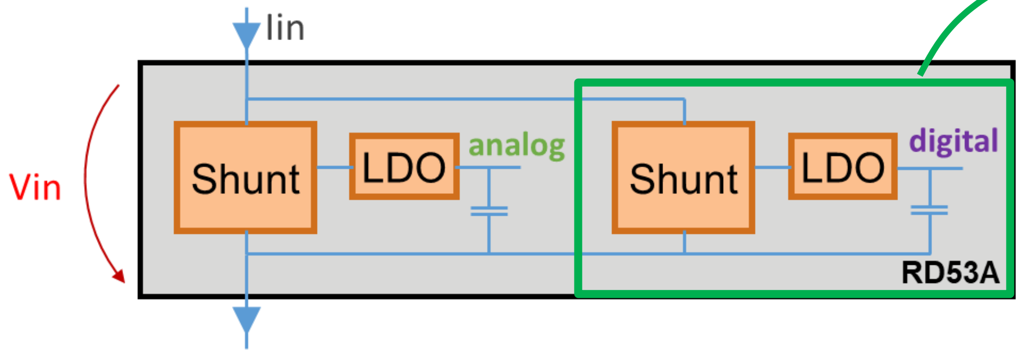
Shunt-LDO components on chip bottom

The Shunt-LDO regulator

- Constant input current is converted to constant voltage on the chip
- Power consumption (digital in particular) highly variable
- Enough current must be supplied to avoid failures
- Need to "burn" excess current



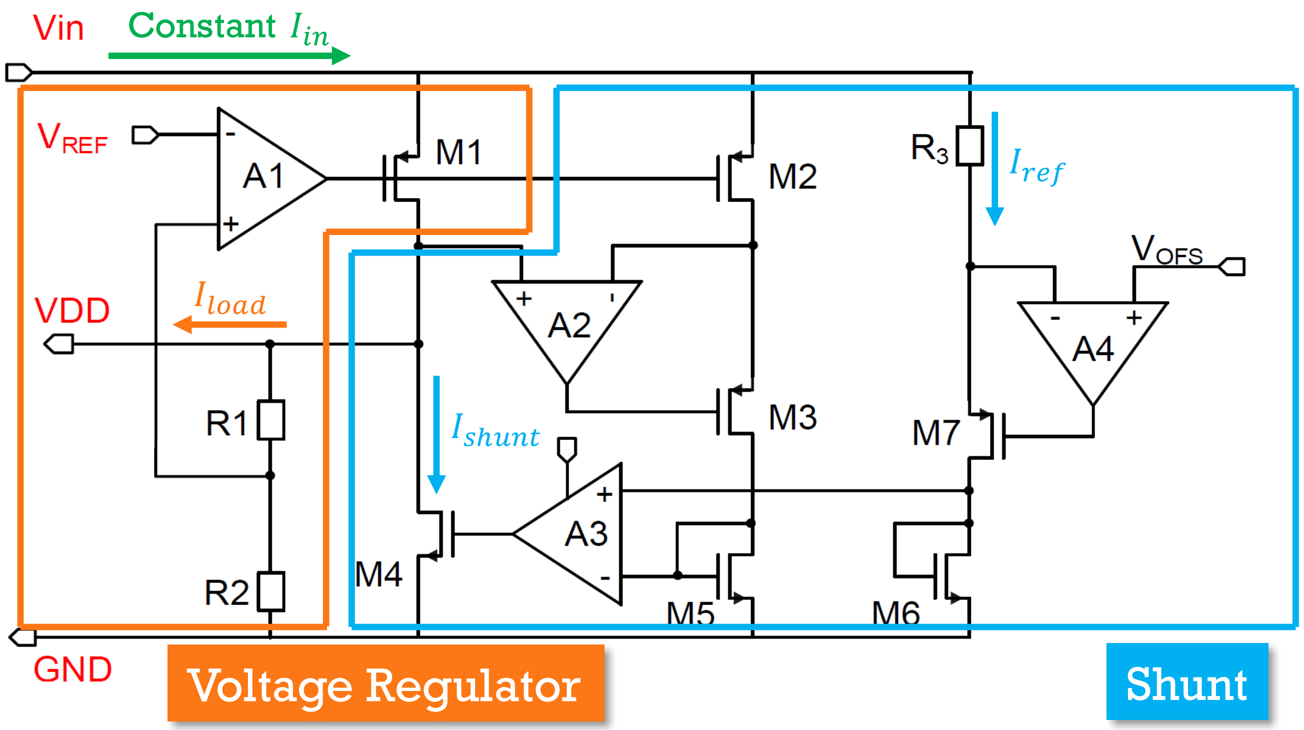
Shunt-LDO solves both issues



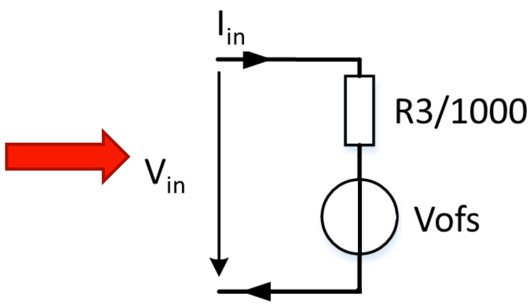
- LDO provides constant voltage (~1.2 V) drawing the required current I_{load}
- Residual current $I_{in} - I_{load}$ is shunt
- While $I_{load} < I_{in}$ the system is seen by the power supply as a constant load $\Longrightarrow$ crucial for a serially powered system

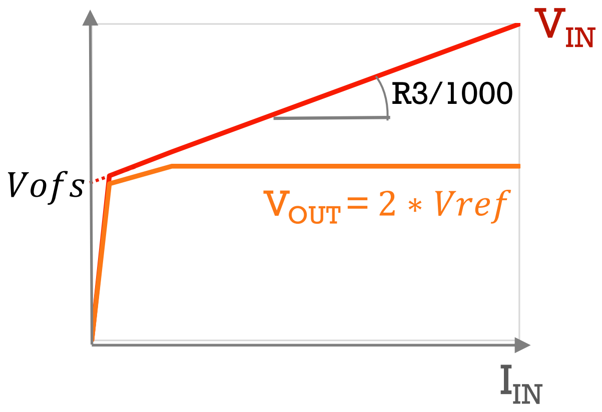
SLDO – some more detail

- Voltage divider + A1-M1 complex ensure $V_{DD} = 2V_{ref}$
- $V_{in} \gtrsim V_{DD} + 0.2V$ needed



- Shunt determines how chip is seen by PS
- $V_{in} = V_{ofs} + \frac{R_3}{1000} I_{in} \equiv V_{ofs} + R_{eff} \cdot I_{in}$
- Power supply sees a constant load
- Independent form power consumption as long as $I_{load} < I_{in}$





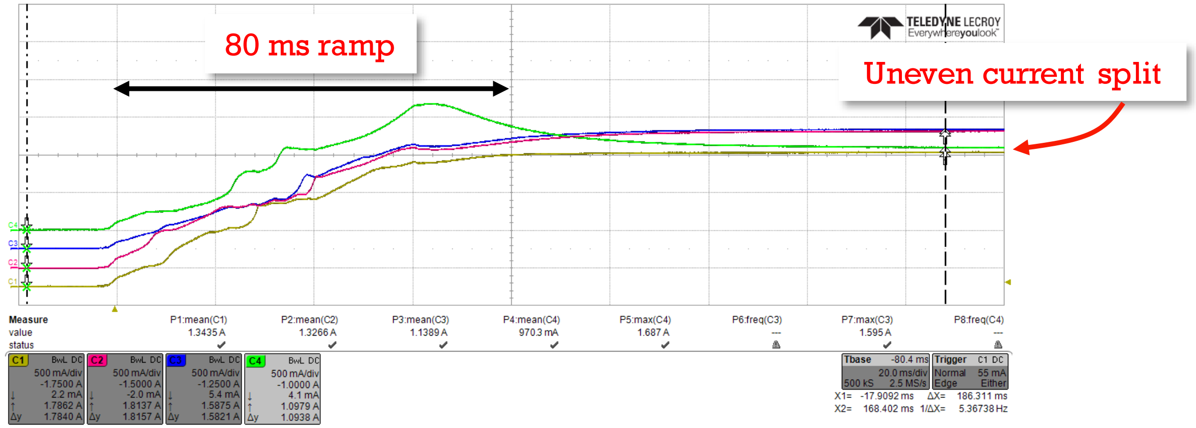
Known Issues and challenges of the system

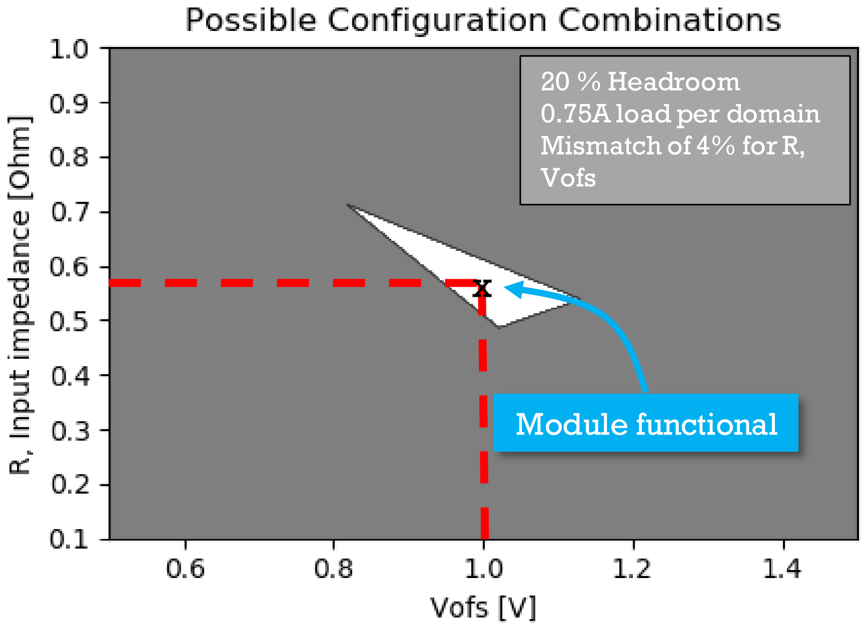
RD53A SLDO

Current sharing and headroom

Current sharing between chips in same module not trivial

- Chips in same module powered in parallel
- Current split determined by V_{ofs}, R_{eff} of each SLDO, startup
- Measured on 4 RD53As in parallel powered with current source



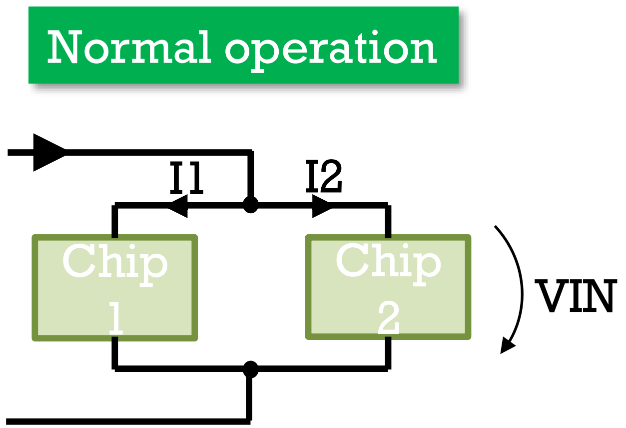


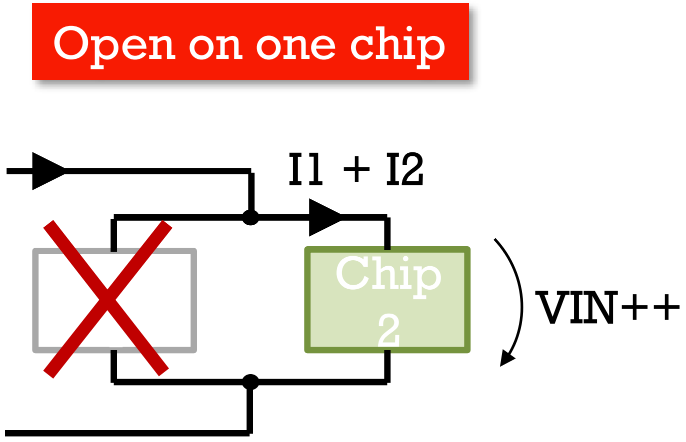
Headroom optimization

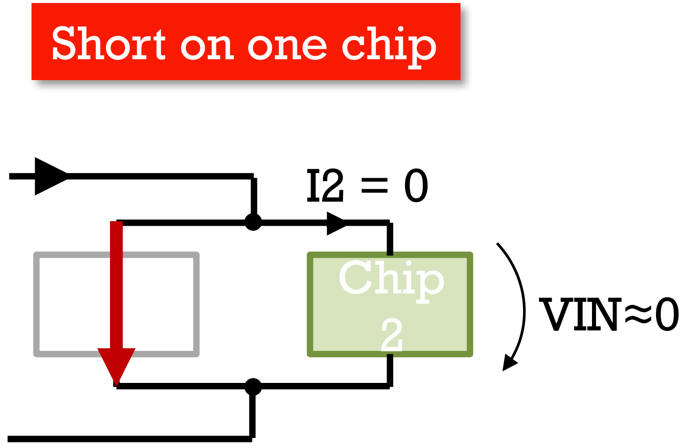
- A headroom is provided, i.e. $I_{in} = I_{load}^{max} + I_{headroom}$
- Covers potential current consumption spikes
- Accounts for mismatch in V_{ofs}, R_{eff} between chips

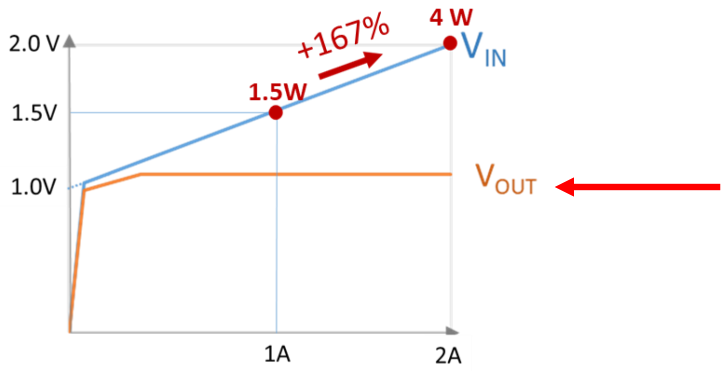
First studies indicate 20% headroom can cover estimated mismatches

Basic failure scenarios









Open on one chip:

- Remaining chip must take full current
- Power burnt on chip strongly increases
- Operational margin limited by thermal issues and input voltage
- Other modules can operate

Short on one chip:

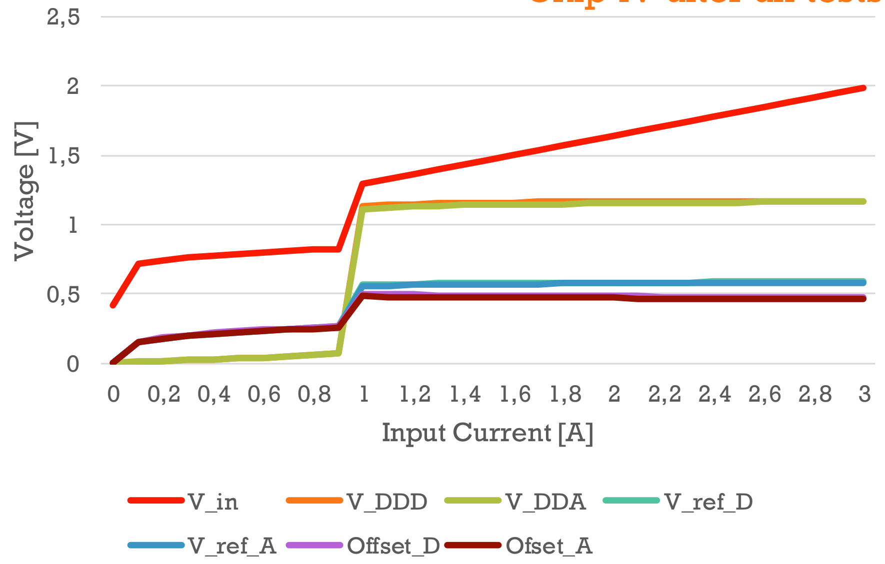
- Module completely looses functionality
- Other modules in the chain can operate

Stress tests

Design limits:
- 4A, 2V max

Tests have been performed stressing SLDO system on the RD53A chip
- 4.5A, 1.8V (high current) for a week (with cooling)
- 5A, 1.9V (high current) for a week (with cooling)
- 1.8A, 2.2V (high voltage) for a week
- 130000 continuous power cycles at nominal operating point
- One week at nominal operation with 1/4 of wire bonds carrying I_{in} removed
- 3 days at 4.5A with removed wire bonds (with cooling)

Chip IV after all tests



No anomalous behavior observed

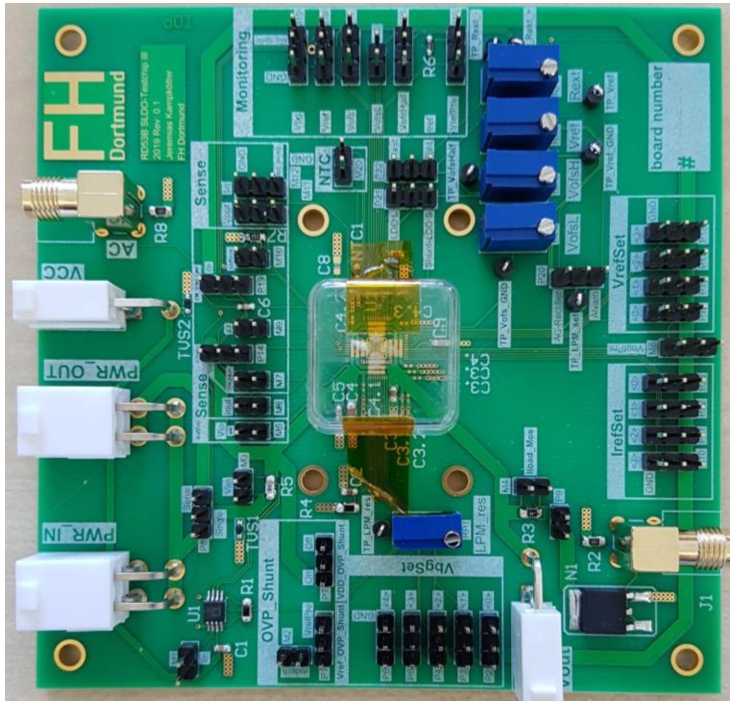
✓ SLDO design appears sturdy

✗ No info on possible failure modes

Improvements over RD53A SLDO

The SLDO test chip version C

- New standalone test chip for shunt LDO available in summer 2019
- Includes many improvements w.r.t. RD53A SLDO



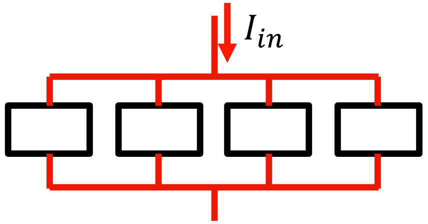
Undershunt protection
- If $I_{load} > I_{in}$ on one chip the regulator fails and the voltage across the module collapses $\Longrightarrow$ whole chain affected
- To prevent this, dedicated circuitry reduces V_{out} in case I_{shunt} gets too low

Improved startup behavior
- Common bandgap regulator for Analog/Digital SLDOs
- Dedicated startup circuit allows for much improved behavior

Overvoltage protection
- Voltage clamp to avoid exceeding 2V input
- Cut off voltage can be set

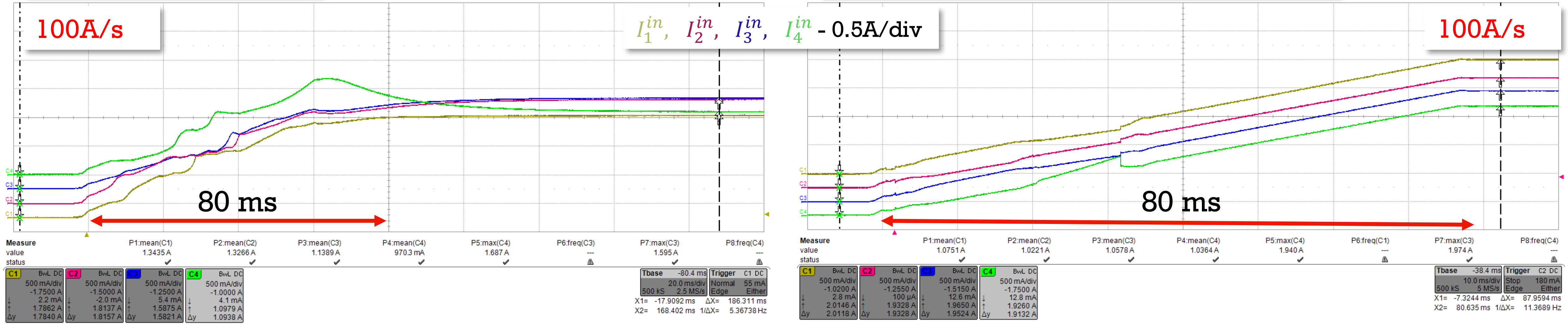
Dynamic startup behavior

- 4 RD53A chips (i.e. 8 SLDOs) in parallel to emulate quad module
- Current source with 100A/s ramp



RD53A internal SLDOs

RD53As powered with SLDO test chips C



Startup behavior shows great improvement, better current sharing

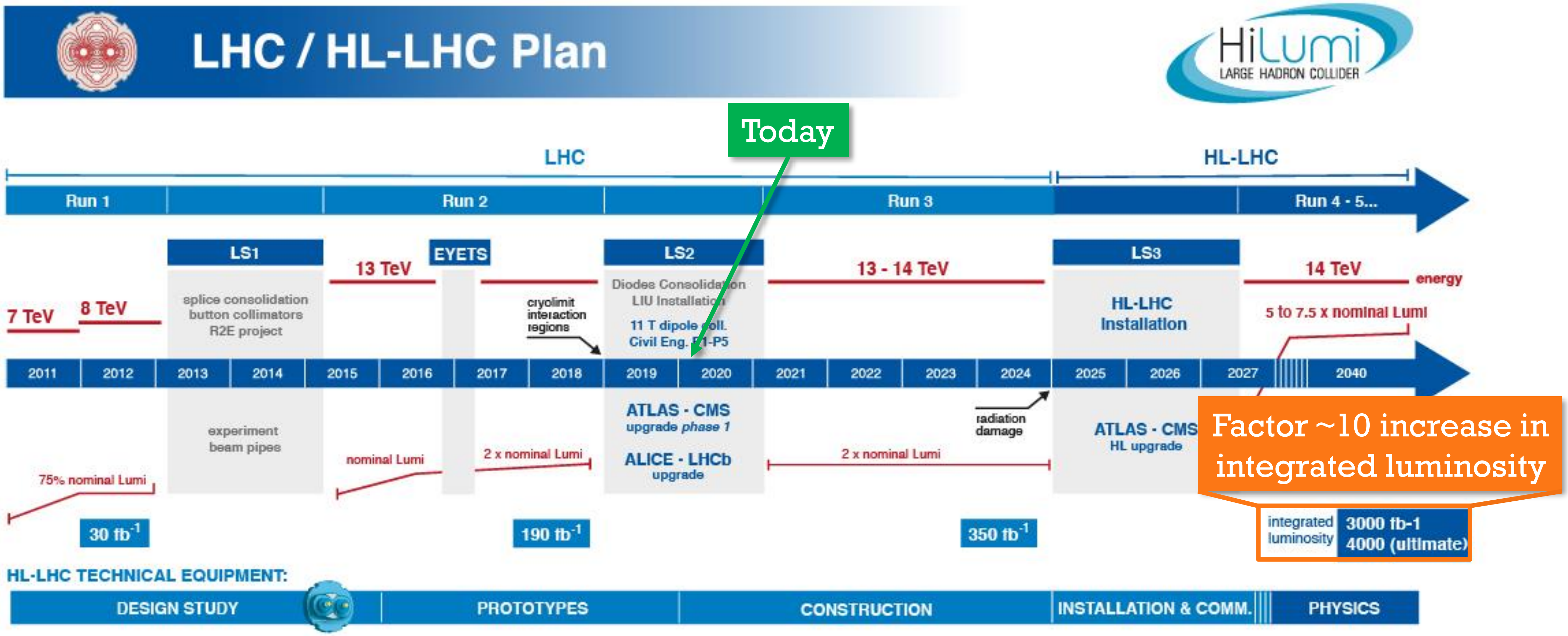
Conclusions

- Serial powering concept proven to be reliable
- Allows to meet the powering challenges faced by the CMS Phase II pixel tracker
- Many tests have been performed and more are ongoing
- Further improvements w.r.t. RD53A have been implemented and tested in dedicated SLDO test chips
- Quad RD53A modules (with and without sensors) are now available for testing
- RD53B-based CMS-ROC will be available in late 2020
- More studies to be done on the optimization of working points and headroom

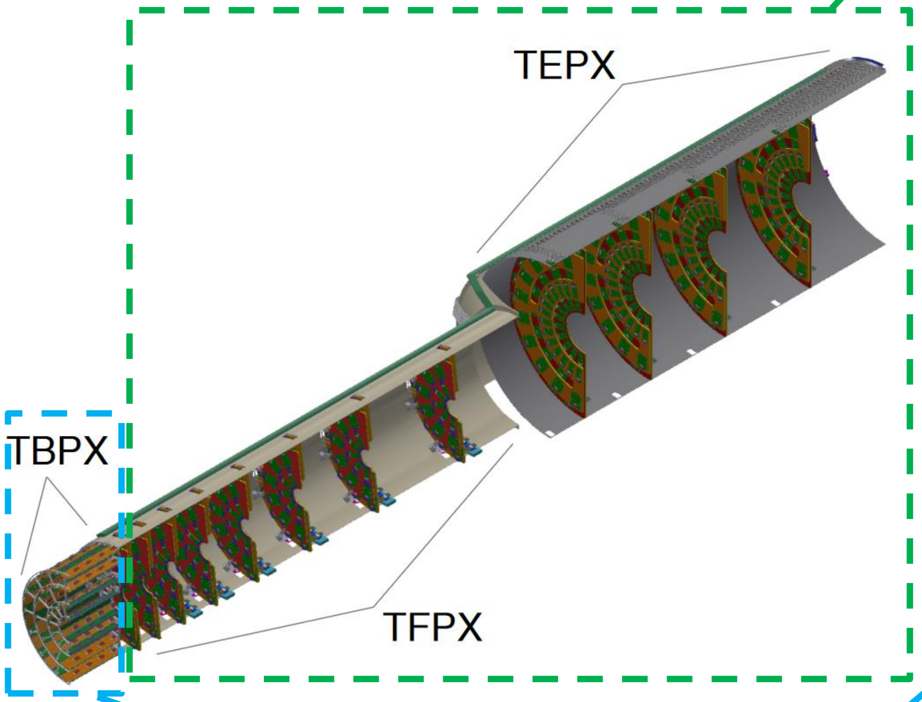
Thank you for your attention

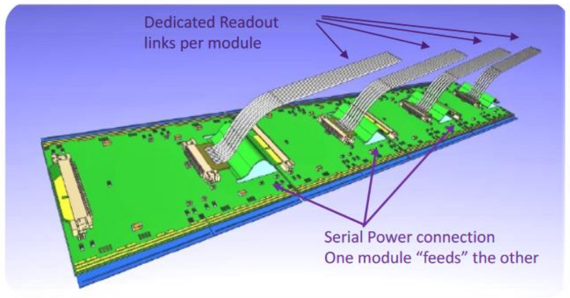
Many thanks to D. Koukola, S. Orfanelli, G. Sguazzoni, S. Paoletti, M. Meschini, A. Cassese
and the whole CMS-IT crew

The HL-HLC update plan

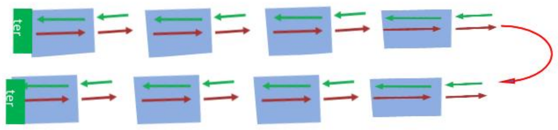


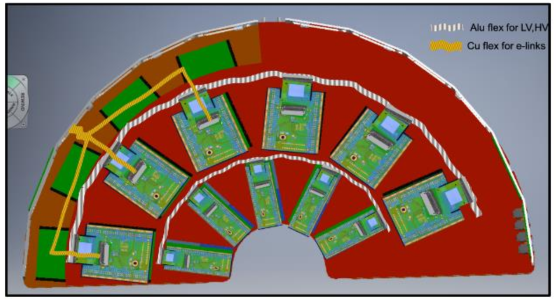
Chain topologies



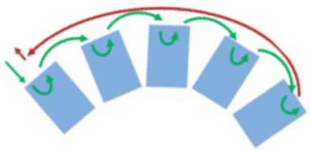


TBPX: 1 chain for 2 consecutive ladders in Phi



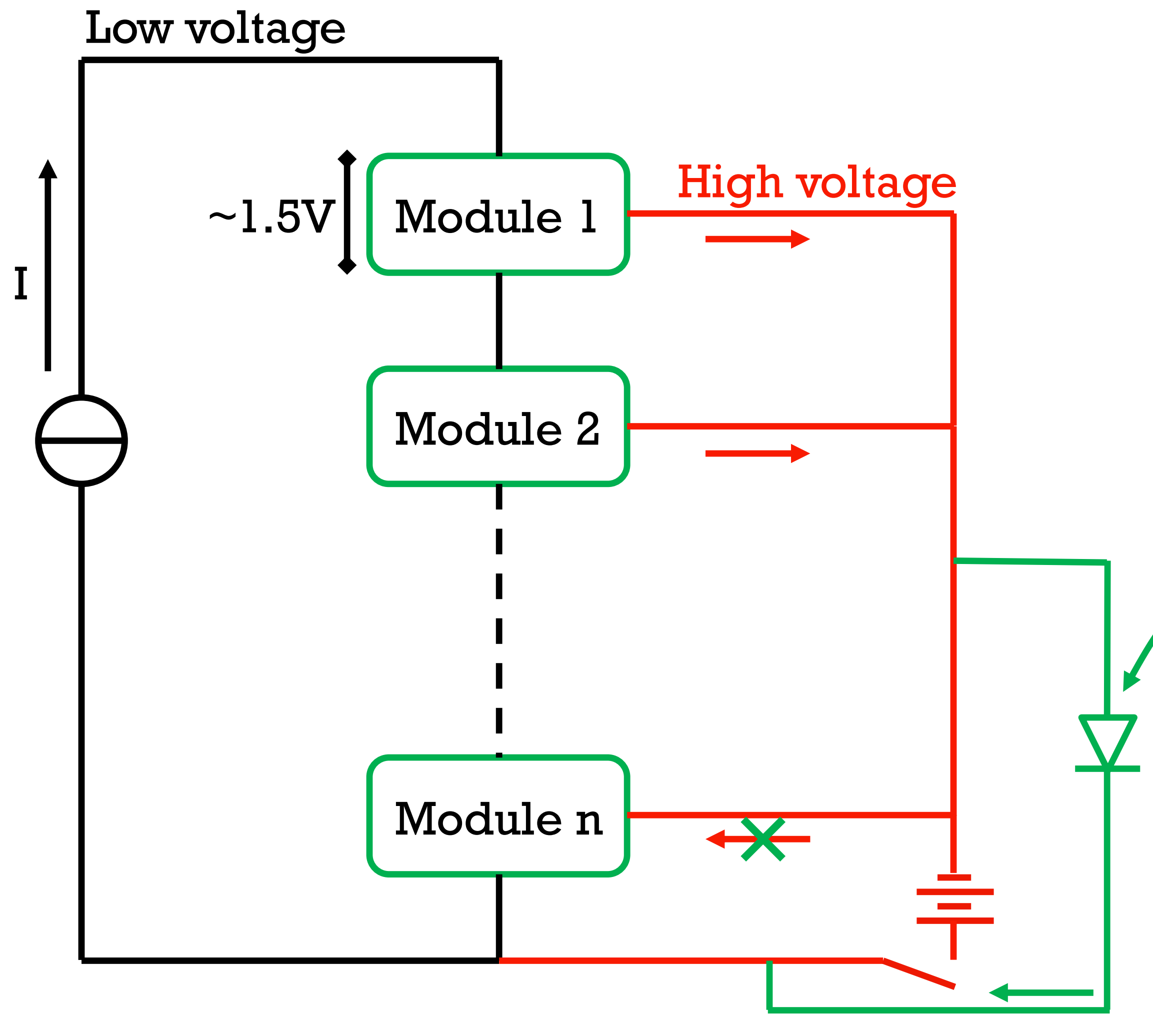


TFPX/TEPX: 1 chain per ring



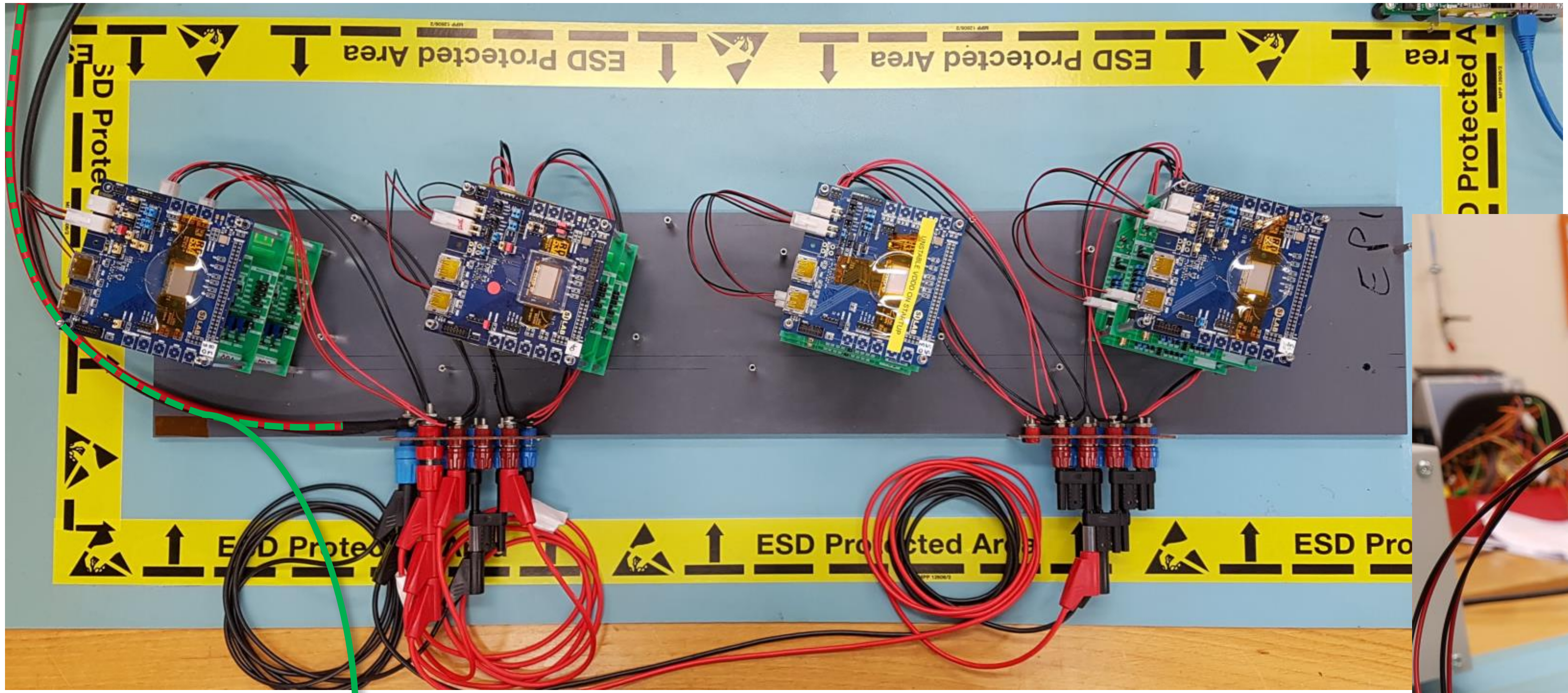
Up to 12 modules per chain

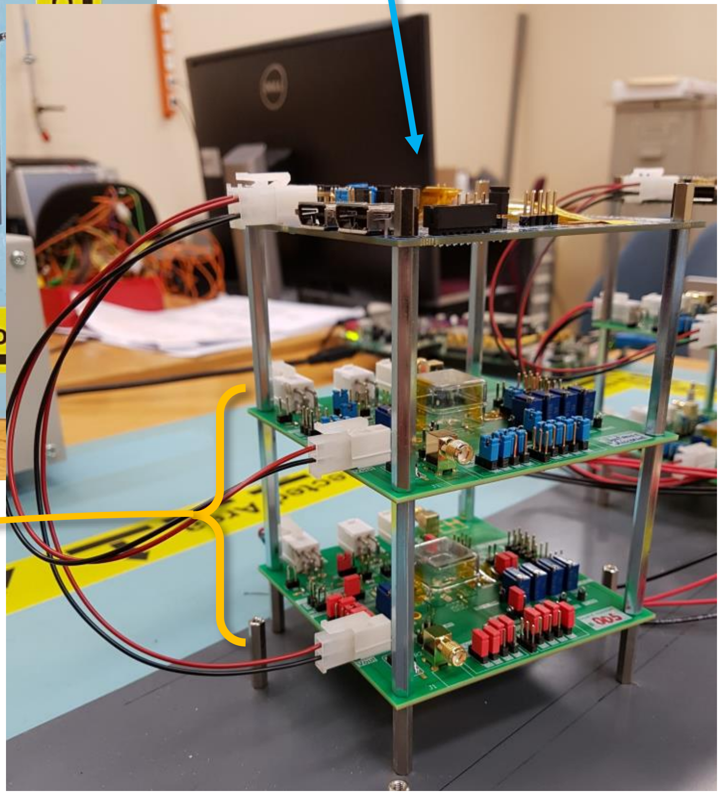
Potential issue with HV



- An issue may arise when HV is off and LV is on
- If HV PS has high ohmic behavior in its off state, difference in local grounds causes leakage currents to flow in downstream module
- Sensor becomes forward biased
- Solved bypassing the HV PS with a diode and/or crowbar

RD53A with SLDOc setup



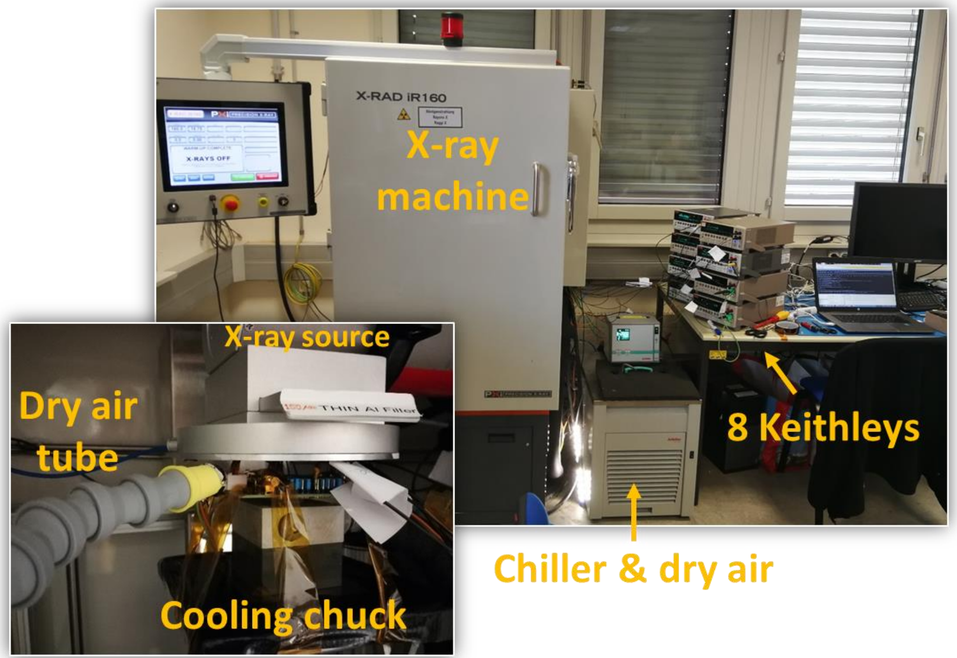


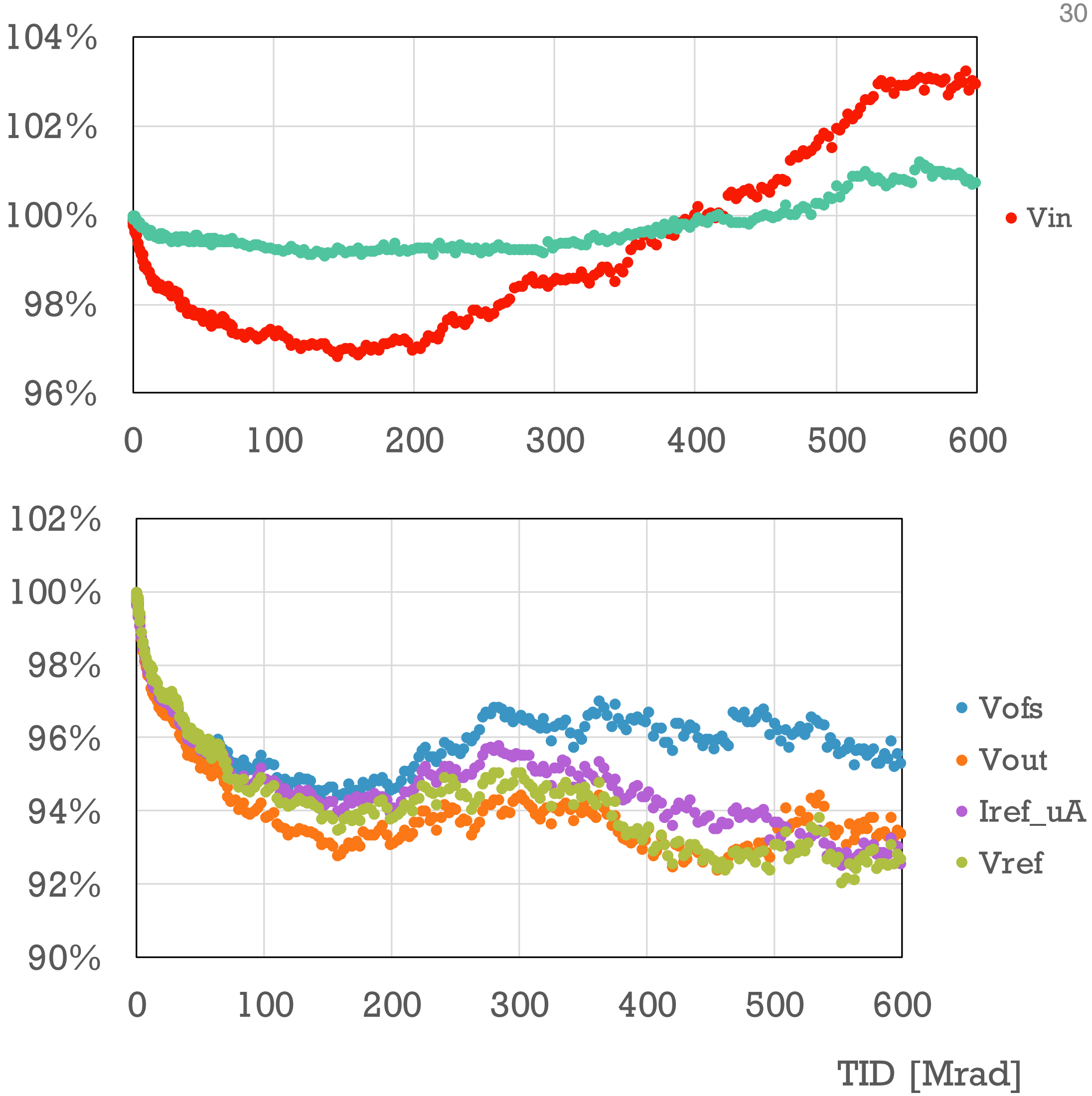
RD53A SCC

Input from current source

Two SLDO test chips power each RD53A
(one each for analog/digital domains)

Irradiation campaign

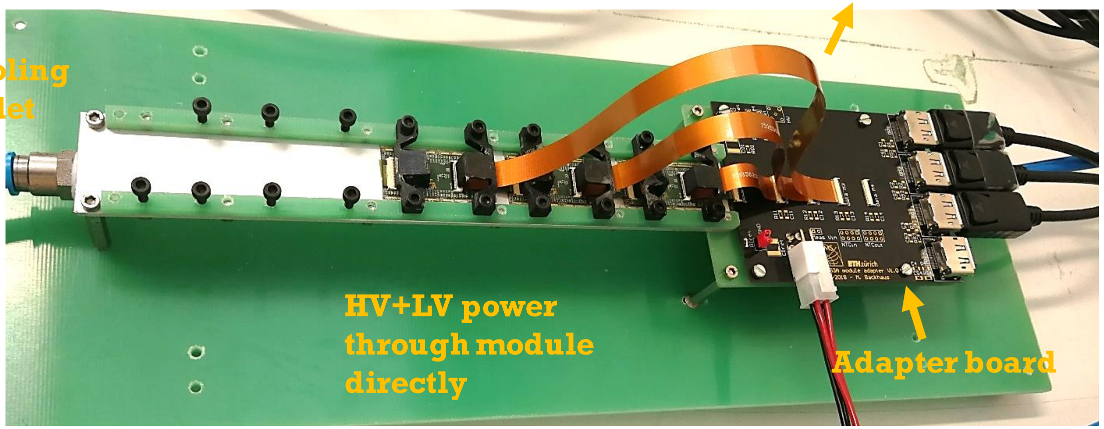


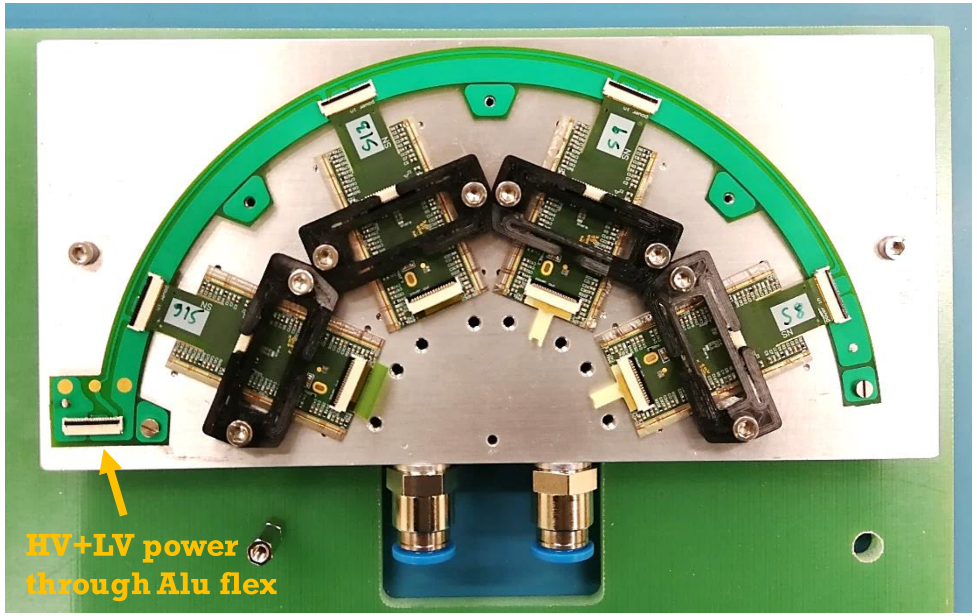


Shunt-LDO is fully functional after 600Mrad at 0C:

- Output behavior is very stable
- Some variations of input behavior
- Reference voltages change due to internal resistor
  - Improved design in RD53B

Detector-like structure tests





Cooling in- and outlet

(Elinks and readout board not shown)

- Electrical connections similar to final detector
- Aluminum structure with water cooling pipe inside
- Cooling is essential: ~10 W per module are dissipated