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Serial powering at CMS silicon tracker detector for High Luminosity Upgrade

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The LHC machine will be upgraded targeting a peak luminosity of $5-7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and aiming to collect an integrated luminosity of $3000 - 4500 \text{ fb}^{-1}$ in 10 years. The Compact Muon Solenoid (CMS) silicon tracker (Inner Tracker, IT) will be replaced at the High Luminosity Large Hadron Collider (HL-LHC) upgrade by a new radiation-hard detector capable of handling higher pileup, higher data rates, and longer trigger latency. RD53A prototype chip in a 65 nm feature size CMOS technology has been developed by RD53 Collaboration to meet these requirements. Meeting the performance specifications requires higher granularity which leads to a higher power consumption. In addition, the smaller feature size leads to lower operating voltage, thus further increasing the current. This cannot be satisfied with the current parallel powering scheme, without significantly increasing the cable mass. Therefore a serial powering scheme will be used. Chains of up to 12 modules will be powered by a constant current generator while the necessary internal rails will be provided by the special on-chip voltage regulators called Shunt Low Drop-Out (SLDO) regulators. The SLDO regulator also ensures that the chip sinks a constant input current independent of the internal circuit consumption. In addition, this scheme is less susceptible to voltage transients and noise, while improving the powering efficiency. Two or four chips on each module are powered in parallel to prevent a single failure from compromising the chain. Powering specification review is ongoing: many tests have been performed and will be presented.

Primary author: COLLABORATION, CMS

Presenter: SEIDITA, Roberto (Universita e INFN, Firenze (IT))

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