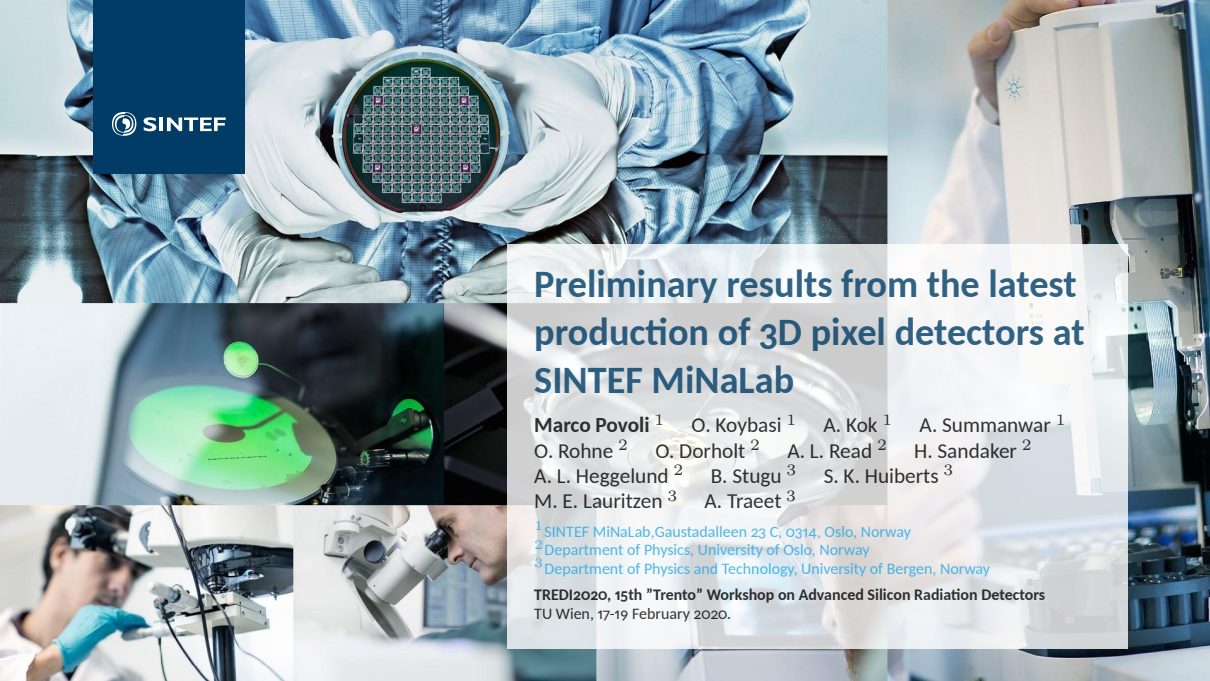

Preliminary results from the latest production of 3D pixel detectors at SINTEF MiNaLab

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M. E. Lauritzen [3] A. Traeet [3]

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TREDI2020, 15th "Trento" Workshop on Advanced Silicon Radiation Detectors
TU Wien, 17-19 February 2020.

Outline

1. Introduction
2. Electrical tests results on temporary metal
   - Full batch yield
   - Planar test structures
   - 3D test structures
   - 3D pixel detectors
   - Effect of sintering
3. Lessons learned
   - Lithography accuracy
   - Deep Reactive Ion Etching - DRIE
   - Wafer bowing/warping
4. Conclusion and future plans

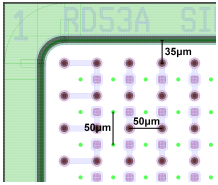
Recent history of 3D technology at SINTEF

Year	Project	Wafer type	Active thickness [µm]	Electrode diameter [µm]	Remarks
2006	Run1	4" SOI	230	15	N-type, low mechanical yield
2008	Run2	4" SOI	230	15	50% yield (roughly)
2010	Run3	4" SOI	230	15	Low yield (2 out of 24 wafers ok)
2018	Run4*	6" Si-Si	50 & 100	4	Very good yield (FE-I4)
2019	**Run5***	**6" Si-Si**	**150**	**6**	**Completed January 2020 OK yield (RD53 A/B)**
2020	Run6*	6" Si-Si	150	6	In the planning phase… Start in 2020.

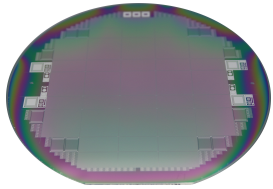
***funded by Norwegian ATLAS R&D**

Forskningsrådet

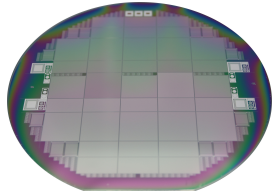
Fabricated wafers

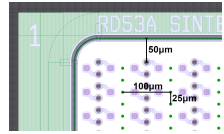


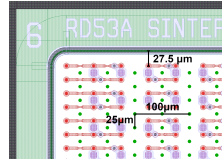
Layout1 - 50x50



Layout2 - 25x100





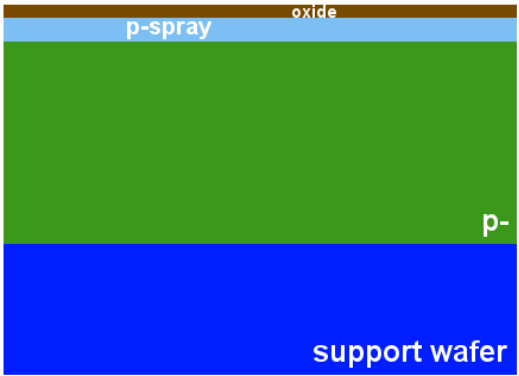


- 24 wafers, 6” Si-Si p-type (**150μm active**)
- **Active-edge** (3μm wide), **3D electrodes** (6μm diameter)
- Depth: N-type electrodes **115μm**, P-type electrode **150μm**
- All processing steps in-house except the **p-spray** implant
- Layout by University of Oslo

	Layout 1	Number per wafer	Layout 2	Number per wafer	TOTAL Layout1	TOTAL Layout2
Planar with Active-Edge	100µm edge	3	100µm edge	3	36	36
3D DIODES	50x50	246	25x100	123 (1E) 123 (2E)	2952	1476 (1E) 1476 (2E)
FE-I4			50x250	3		36
RD53A	50x50	22	25x100	11 (1E) 11 (2E)	264	132 (1E) 132 (1E)
RD53B	50x50	15	25x100	6 (1E) 6 (2E)	180	72 (1E) 72 (2E)
STRIP	50x50	12	25x100	6 (1E) 6 (2E)	144	72 (1E) 72 (2E)

3D RUN5 - Fabrication process

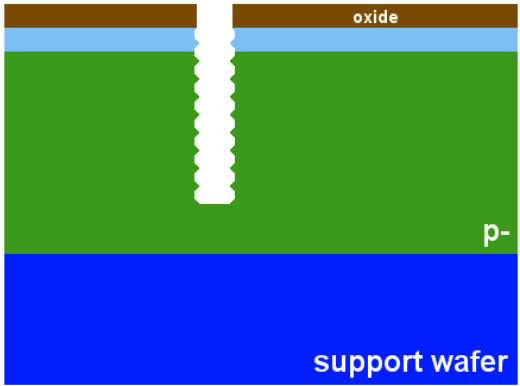
1. P-spray implantation + oxidation



3D RUN5 - Fabrication process

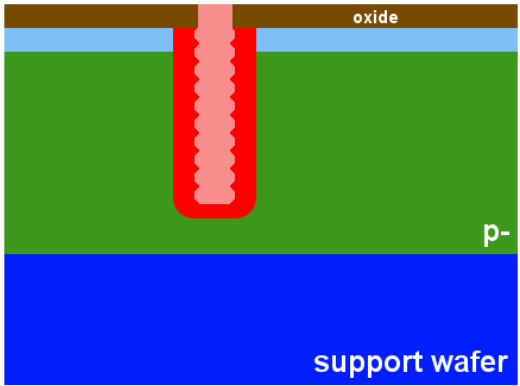
1. P-spray implantation + oxidation
2. Etching mask for DRIE (aluminium)

3D RUN5 - Fabrication process



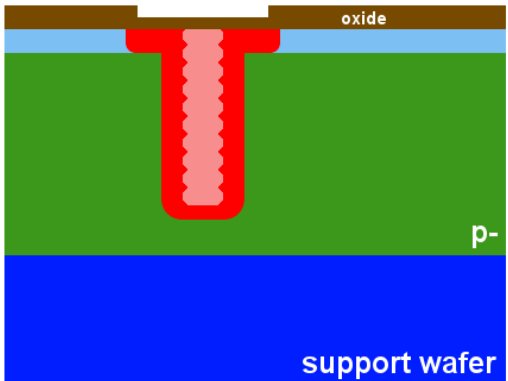
1. P-spray implantation + oxidation
2. Etching mask for DRIE (aluminium)
3. DRIE of n+ columns

3D RUN5 - Fabrication process



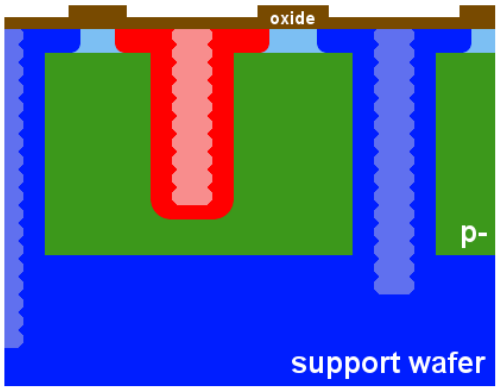
1. P-spray implantation + oxidation
2. Etching mask for DRIE (aluminium)
3. DRIE of n+ columns
4. Phosphorus doping and poly filling

3D RUN5 - Fabrication process



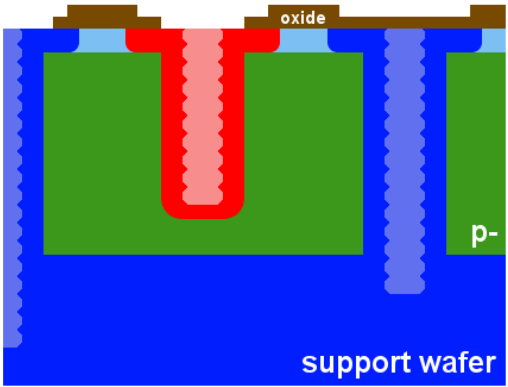
1. P-spray implantation + oxidation
2. Etching mask for DRIE (aluminium)
3. DRIE of n+ columns
4. Phosphorus doping and poly filling
5. Planar n+ doping

3D RUN5 - Fabrication process



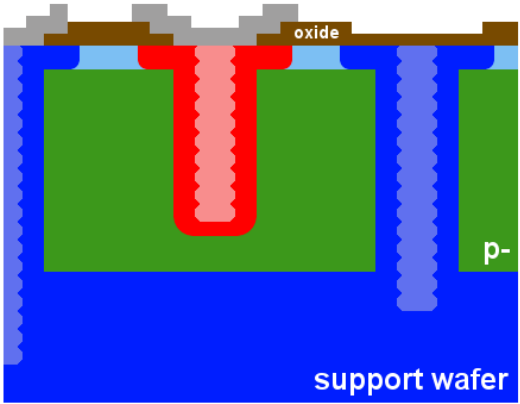
1. P-spray implantation + oxidation
2. Etching mask for DRIE (aluminium)
3. DRIE of n+ columns
4. Phosphorus doping and poly filling
5. Planar n+ doping
6. Repeat **<2-5>** for p+ columns/trenches (Boron)

3D RUN5 - Fabrication process



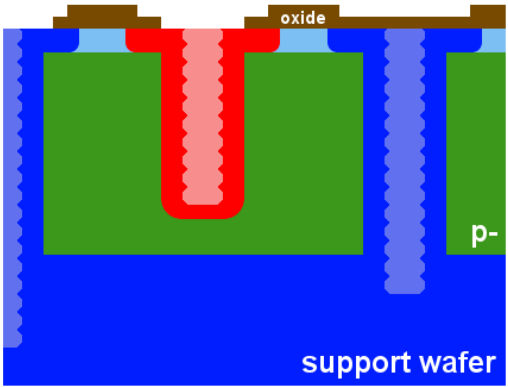
1. P-spray implantation + oxidation
2. Etching mask for DRIE (aluminium)
3. DRIE of n+ columns
4. Phosphorus doping and poly filling
5. Planar n+ doping
6. Repeat **<2-5>** for p+ columns/trenches (Boron)
7. Contact opening

3D RUN5 - Fabrication process



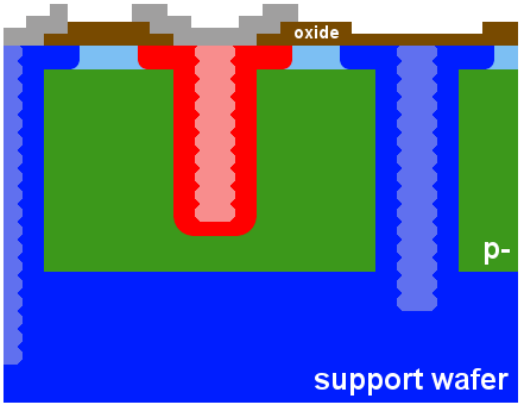
1. P-spray implantation + oxidation
2. Etching mask for DRIE (aluminium)
3. DRIE of n+ columns
4. Phosphorus doping and poly filling
5. Planar n+ doping
6. Repeat **<2-5>** for p+ columns/trenches (Boron)
7. Contact opening
8. Temporary metal deposition and patterning
9. **TEMP METAL MEASUREMENTS**

3D RUN5 - Fabrication process



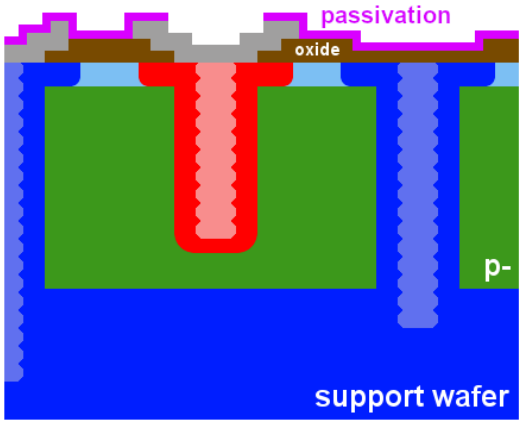
1. P-spray implantation + oxidation
2. Etching mask for DRIE (aluminium)
3. DRIE of n+ columns
4. Phosphorus doping and poly filling
5. Planar n+ doping
6. Repeat **<2-5>** for p+ columns/trenches (Boron)
7. Contact opening
8. Temporary metal deposition and patterning
9. **TEMP METAL MEASUREMENTS**
10. Temporary metal removal and cleaning

3D RUN5 - Fabrication process



1. P-spray implantation + oxidation
2. Etching mask for DRIE (aluminium)
3. DRIE of n+ columns
4. Phosphorus doping and poly filling
5. Planar n+ doping
6. Repeat **<2-5>** for p+ columns/trenches (Boron)
7. Contact opening
8. Temporary metal deposition and patterning
9. **TEMP METAL MEASUREMENTS**
10. Temporary metal removal and cleaning
11. Final metal deposition, patterning and **sintering**

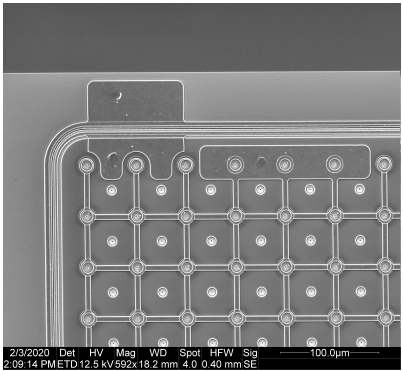
3D RUN5 - Fabrication process

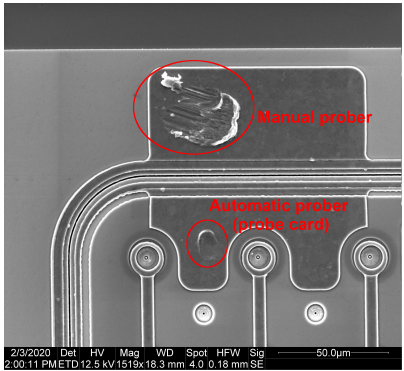


1. P-spray implantation + oxidation
2. Etching mask for DRIE (aluminium)
3. DRIE of n+ columns
4. Phosphorus doping and poly filling
5. Planar n+ doping
6. Repeat **<2-5>** for p+ columns/trenches (Boron)
7. Contact opening
8. Temporary metal deposition and patterning
9. **TEMP METAL MEASUREMENTS**
10. Temporary metal removal and cleaning
11. Final metal deposition, patterning and **sintering**
12. Passivation deposition and patterning
13. Final baking if necessary

→ **60 main steps! 10 months of net processing**

Temporary metal test results





3D RUN5 - Fabrication YIELD

RD53 pixel detectors MEASURED BEFORE SINTERING

LAYOUT1

WAFER	Thickness	SENSOR TYPE	# of sensors	YIELD SOFT	YIELD VERY SOFT
F1	450	RD53A	22	27.27 %	45.45 %
		RD53B	15	13.33 %	13.33 %
F2	450	RD53A	22	45.45 %	59.09 %
		RD53B	15	20.00 %	33.33 %
F3	450	RD53A	22	50.00 %	59.09 %
		RD53B	15	20.00 %	26.67 %
F4	450	RD53A	22	63.64 %	63.64 %
		RD53B	15	13.33 %	26.67 %
F5	450	RD53A	22	63.64 %	77.27 %
		RD53B	15	53.33 %	73.33 %
F6	450	RD53A	22	50.00 %	81.82 %
		RD53B	15	33.33 %	60.00 %
F7	450	RD53A	22	59.09 %	72.73 %
		RD53B	15	20.00 %	33.33 %
F16	650	RD53A	22	31.82 %	40.91 %
		RD53B	15	6.67 %	20.00 %
F17	650	RD53A	22	50.00 %	63.64 %
		RD53B	15	26.67 %	53.33 %
F18	650	RD53A	22	27.27 %	63.64 %
		RD53B	15	33.33 %	53.33 %
F19	650	RD53A	22	50.00 %	81.82 %
		RD53B	15	0.00 %	20.00 %
F20	650	RD53A	22	40.91 %	59.09 %
		RD53B	15	6.67 %	13.33 %

RD53A TOT.	264	46.59 %	64.02 %
RD53B TOT.	180	20.56 %	35.56 %
TOTAL	444	36.04 %	52.48 %

LAYOUT 2 - RD53A 1E vs 2E

WAFER	Thickness	SENSOR TYPE	# of sensors	YIELD SOFT	YIELD VERY SOFT
F8	450	RD53A (1E)	11	73 %	100 %
		RD53A (2E)	11	0 %	9 %
F9	450	RD53A (1E)	11	64 %	91 %
		RD53A (2E)	11	0 %	27 %
F10	450	RD53A (1E)	11	55 %	100 %
		RD53A (2E)	11	18 %	36 %
F11	450	RD53A (1E)	11	73 %	100 %
		RD53A (2E)	11	0 %	18 %
F12	450	RD53A (1E)	0		
		RD53A (2E)	0		
F13	450	RD53A (1E)	0		
		RD53A (2E)	0		
F14	450	RD53A (1E)	11	36 %	64 %
		RD53A (2E)	11	18 %	36 %
F15	450	RD53A (1E)	11	82 %	100 %
		RD53A (2E)	11	36 %	55 %
F21	650	RD53A (1E)	11	64 %	82 %
		RD53A (2E)	11	18 %	55 %
F22	650	RD53A (1E)	11	45 %	73 %
		RD53A (2E)	11	0 %	18 %
F23	650	RD53A (1E)	11	55 %	82 %
		RD53A (2E)	11	9 %	27 %
F24	650	RD53A (1E)	11	100 %	100 %
		RD53A (2E)	11	36 %	55 %

[1E] TOT.	110	65 %	89 %
[2E] TOT.	110	14 %	34 %
TOTAL	220	39 %	61 %

LAYOUT 2 - RD53B 1E vs 2E

WAFER	Thickness	SENSOR TYPE	# of sensors	YIELD SOFT	YIELD VERY SOFT
F8	450	RD53B (1E)	6	50 %	50 %
		RD53B (2E)	6	0 %	17 %
F9	450	RD53B (1E)	6	67 %	67 %
		RD53B (2E)	6	50 %	50 %
F10	450	RD53B (1E)	6	0 %	67 %
		RD53B (2E)	6	0 %	17 %
F11	450	RD53B (1E)	6	33 %	67 %
		RD53B (2E)	6	17 %	17 %
F12	450	RD53B (1E)	0		
		RD53B (2E)	0		
F13	450	RD53B (1E)	0		
		RD53B (2E)	0		
F14	450	RD53B (1E)	6	17 %	83 %
		RD53B (2E)	6	17 %	17 %
F15	450	RD53B (1E)	6	83 %	83 %
		RD53B (2E)	6	17 %	17 %
F21	650	RD53B (1E)	6	33 %	33 %
		RD53B (2E)	6	0 %	17 %
F22	650	RD53B (1E)	6	17 %	50 %
		RD53B (2E)	6	0 %	0 %
F23	650	RD53B (1E)	6	33 %	83 %
		RD53B (2E)	6	0 %	0 %
F24	650	RD53B (1E)	6	17 %	67 %
		RD53B (2E)	6	0 %	17 %

[1E] TOT.	60	35 %	65 %
[2E] TOT.	60	10 %	17 %
TOTAL	120	23 %	41 %

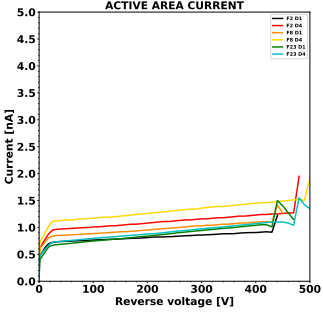
- **RD53A - 50x50:** 47%
- **RD53B - 50x50:** 21%

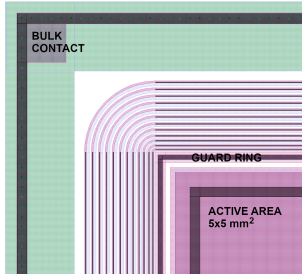
- **RD53A - 25x100:** [1E] 65% - [2E] 14%
- **RD53B - 25x100:** [1E] 45% - [2E] 10%

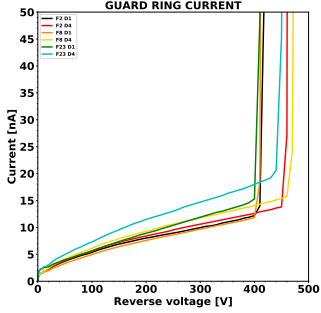
AUTOMATIC SENSOR SELECTION: Must have close to flat current and breakdown past 20V of bias
"YIELD VERY SOFT": Includes some sensors that could become either good or bad after sintering and passivation

I-V of planar test diodes

Measured before sintering

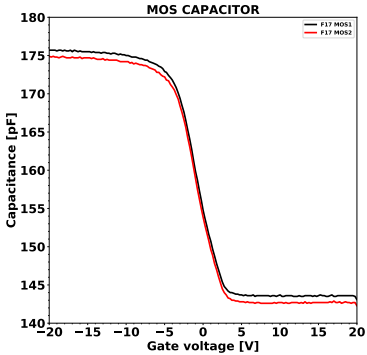


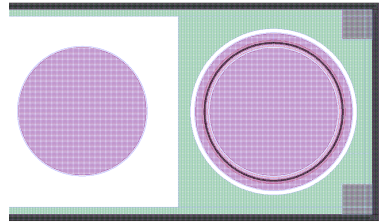




- Current saturates and does not show early rise before breakdown
- Breakdown voltages around **500 V**, as expected for planar diodes with p-spray
- Average current value **before sintering** equal to **970 pA**
- Corresponding to life times of roughly **6 ms**
- Considerable improvement expected after sintering

MOS Capacitor C-V
Only reliable AFTER sintering

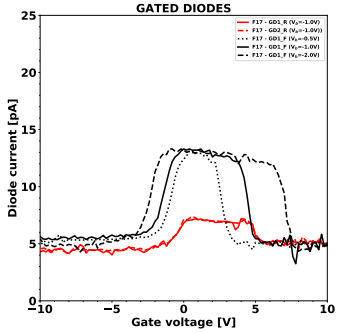




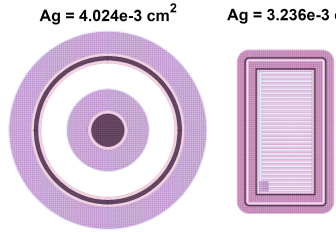
AREA [cm^{-2}]	$T_{OX}[nm]$	V_{FB} [V]	Q_{OX} [cm^{-2}]
0.035	691	2.146	9.28×10^{10}

- Field Oxide thickness in agreement with what measured by the ellipsometer
- Oxide charge value in agreement with expectations
- Final oxide charge might vary slightly after passivation

Gated Diode
Only reliable AFTER sintering



- Preliminary analysis suggests very low surface recombination velocity
- Large influence of the applied bias (expected)
- Requires further analysis
  [G. Verzellesi et al., IEEE TNS, Vol.46, no.4, Apr. 1999]



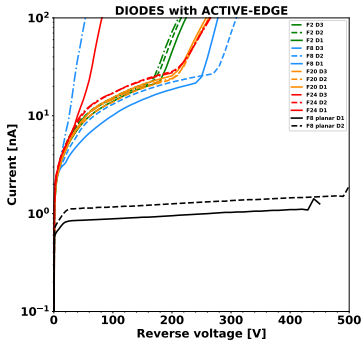
Diode type	A_g [cm^2]	I_{surf} [A]	s_0 [cm/s]
Round	4.024×10^{-3}	1.84×10^{-12}	0.29
Finger	3.236×10^{-3}	8.32×10^{-12}	1.61

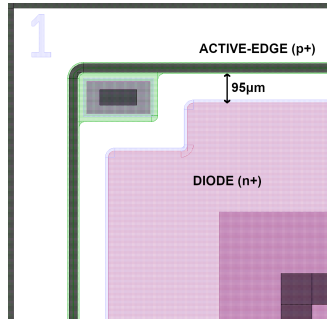
$$I_{surf} = I_{depl} - I_{inv}$$

$$s_0 = \frac{I_{surf}}{q n_i A_g}$$

ACTIVE-EDGE planar diodes

Measured before sintering

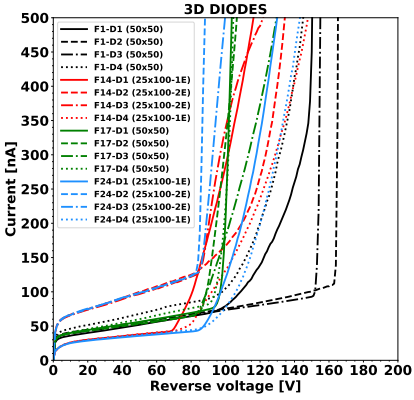


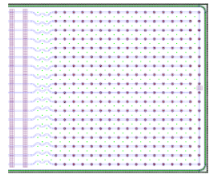


- The current saturates less than in the regular diodes (p-spray/ n+-p+ distance)
- Breakdown voltages around **250 V**, as expected for active-edge diodes with p-spray
- Average current value **before sintering** equal to **15 nA** at **100V**
- Considerable improvement expected after sintering (roughly 15-20 times lower)

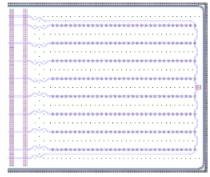
3D DIODES (all layouts)

Measured before sintering

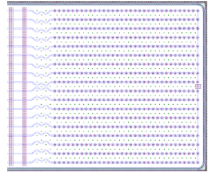




LAYOUT1
50x50 - 1E
(306 n+ col.)



LAYOUT2
25x100 - 1E
(264 n+ col.)

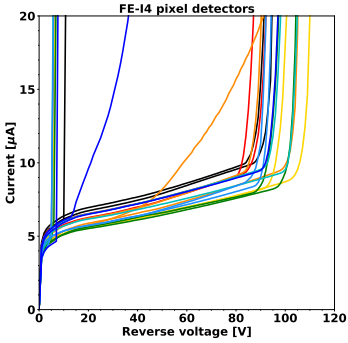


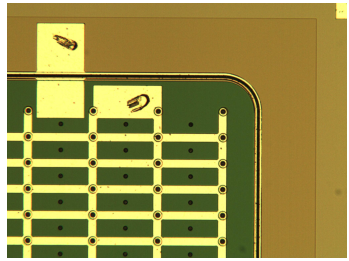
LAYOUT2
25x100 - 2E
(594 n+ col.)

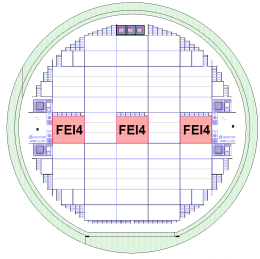
- Current related to the number of columns (**100-200 pA/col.**)
- There is a large surface contribution (p-spray / short pitch)
- Breakdown high but with large spread

FE-I4 pixel detectors (50x250 - 2E)

Measured before sintering



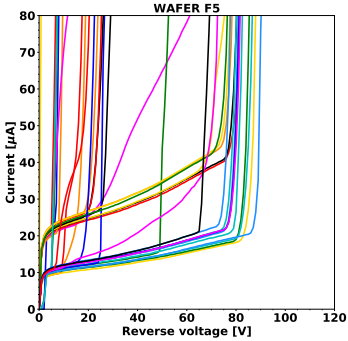


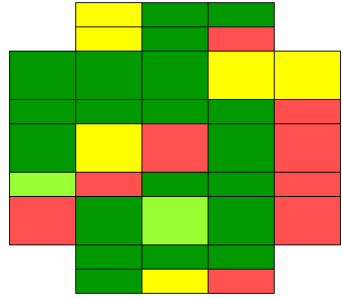


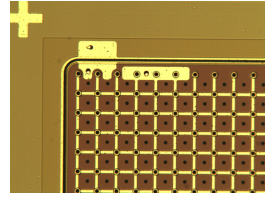
- **Yield 63%** (19 good sensors out of 30)
- Early current saturation and high breakdown
- Overall good uniformity
- Active-edge distance to last n+ column 67.5μm

RD53A and RD53B pixels (LAYOUT1 - 50x50)

Measured before sintering



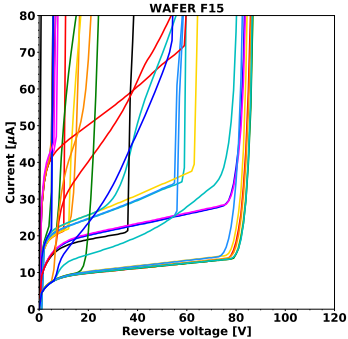


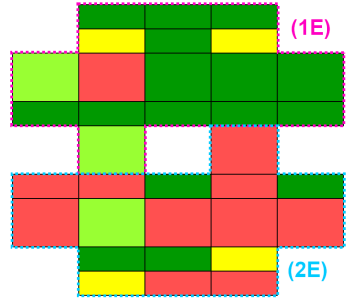


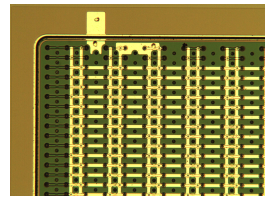
- **RD53A: Yield 64%** (14 out of 22, green and light green)
- **RD53B: Yield 53%** (8 out of 15, green and light green)
- Clear difference in current between RD53A and RD53B (sensor size)
- Active-edge at 35μm from last n+ column (**very close!**)

RD53A and RD53B pixels (LAYOUT2 - 25x100 - 1E/2E)

Measured before sintering

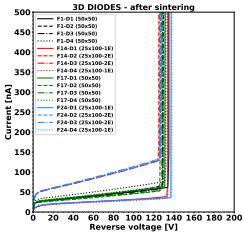


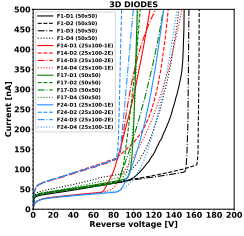




- **YIELD ⇒ RD53A: [1E → 82%] / [2E → 36%]**
- **YIELD ⇒ RD53B: [1E → 83%] / [2E → 17%]**
- Not enough RD53B for reliable yield calculation per wafer
- Active edge distance: 50μm (1E), 27.5μm (2E)

Effect of Sintering on I-V curves (1)



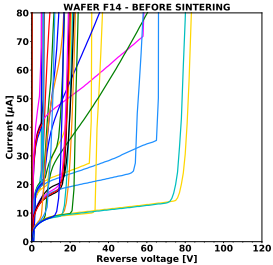


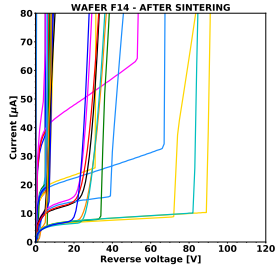
DEVICE TYPE	RUN	Thickness	BEFORE [uA/cm2]	AFTER [uA/cm2]	Improvement factor	Comment
Planar ActiveEdge	5	150	1.171E-02	7.106E-04	16.477	
FE-I4 pixel	5	150	1.892	0.578	3.270	
3D DIODE (50x50)	5	150	6.106	4.209	1.451	
RD53A (50x50)	5	150	7.744	5.816	1.332	
RD53A (25x100 1E)	5	150	6.935	3.796	1.827	
RD53A (25x100 2E)	5	150	13.122	12.110	1.084	
FE-I4 pixel	4	100	0.909	0.026	34.323	SINTERED AND BUMP BONDED
3D DIODE (50x50)	4	100	258.500	8.733	29.602	

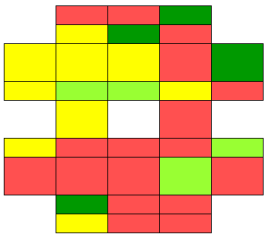
- Sintering done at **350°C**
- On good devices, it **reduces surface current** and **improves the breakdown**
- Lower density of 3D structures results in a **larger improvement** after sintering
- Similar performances for 3D detectors with **50x50** or **25x100** pitch in **1E** configuration
- Comparison with the previous run shows that **results are similar or better**
- FE-I4 pixel detectors in RUN4 showed a **major improvement after sintering, passivation and bump-bonding**

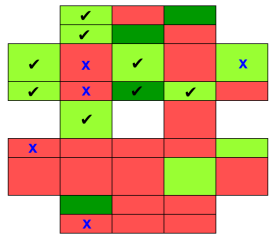
Effect of Sintering on I-V curves (2)

RD53 pixel detectors (example with 25x100)







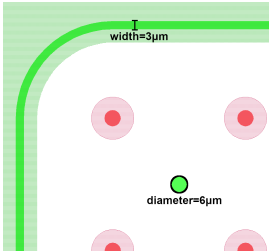


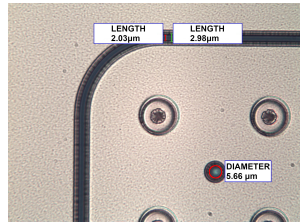
- Example with lower quality wafer
- Lowering and slight flattening of the currents
- Breakdown of good detectors mostly unchanged
- Much more clear separation between bad and good detectors
- IMPROVED → 8
- DEGRADED → 5
- **The tests will be repeated on one wafer by putting the temporary metal on top of the passivation!**

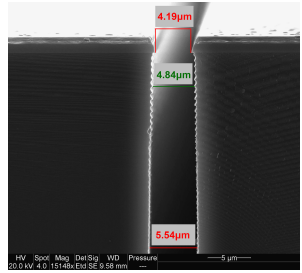
Lessons learned in RUN 5

Lithography accuracy

Designed vs. Real feature size



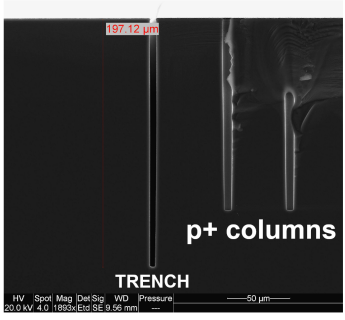




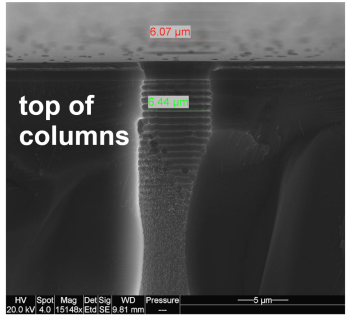
- Tuning of the parameters can be difficult
- Especially with largely different geometries (e.g. columns and trenches)
- Limited measurement precision at the optical microscope
- SEM is used to confirm final of the feature size
- **IMPORTANT** → large trenches can cause a lot of issues in following lithographic steps

Deep Reactive Ion Etching - DRIE (1)

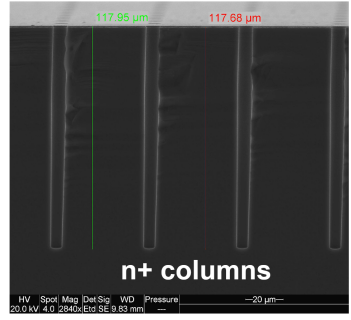
Calibration and monitoring



Trench depth = 197.12µm
p+ col. depth = 152.75µm



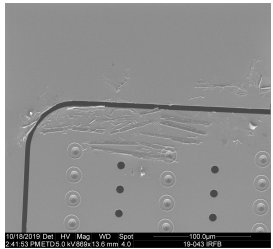
Column top = 6.07µm
Column bot = 6.12µm

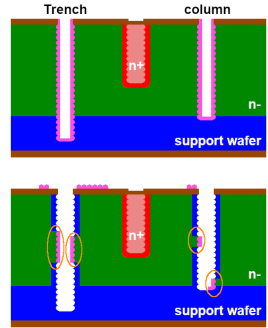


n+ col. depth = 117.95µm

Deep Reactive Ion Etching - DRIE (2)

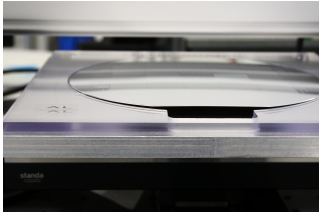
Cleaning after etching

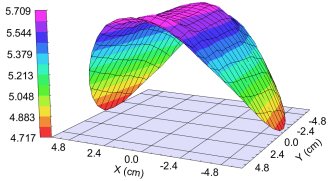


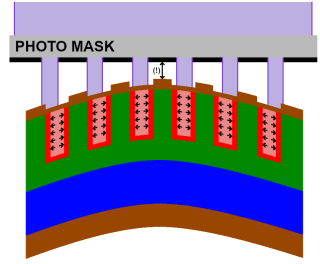


- DRIE alternates steps of etching and passivation layer deposition to achieve anisotropic etching
- The passivation layer is similar to Teflon and Carbon and Fluorine based
- The etching tool can remove it, but it can be difficult in high aspect ratio structures
- If not removed correctly could be cause of contamination
- Could result in masking of the gas doping resulting in undoped regions along the 3D electrodes
- Extra cleaning steps necessary (e.g. plasma ashing)

Wafer bowing and warping (1)





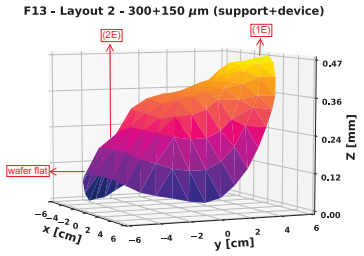


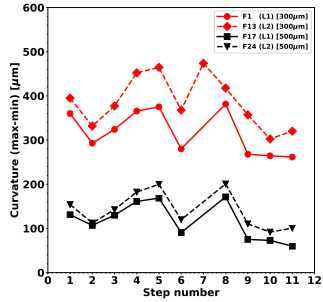
- Issue discovered during the deposition of the metal mask for the DRIE of p+ columns and trenches
- The robot in the sputtering tool was not able to load one of the test wafers
- Curvature measured at the ellipsometer
- Height difference (center to edge) **992μm (!)** $\rightarrow$ **worst case detected** (see next slide...)
- Test wafer (**FZ - SSP**), thickness **500μm (RD53, 25x100)**
- Density of columns double in the bottom half of the wafer
- Stress induced by **polysilicon filling** and slight **unbalance** of **oxide thickness** on fron and back sides of the wafer
- Wafer bowing measurements on RUN4 wafers showed a bowing of $\sim$150μm
- Must be kept under control $\rightarrow$ **alignment, proximity to the photo-mask etc...**

Wafer bowing and warping (2)

Tracking during the process

	WAFER NUMBER	F1	F13	F17	F24
	LAYOUT	1	2	1	2
	SUPPORT WAFER	300µm	300µm	500µm	500µm
1	N+ columns completed	360	395	131	154
2	After Boron doping of P+ columns	292.9	331.7	106.9	112.3
3	After first Polysilicon dep.	324.2	377.2	130	142.5
4	Middle of Polysilicon dep.	365.7	452.1	161.1	182.4
5	End of Polysilicon dep.	375	464.6	168.6	199.9
6	Poly etch (half front)	280	367.9	90.7	119.8
7	Poly etch (front)		473.7		
8	Poly etch (back)	381.5	417.7	171.3	200.7
9	End of Poly etch	267.8	357.2	75.2	110.3
10	After planar p+ doping	264.4	302.7	72.8	91.8
11	AFTER FINAL OXIDATION	261.6	320.1	59.9	100.6



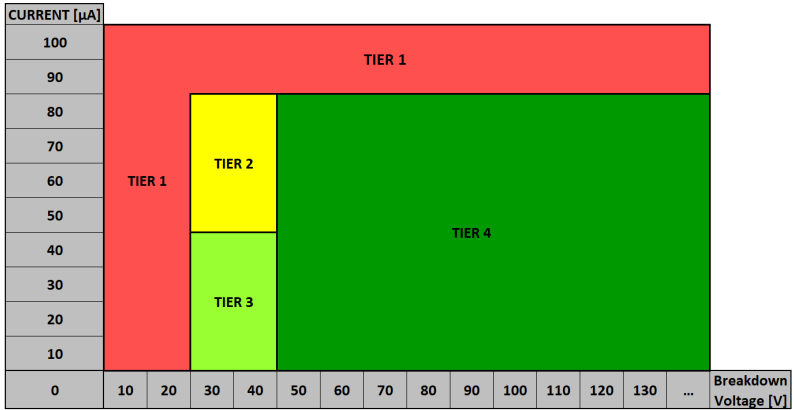


- All wafers follow the same trends
- Bowing increase with processed that have unbalance front/back (e.g. plasma etching)
- **Worst case:** Layout2 with 300μm support wafer
- **Good news:** bowing can be kept under control

Conclusions and future plans

- We have completed the 5th run of 3D detectors at SINTEF MiNaLab
- Temporary metal measurements before sintering are promsing
- Yield slightly lower than in RUN4, but the design was more challenging
- The presence of the active-edge makes processing very challenging
- A lot was learned during each processing step and new QA procedures have been put in place
- Temporary metal on top of the passivation will be tested on one wafer at the end of the process (2-3 weeks from now)
- The design for RUN6 is completed (common layout with the other fabs)
- The active-edge is not strictly necessary and will not be implemented anymore
- Wafers for the next fabrication run should arrive in the next 2 weeks
- RUN6 will be ready to start processing soon

Technology for a better society

BACKUP SLIDES

Sensor selection criteria