FAST: a front-end readout ASIC for picosecond time resolution applications with UFSD

By Jonhatan Olave

F.Fausti, N. Cartiglia, R. Arcidiacono

TREDI2020

15th "Trento" Workshop on Advanced Silicon Radiation Detectors

Wien 18th February 2020

OUTLINE

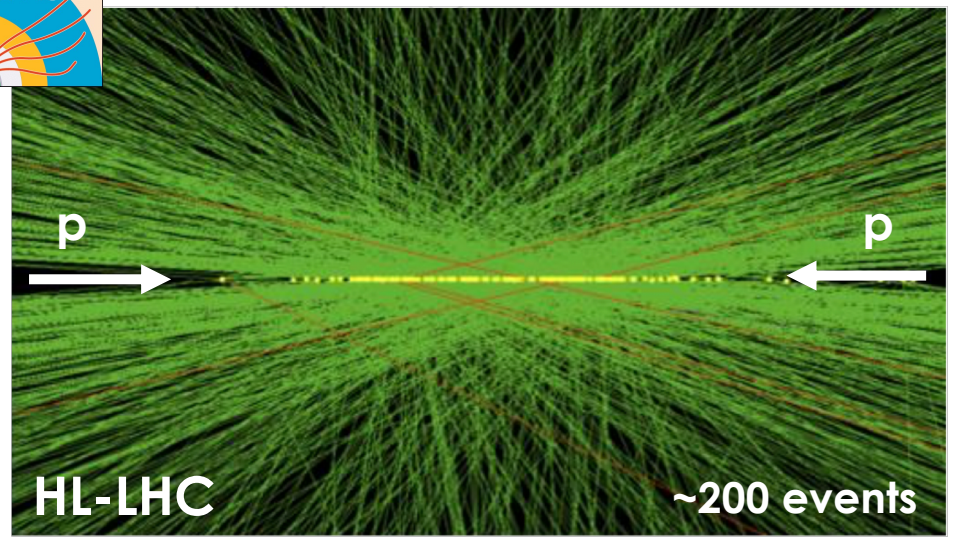
1. Motivation
2. Picosecond time resolution: what is needed?
3. State of the art of picosecond ASICs
4. The FAST prototypes
5. Simulation and silicon results
6. Conclusions and future plans

1/6

Motivation

Picosecond time resolution in HEP experiments

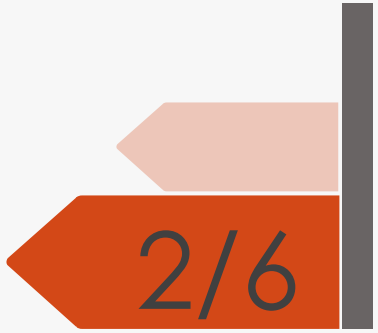
Why picosecond time resolution?



Pile-up in LHC

	Ins. Lumi ($cm^{-2}s^{-1}$)	Peak pileup
LHC	1.7 x 10^{34}	60
HL-LHC	5-7.5 x 10^{34}	200

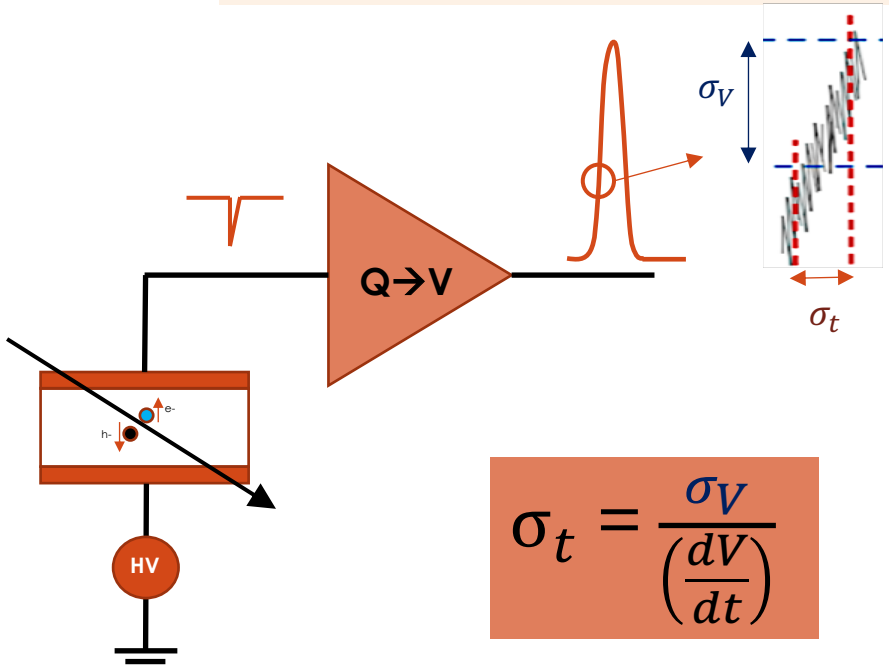
- In future experiments pile-up is an important factor to take into account. In HL-LHC the expected **events per bunch crossing** are going to increase from 60 to about **150-200**
- According to simulations the **fraction of overlapping vetexes** is **15-20 %**
- The reconstruction of time information with picosecond time resolution allows to distinguish among events overlapped in space
- Timing is included in future experiments in different ways:
  - **Timing layers** (like ETL in CMS or HGTD in ATLAS)
  - **4D detectors**: timing is measured for each point along the track
- In medical applications: Positron Emission Tomography (PET) it allows to improve the image resolution



Detectors for picosecond time resolution

What is really needed?

Picosecond time resolution: what is needed?



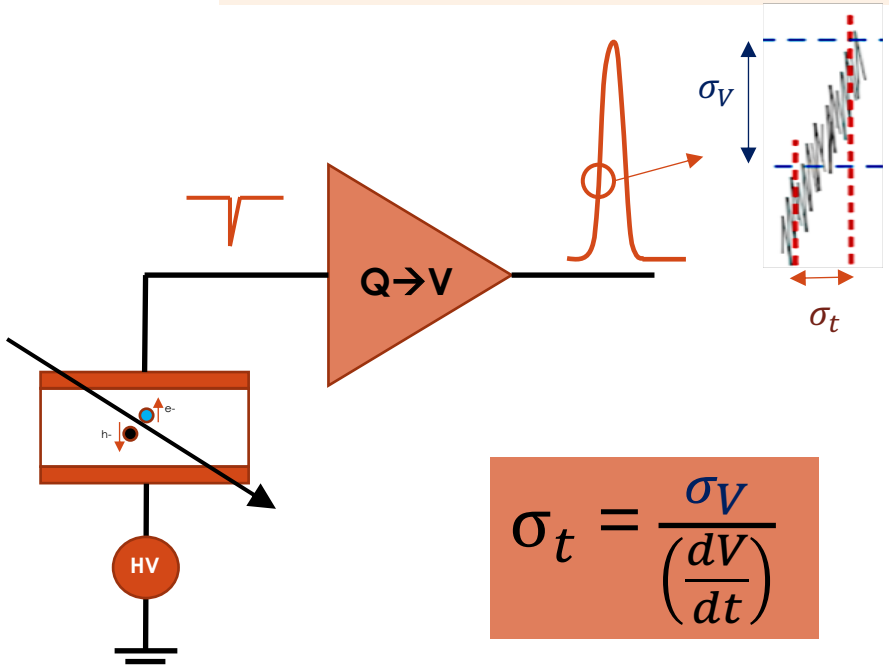
$$\sigma_t = \frac{\sigma_V}{\left(\frac{dV}{dt}\right)}$$

$$\sigma_t^2 = \sigma_{sensor}^2 + \sigma_{electronics}^2$$

- **dV/dt term increases** if

amplitude ↑ rise time ↓

Picosecond time resolution: what is needed?



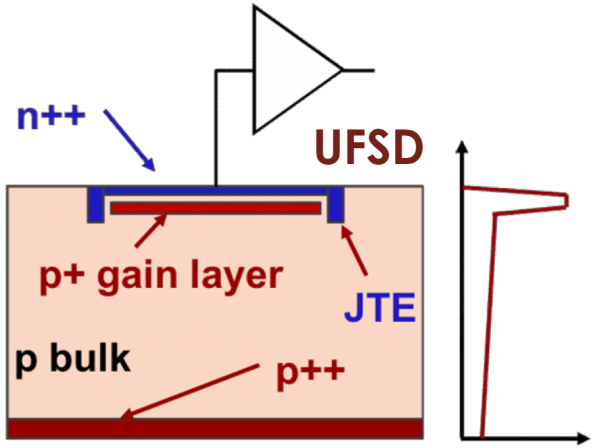
$$\sigma_t = \frac{\sigma_V}{\left(\frac{dV}{dt}\right)}$$

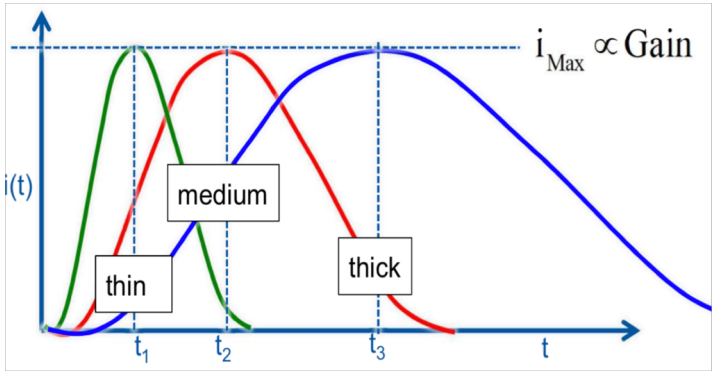
$$\sigma_t^2 = \sigma_{sensor}^2 + \sigma_{electronics}^2$$

- **dV/dt term increases** if

amplitude ↑ rise time ↓

Silicon sensors for timing





- Signal amplitude:
  - **modulated** with the internal **gain**
  - **does not depend on the thickness**
- Signal rise time:
  - **thin sensors → fast rise time**
  - typical duration (55 µm): 1.2 ns

$$\frac{dV}{dt} \propto \frac{G}{d}$$

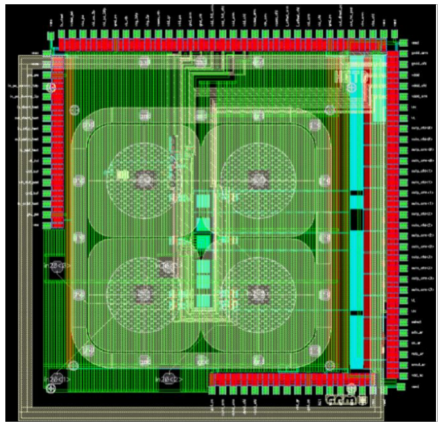
3/6

Picosecond ASICs

State of the art

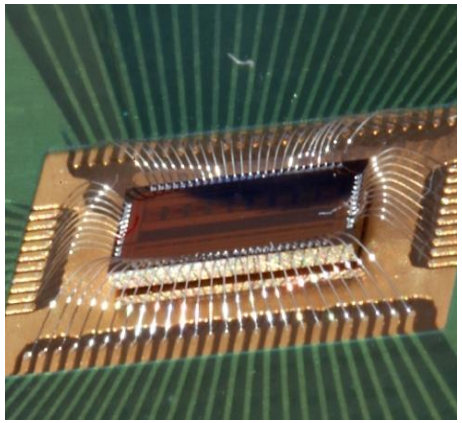
Examples of fast front end electronics

ALTIROC0 (OMEGA)



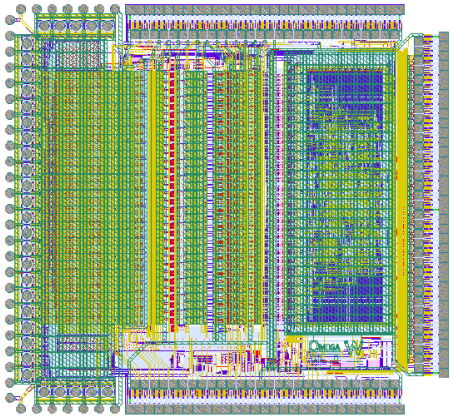
Sensor: LGAD 3.4 pF
jitter = 48 ps
Power = 5 mW/ch
Q_{in}= 3fC – 30fC
CHs: 8
Tech: CMOS 0.13 µm

NINO (CERN)



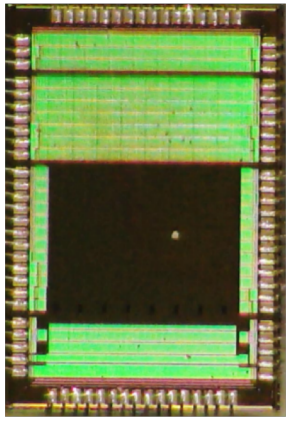
Sensor: SiPM
Jitter = 10 ps
Power = 27 mW/ch
Q_{in} = 30 fC – 2 pC
CHs: 8
Tech: CMOS 0.25 µm

PETIROC2 (OMEGA)



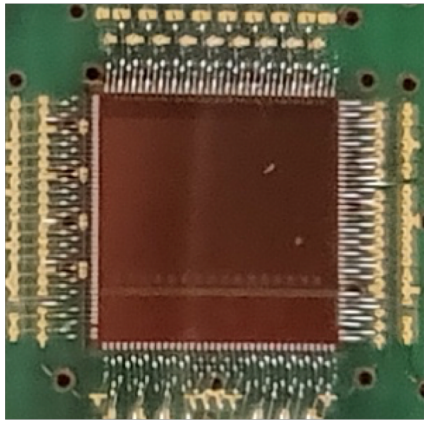
Sensor: SiPM
jitter = 20–30 ps
Power= 6 mW/CH
Q_{in} = 160 fC-400pC
CHs: 32
Tech: SiGe 0.35 µm

TOFFEE (TORINO)



Sensor: LGAD 3/6 pF
jitter = 50 ps
Power= 12 mW/ch
Q_{in} = 3fC-30fC
CHs: 8
Tech: CMOS 0.11 µm

TOFHIR (LIP)



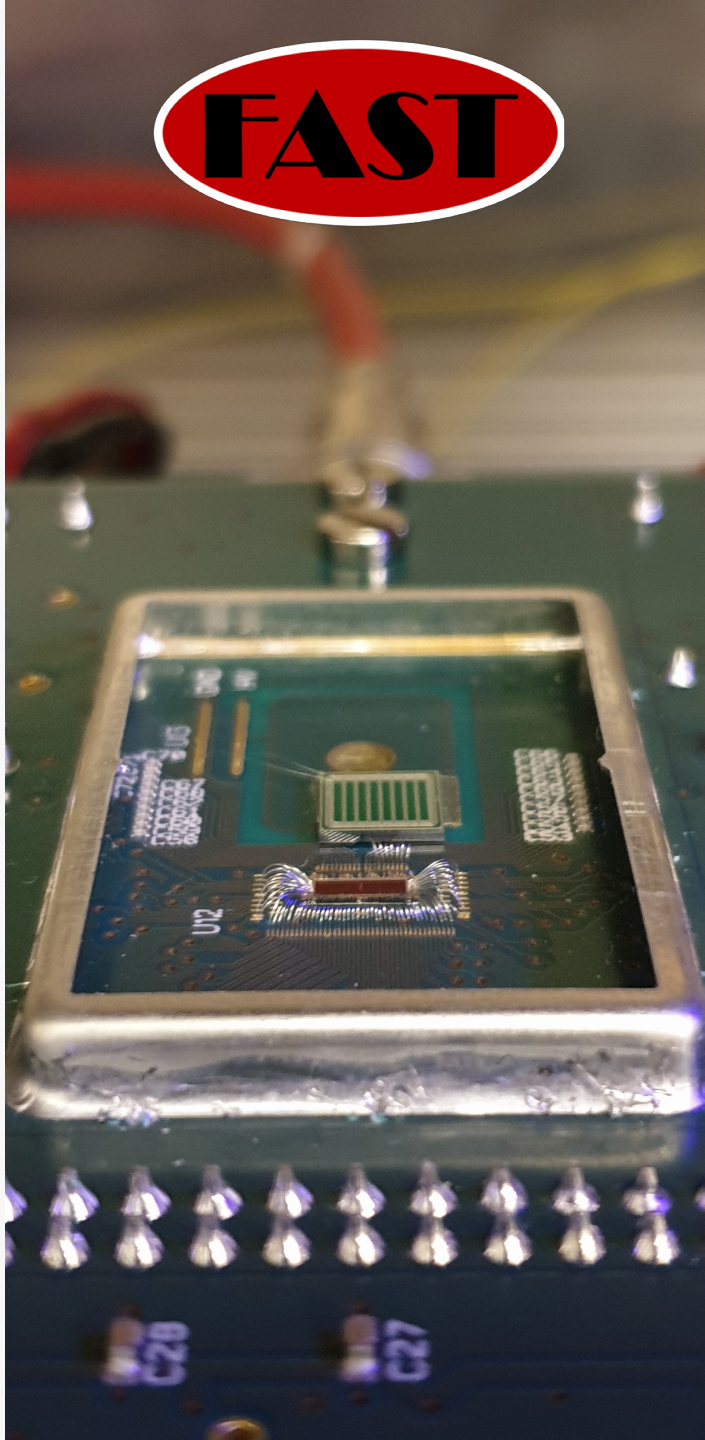
Sensor: SiPM
jitter = 30 ps
Power= 8 mW/ch
CHs: 16
Tech: CMOS 0.11 µm

It's quite difficult to combine the requirements of timing with sensor size and power

4/6

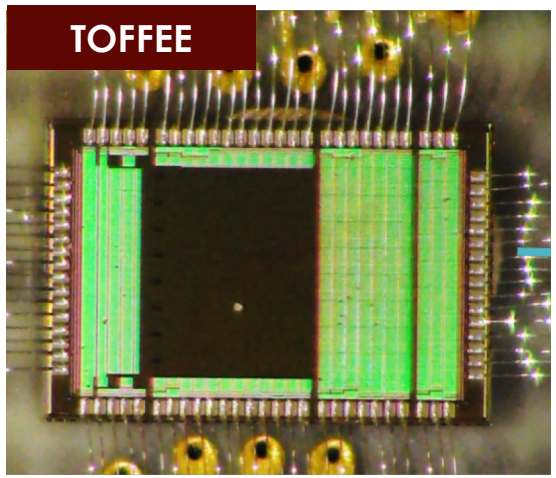
The FAST prototypes

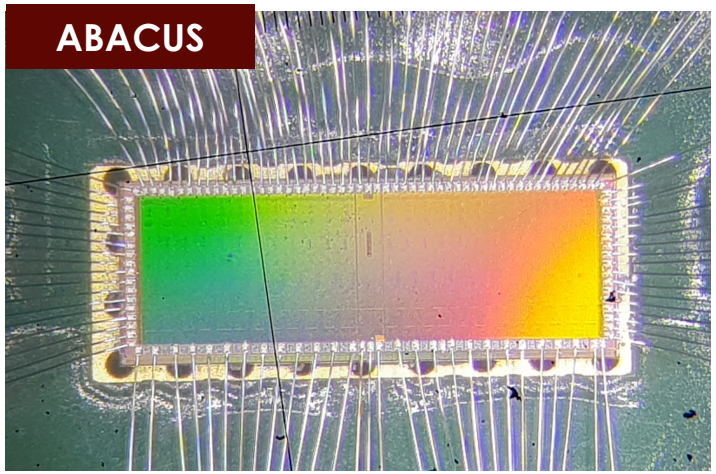
General ASICs description

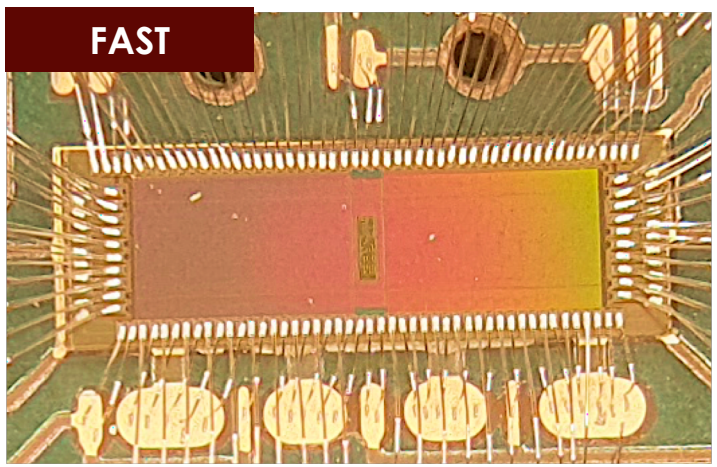


ASICs developed for applications with UFSD

Developed @ INFN Torino







TIME

ASIC	Application	#ch	mm²	mW/ch	technology	FoM	Production
TOFFEE	Timing	8	3.6x2.5	20	110nm	45 ps (8 fC MIP)	2016
ABACUS	Single ion counting	24	5x2	15	110nm	3-130 fC Qin @ 100 MHz	2018
FAST	Timing and counting	20	5x1.7	3	110nm	25 ps Jitter (8 fC MIP)	July 2019

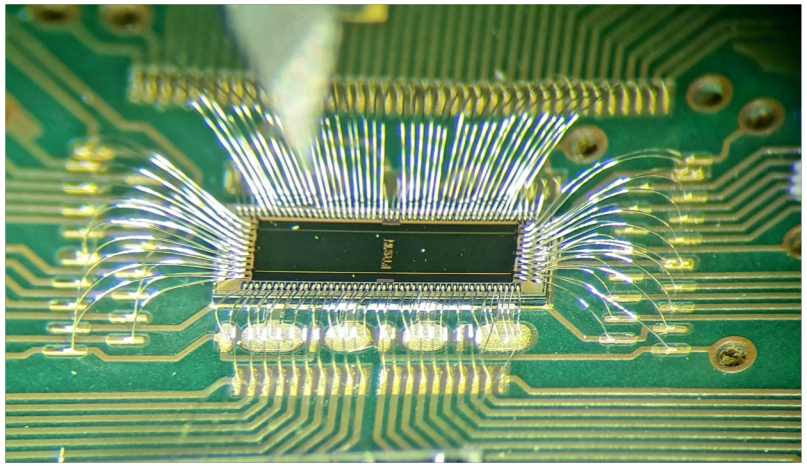
- **FoM**: picosecond time resolution and single ion detection at high rates (e.g. particle therapy applications)
- **Main challenges**: low power budget (<1.5 mW/Ch) and large sensor capacitance (6pF)

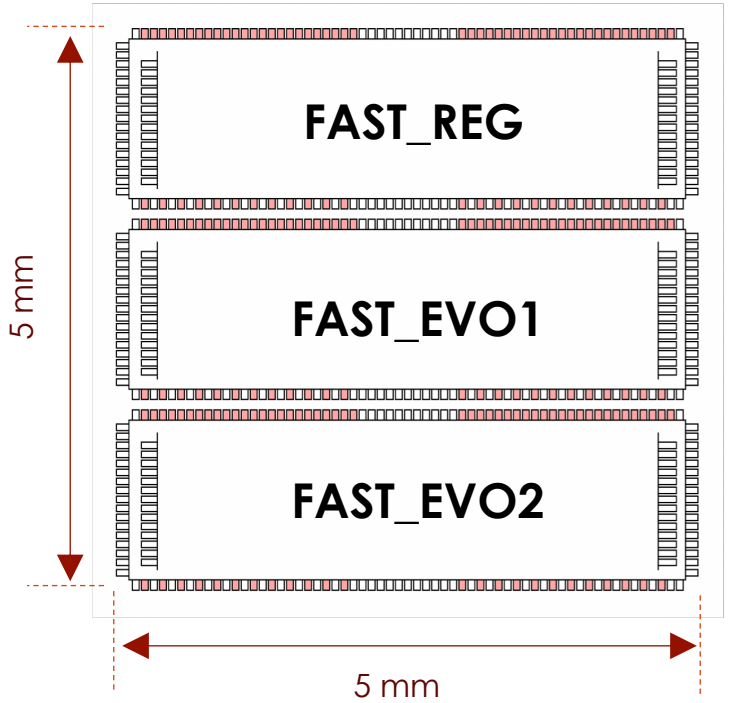
The FAST prototypes

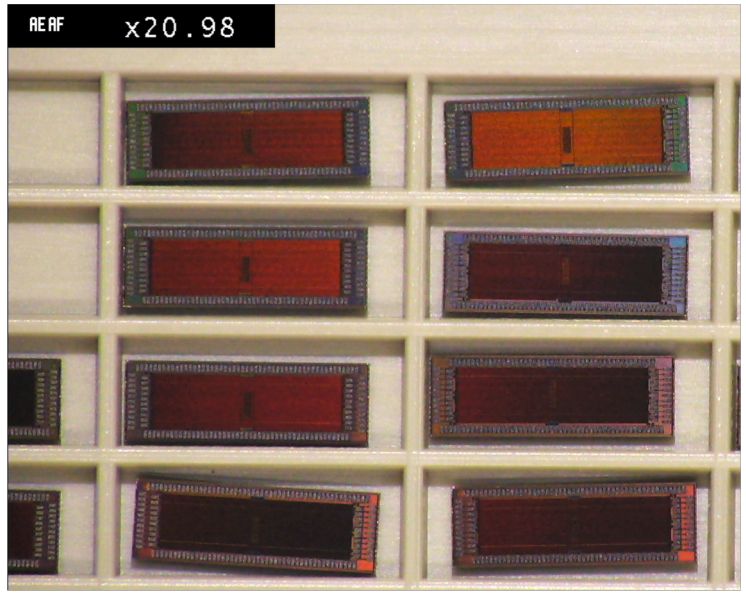
Specifications

Channels number	20
FAST flavors	Regular, EVO1, EVO2
Operation Voltage	1.2 V
Size	1.6 × 5 mm^2
Sensor Cap	2-6 pF
$\overline{SNR}$	60
RMS Noise	~ 0.7 mV
Power consumption	< 2 mW/CH
Time Walk correction	ToA, Tot
MPV input signal	8fC
Nominal input dynamic range	1 fC - 60 fC

- A set of 3 ASICs has been produced in a **MPW** (07/2019)
- Chip size: 1.6 x 5 mm^2
- The flavours differ on the front-end amplifiers
- The same IO-ring is used → the **same PCB and setup**
- Each ASIC implements 20 channels

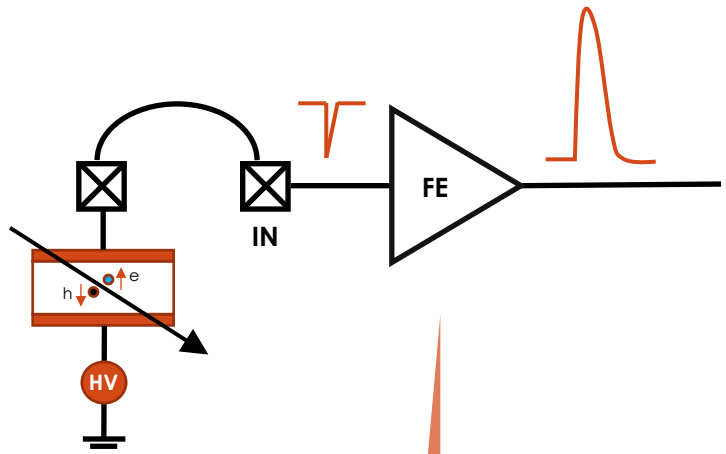






The channel

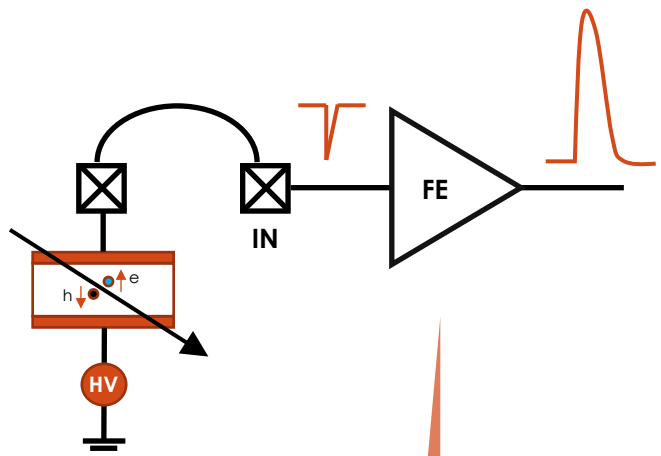
Very front-end



The very front end

- **Three** architectures
- Power limited to **1.5 mW/CH**
- Designed for **1 proton MIP in 50 µm** thick UFSD sensor
- Sensor cap: **1 pF – 6 pF**

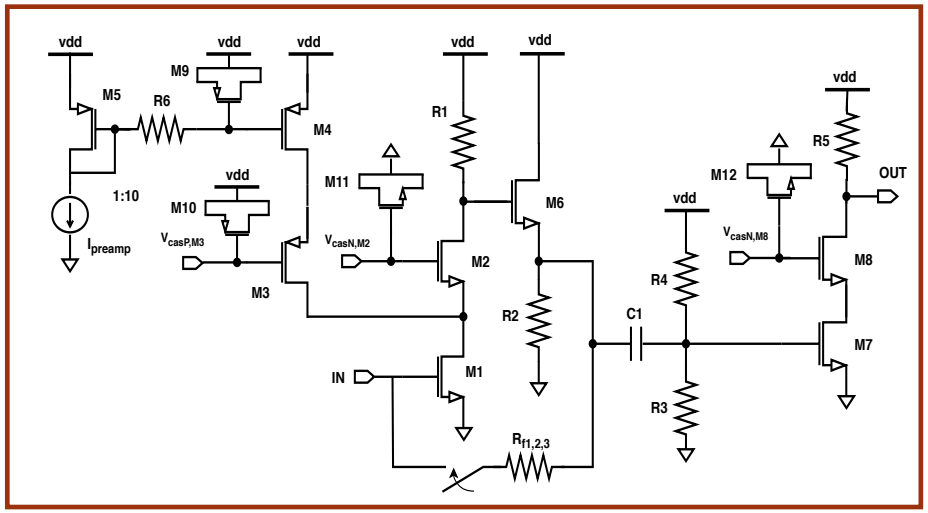
The channel



The very front end

- **Three** architectures
- Power limited to **1.5 mW/CH**
- Designed for **1 proton MIP in 50 µm** thick UFSD sensor
- Sensor cap: **1 pF – 6 pF**

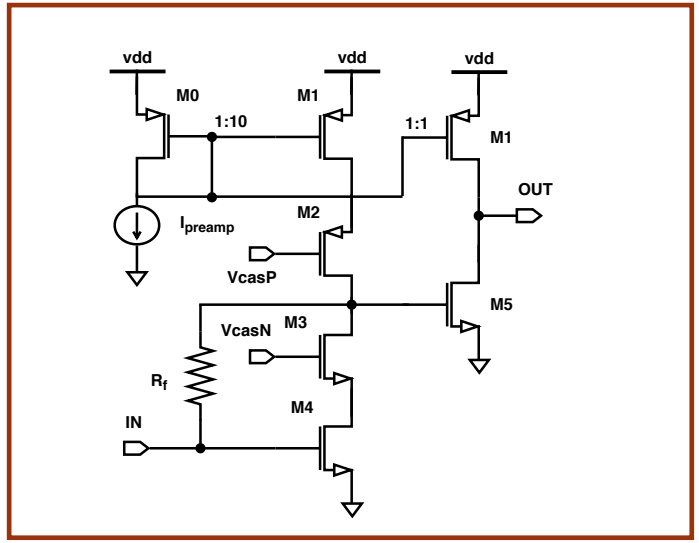
Trans-impedance - BB



EVO

- Larger bandwidth: ~ 400 MHz
- Gain: ~ 31 mV/fC (8 regulations)
- Noise: ~640 e$^-$
- Power consumption: ~1.2mW/CH
- SNR(MIP): ~75
- Max hit rate: 300 MHz
- AC coupling to reduce mismatch
- 2 topologies: standard CMOS & RF

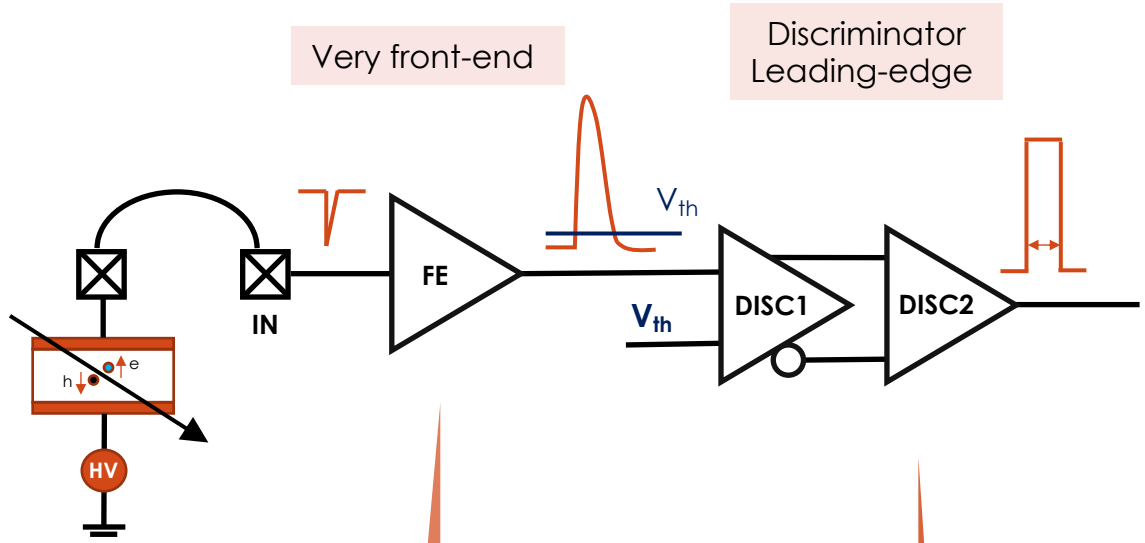
Trans-impedance - CS



REGULAR

- Limited bandwidth to 100 MHz
- Gain: ~ 60 mV/fC
- Noise: ~310 e$^-$
- Power consumption: ~1.2mW/CH
- SNR (MIP): ~ 160
- Max hit rate: 50 MHz

The channel



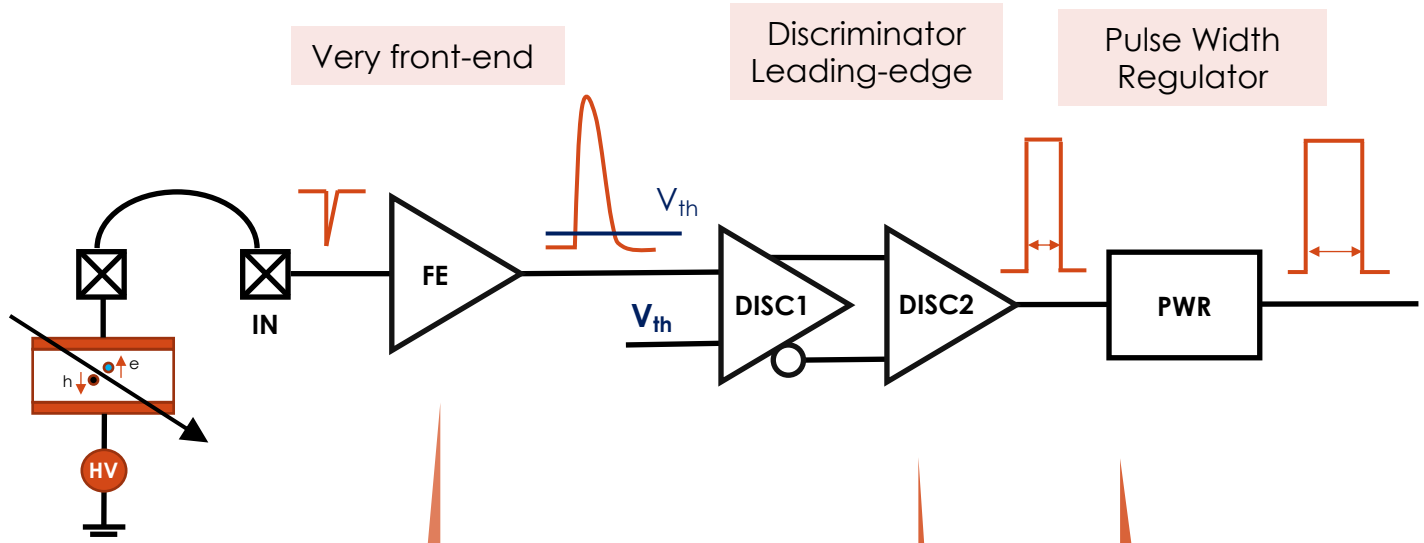
The very front end

- **Three** architectures
- Power limited to **1.5 mW/CH**
- Designed for **1 proton MIP in 50 µm** thick UFSD sensor
- Sensor cap: **1 pF – 6 pF**

Discriminator

- Two stage leading-edge differential discriminator
- Power < **0.6 mW/CH**
- **time walk**
  → offline corrected

The channel



The very front end

- **Three** architectures
- Power limited to **1.5 mW/CH**
- Designed for **1 proton MIP in 50 µm** thick UFSD sensor
- Sensor cap: **1 pF – 6 pF**

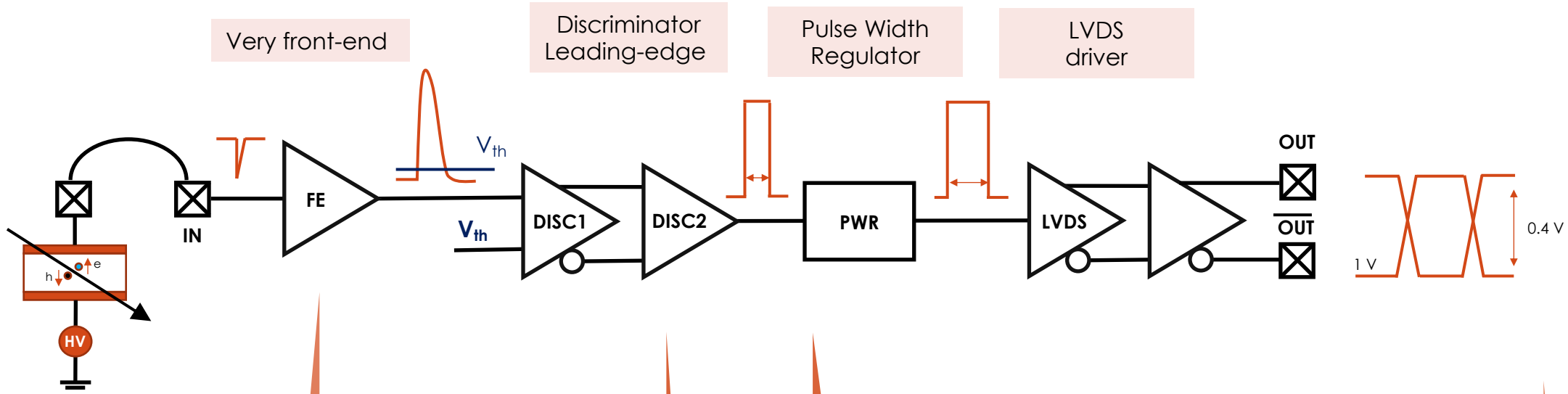
Discriminator

- Two stage leading-edge differential discriminator
- Power < **0.6 mW/CH**
- **time walk**
  → offline corrected

Pulse width regulator

- Pulse duration(MPV): **2-4 ns**
- This block can increase a regulated Δt to the output duration to make it compatible with **commercial TDCs**

The channel



The very front end

- **Three** architectures
- Power limited to **1.5 mW/CH**
- Designed for **1 proton MIP in 50 µm** thick UFSD sensor
- Sensor cap: **1 pF – 6 pF**

Discriminator

- Two stage leading-edge differential discriminator
- Power < **0.6 mW/CH**
- **time walk**
  → offline corrected

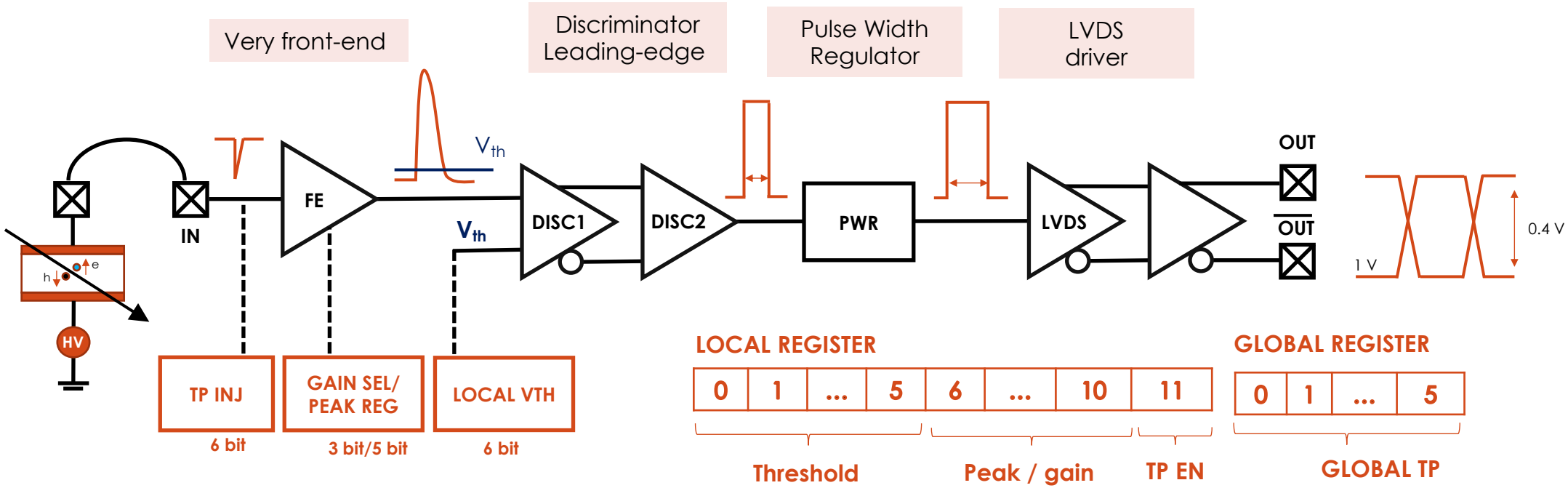
Pulse width regulator

- Pulse duration(MPV): **2-4 ns**
- This block can increase a regulated Δt to the output duration to make it compatible with **commercial TDCs**

LVDS drive

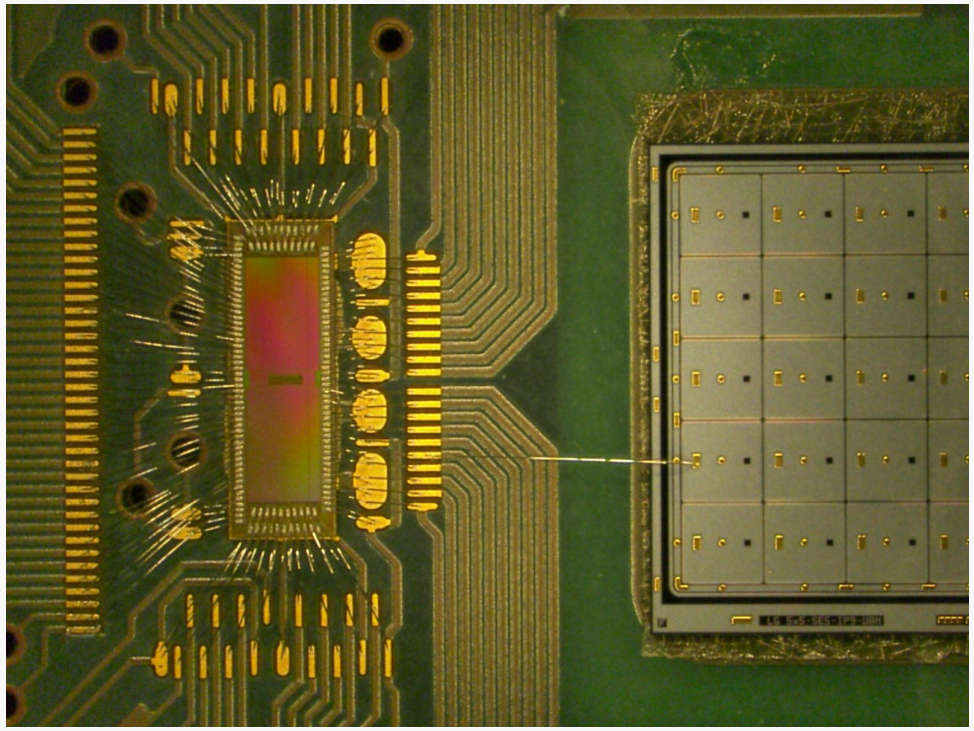
- It allows compatibility with **commercial TDCs and FPGAs**

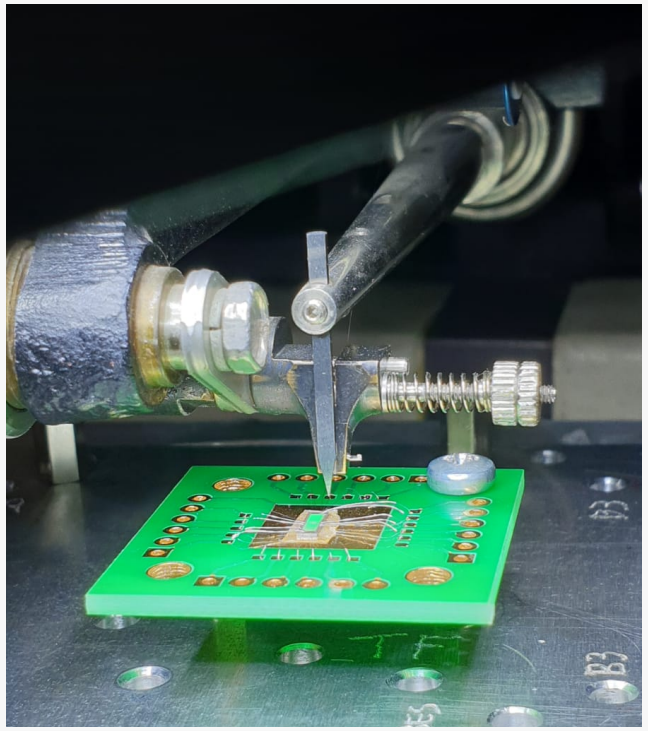
The channel



Ancillary circuitry

- **Test Pulse injection system:** a global register of 6 bits is used to inject charge from 0.3 fC to 18 fC
- **Selectable gain (EVO) or peaking time (REG):** 3 bits/5bits used to select 8 different gains in EVO or for the peaking time tuning in REG. The last regulation is meant to minimize noise
- **Local threshold regulation:** the threshold can be locally regulated up to 30 mV with 6 bits DAC
- **Pulse width regulation:** It allows to add a fixed Δt to the pulse duration.

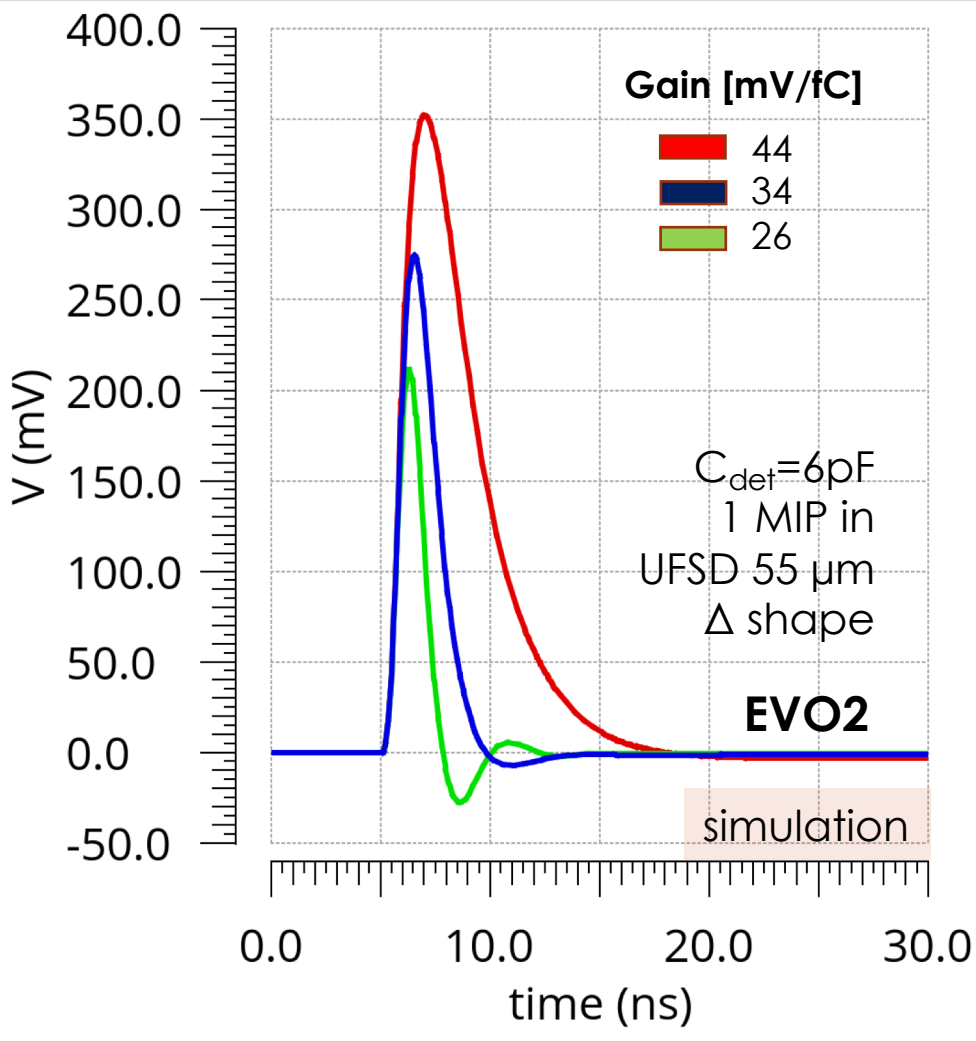




Simulations and silicon results

Effects of the FE gain: analog output and jitter

Vout vs gain



jitter and rate vs gain

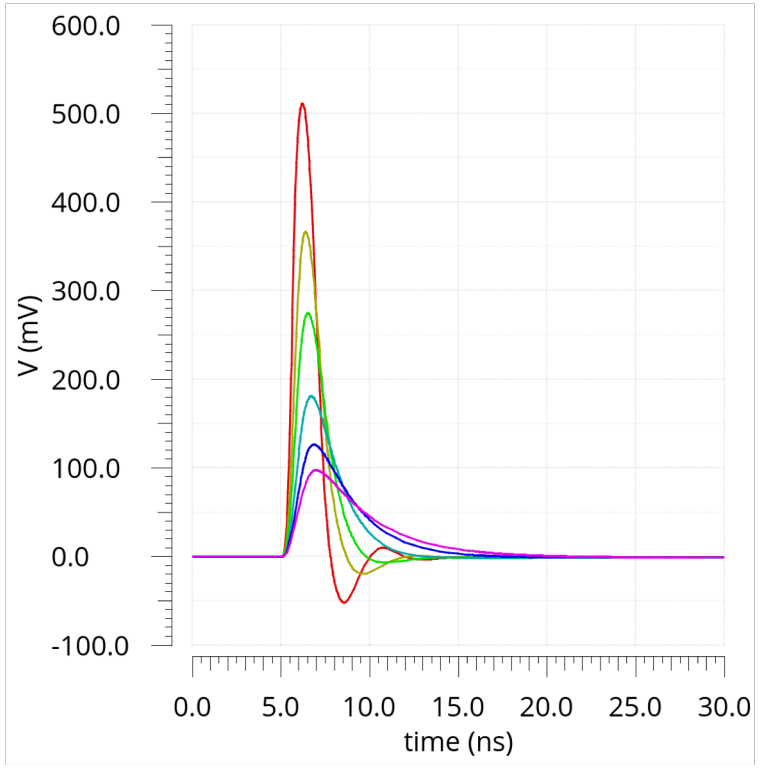
simulation

Gain [mV/fC]	Amplitude [mV]	Jitter [ps]	Noise [e^-]	Max rate [MHz]
26	211	19.8	779	300
34	274	18.5	610	227
44	352	19.8	493	128

- EVO channels have a **programmable gain** that changes the bandwidth of the FE. This can be used to tune the analog signal duration and amplitude
- Gain does not affect significantly the timing performances. In all cases jtter is ~20 ps
- Generally noise decreases with gain
- Gain ↓ → max rate ↑

Effects of C_{det}: analog output and jitter

Analog output vs C_{det}



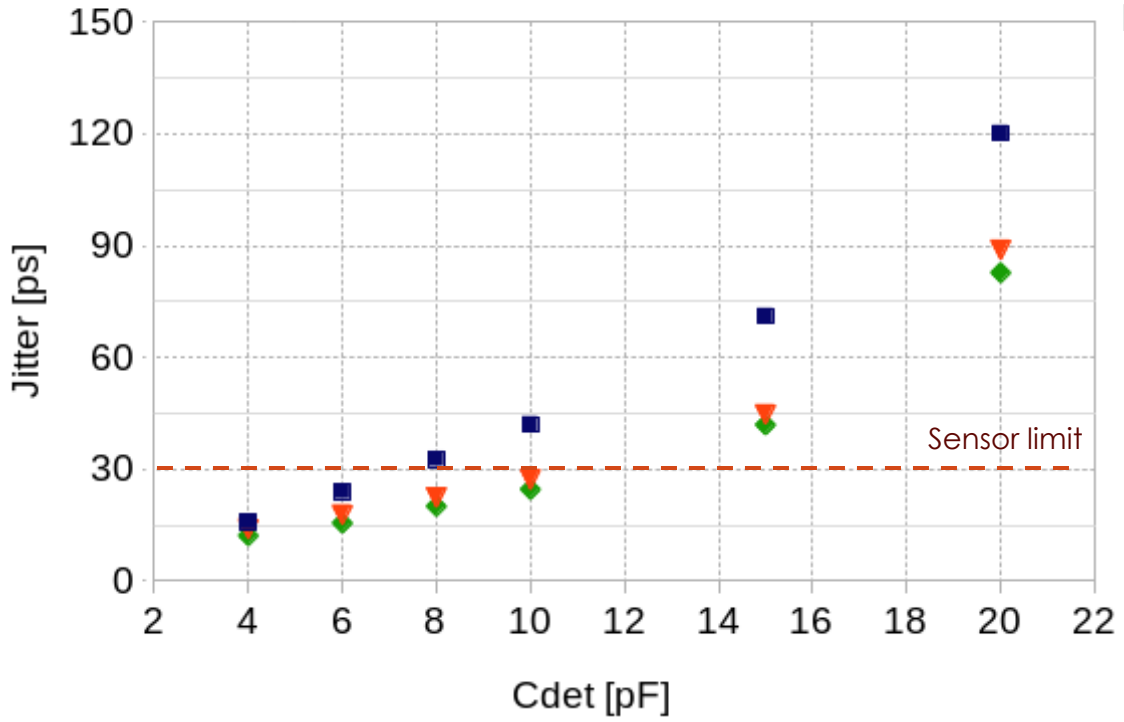
Cdet [pF]

- 2
- 4
- 6
- 10
- 15
- 20

1 MIP in
UFSD 50 µm
Δ shape

EVO2
simulation

jitter vs C_{det}



Front-end

- REG
- EVO1
- EVO2

1 MIP in
UFSD 50 µm
Vth=3fC

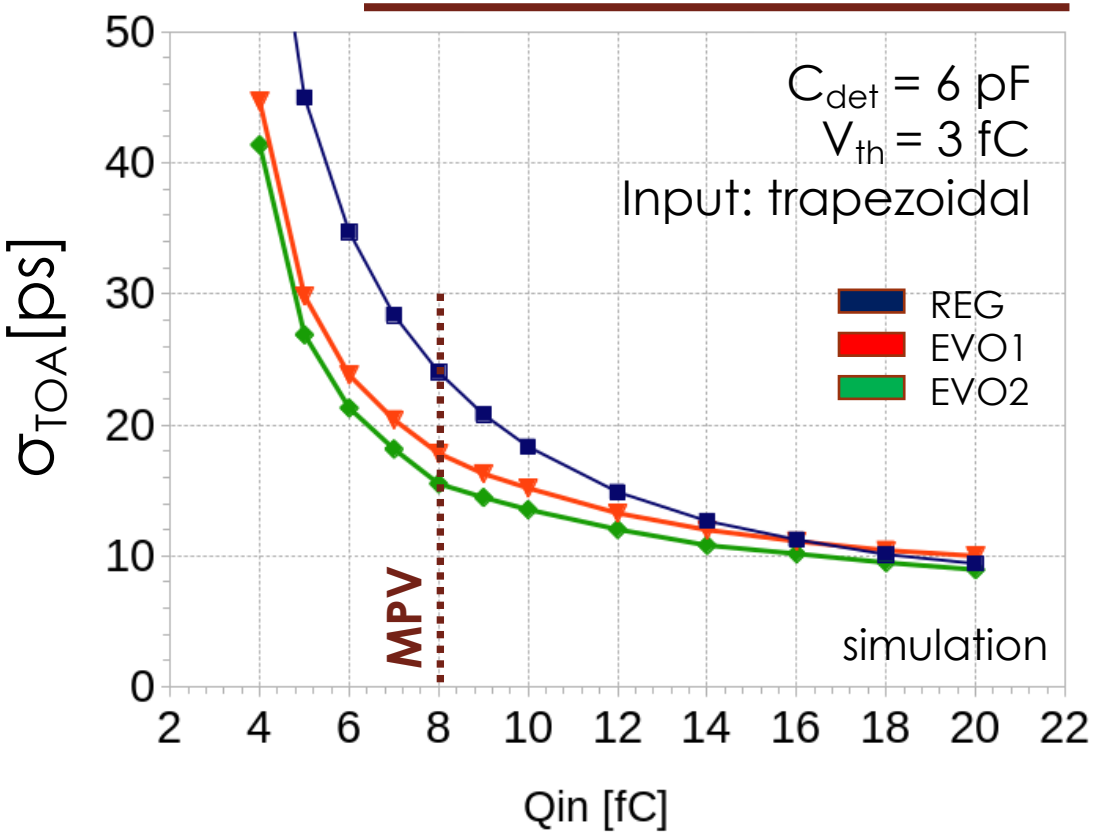
simulation

- The analog output (amplitudes and duration) changes with the C_{det}
- Amplifiers are designed to reach 30 ps with 6 pF UFSD sensor
- Sensor cap ↓ Time resolution
  Max rate ↑

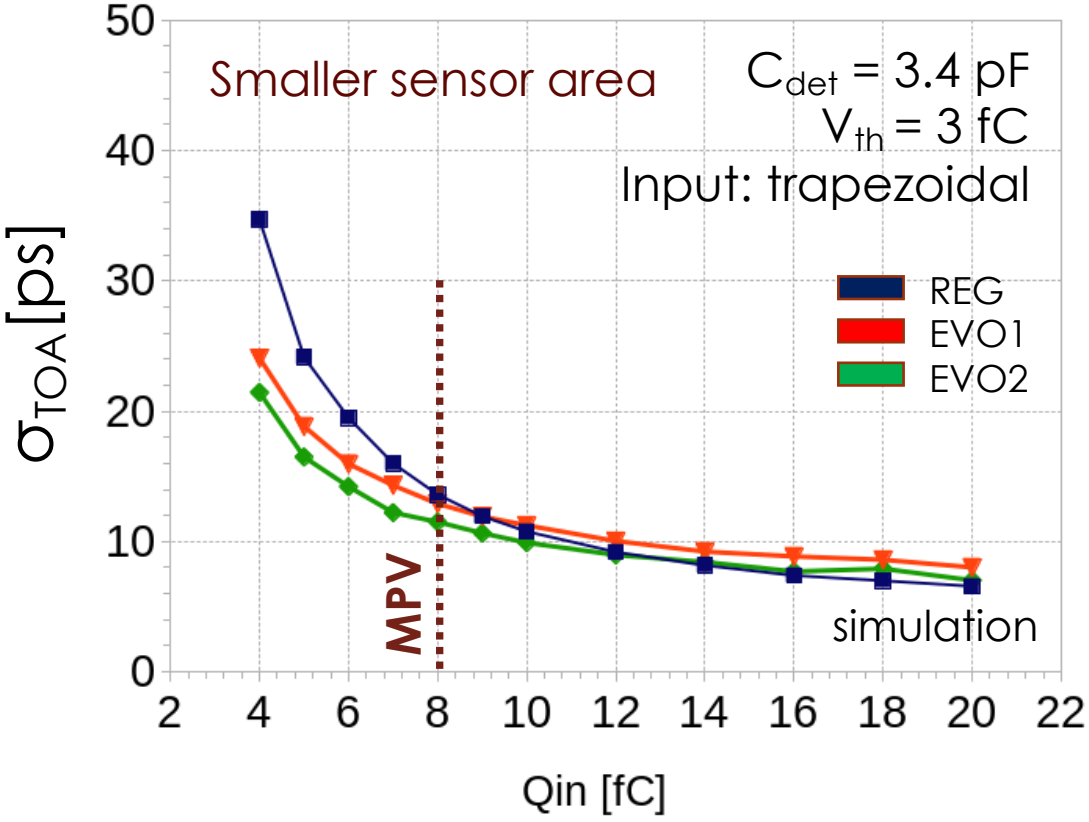
Jitter vs input charge

- 1 proton MIP release charge in silicon according to **the Landau distribution**
- The most probable value (MPV) 55 µm thick UFSD (G=15) is 8 fC
- Jitter of the MPV is about **20 ps** and **12 ps** for 6 pF and 3.4 pF sensors
- LE-discriminator is used → time walk degrades time resolution → corretion is needed (ToT)

6 pF sensor



3.4 pF sensor



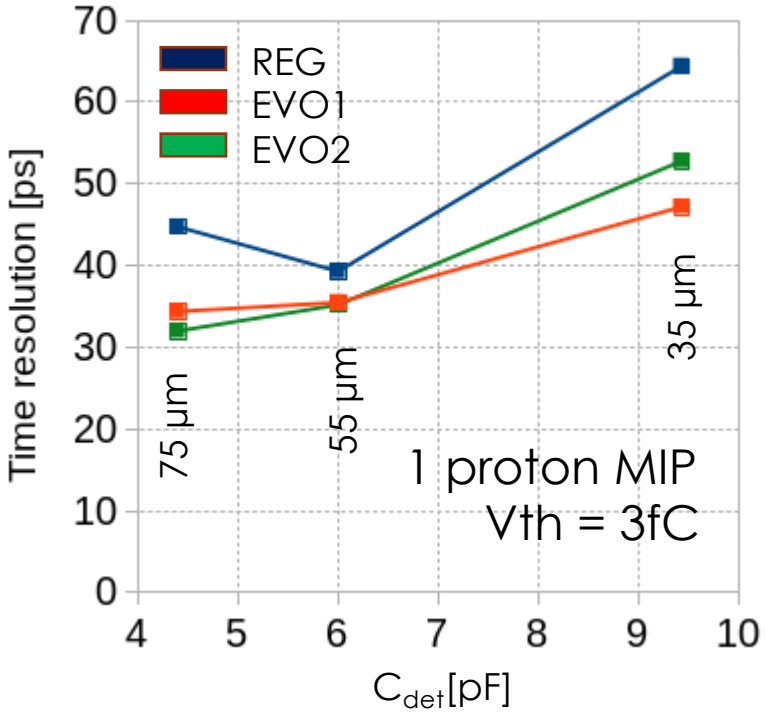
Time resolution vs sensor area and thickness

- Almost all terms that affect time resolution are simulated:

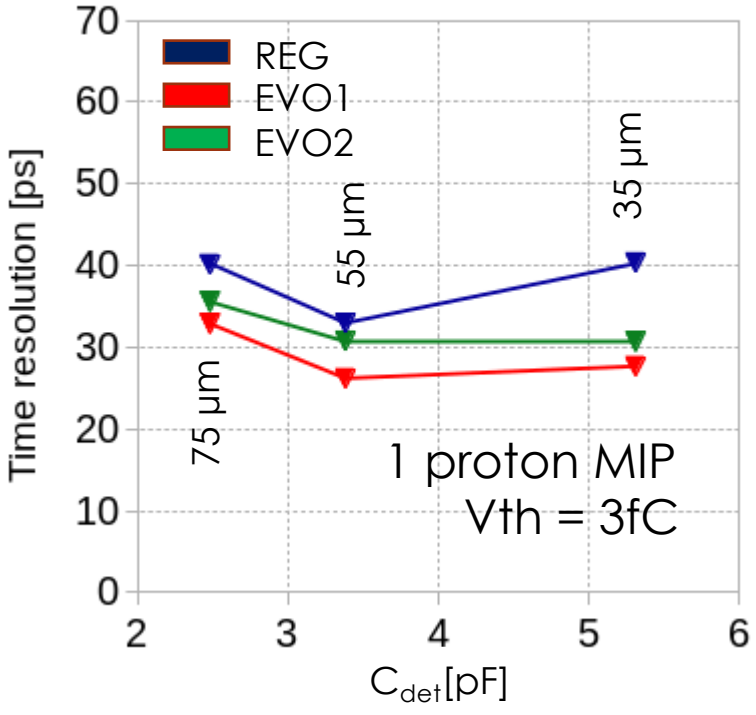
$$\sigma_t^2 = \sigma_{LANDAU\ NOISE}^2 + \sigma_{DISTORTION}^2 + \sigma_{JITTER}^2 + \cancel{\sigma_{TDC}^2} + \sigma_{TIME\ WALK}^2$$

- Important parameters:
  - → **3 Sensor thicknesses**: 35 µm, 55 µm, 75 µm (3 values of C_{det})
  - → **3 Sensor geometries**: 1x1 mm², 1.3x1.3 mm² and 1x3 mm²
  - → **3 Front-ends**: REGULAR, EVO1 and EVO2

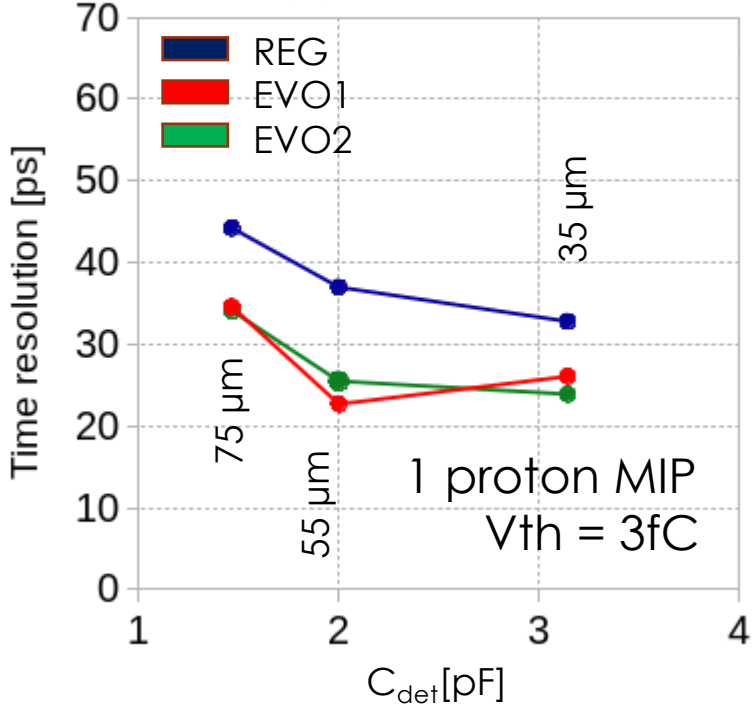
Area = 1x3 mm²



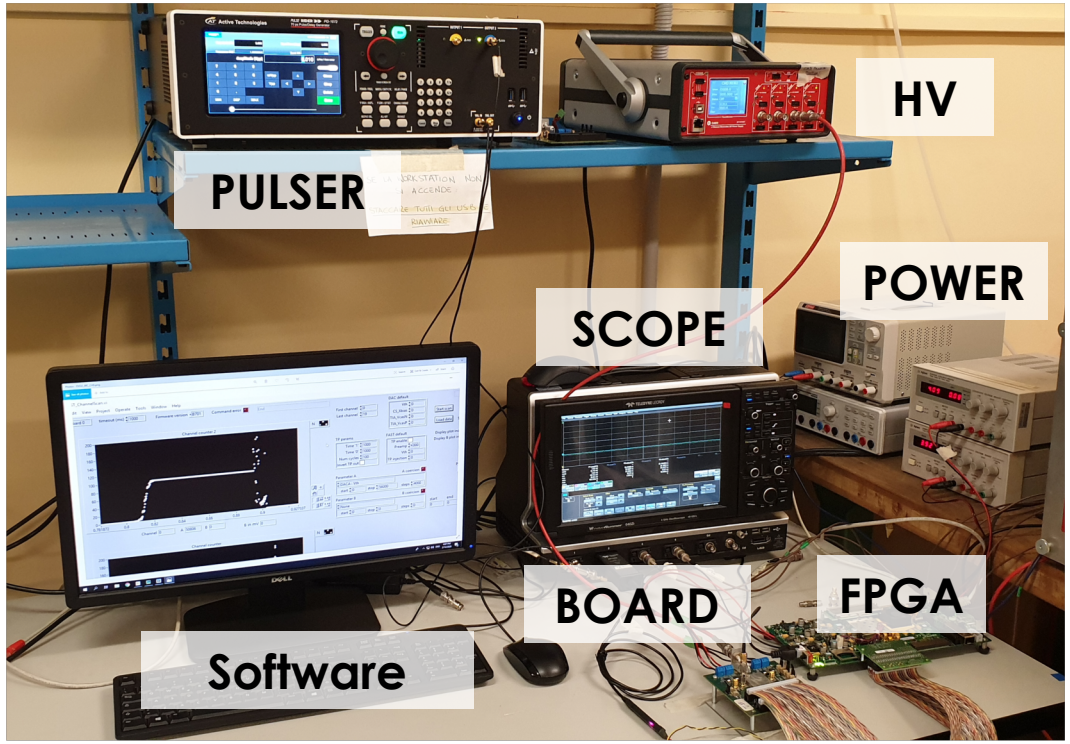
Area = 1.3x1.3 mm²

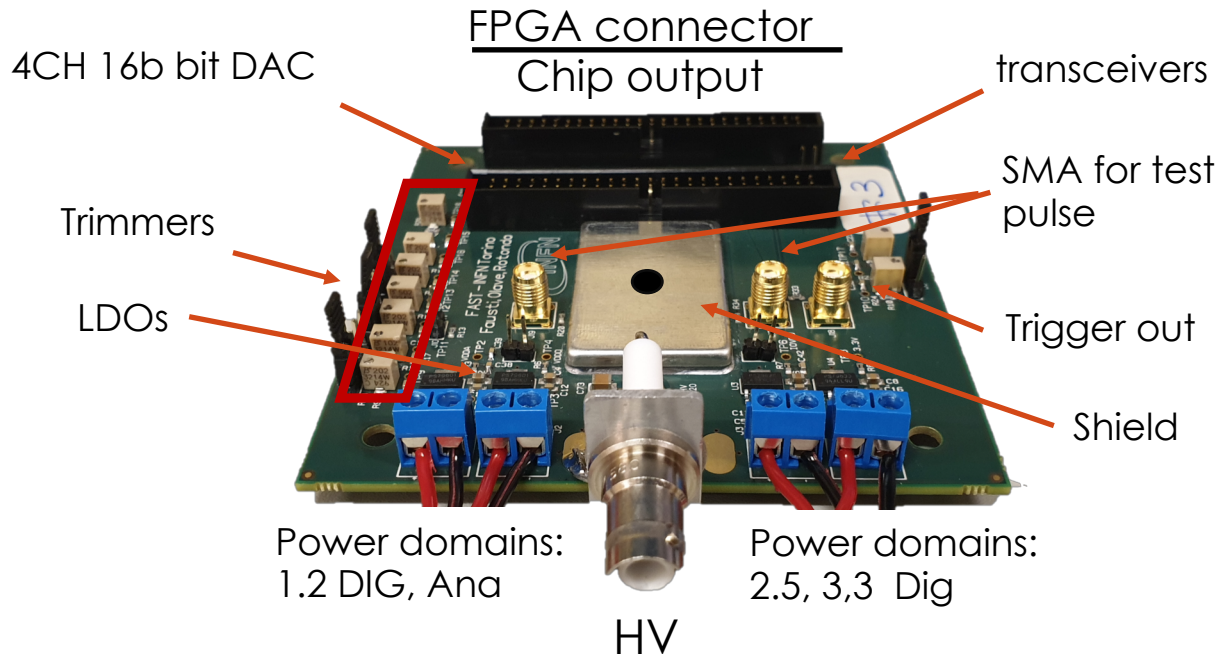


Area = 1x1 mm²



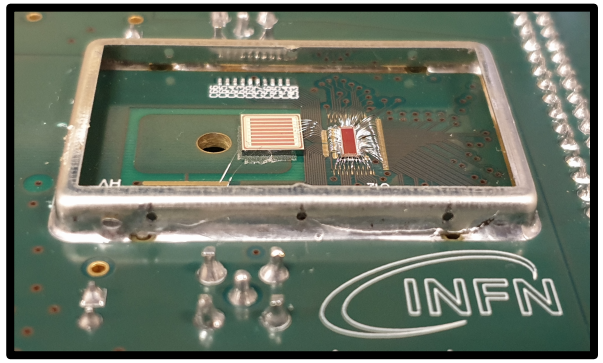
The setup





- Pulser (Pulse Rider PG-1000) with fast rise time (< 70 ps)
- Kintex-7 FPGA used to control the board and to process the data sent from the ASIC
- Software based on LabView meant to control the data acquisition system
- Differential probe used for reading the differential output

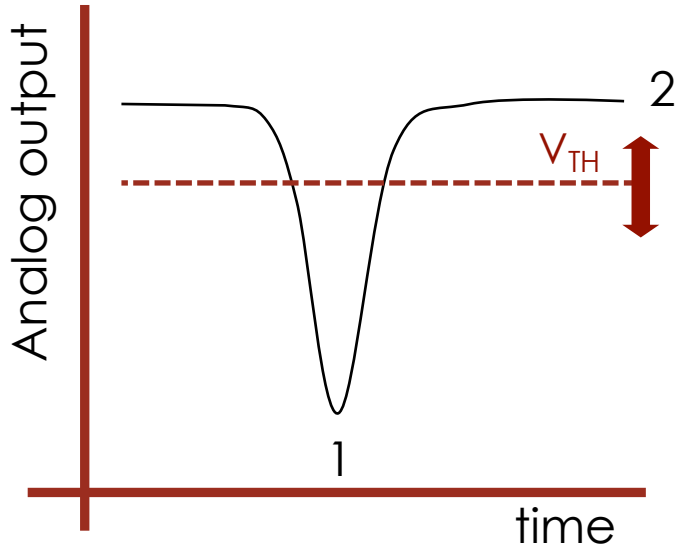
FAST + FBK strip UFSD2 1x5 mm²



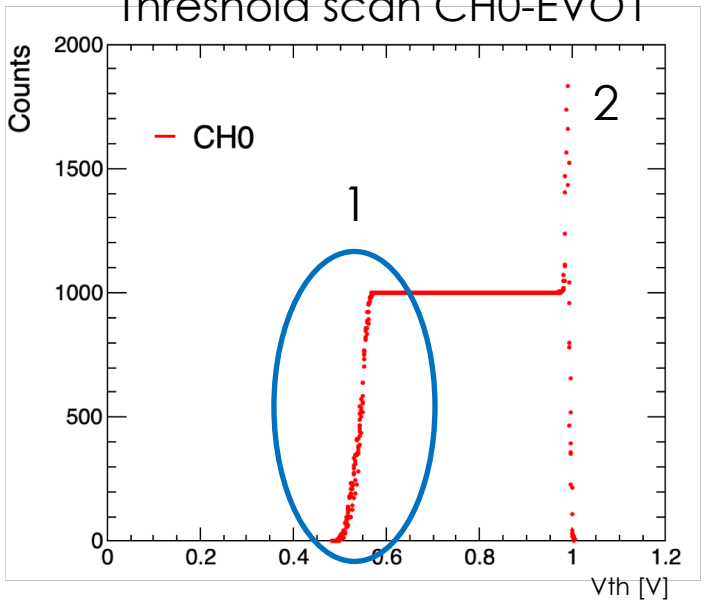
Noise reduction strategies

- Power domains are separated
- Shielding is used in both PCB sides to avoid EMI disturbance
- Threshold is provided in two independent ways: simple trimmer or 16 bit DAC

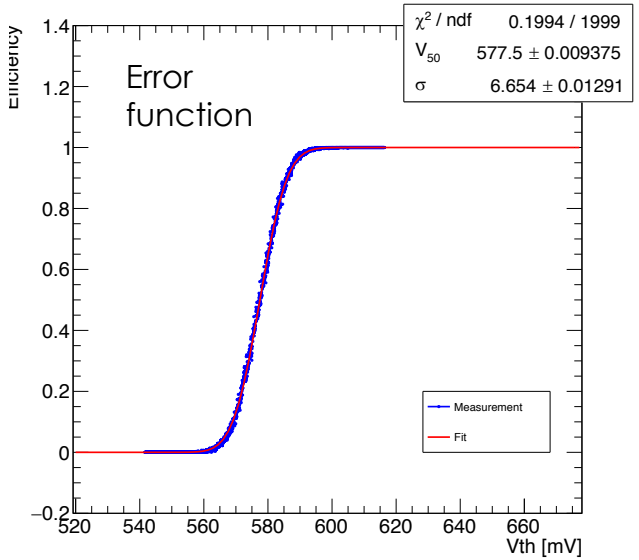
Noise measurements (I)



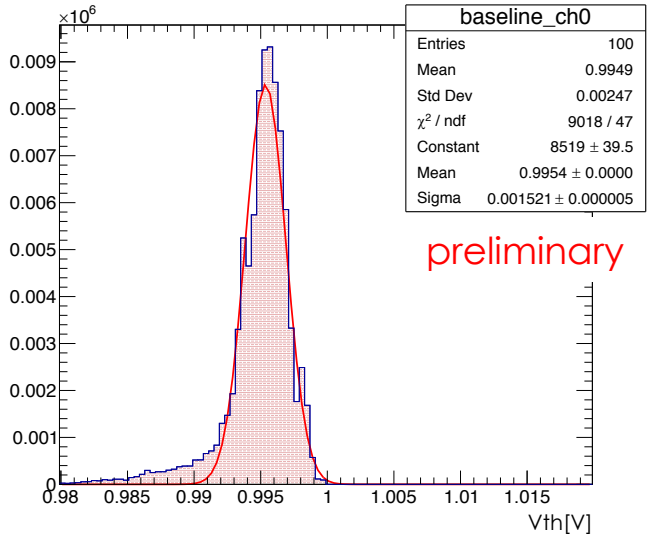
Threshold scan CH0-EVO1



S-curve CH0-EVO1



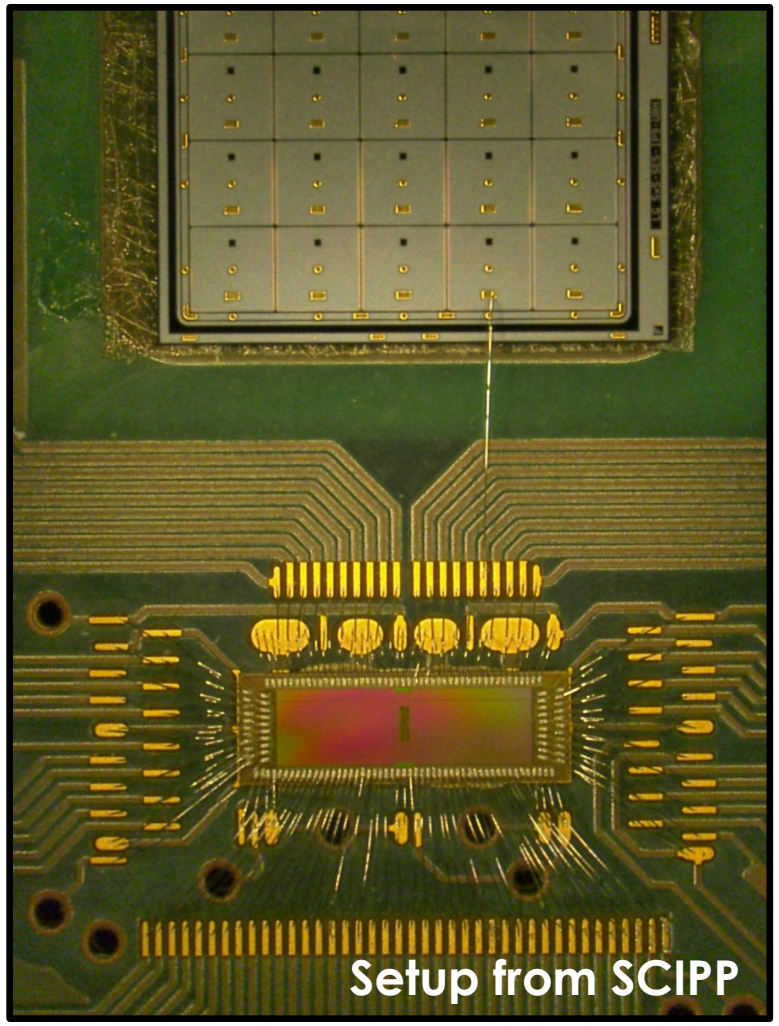
Baseline noise CH0-EVO1

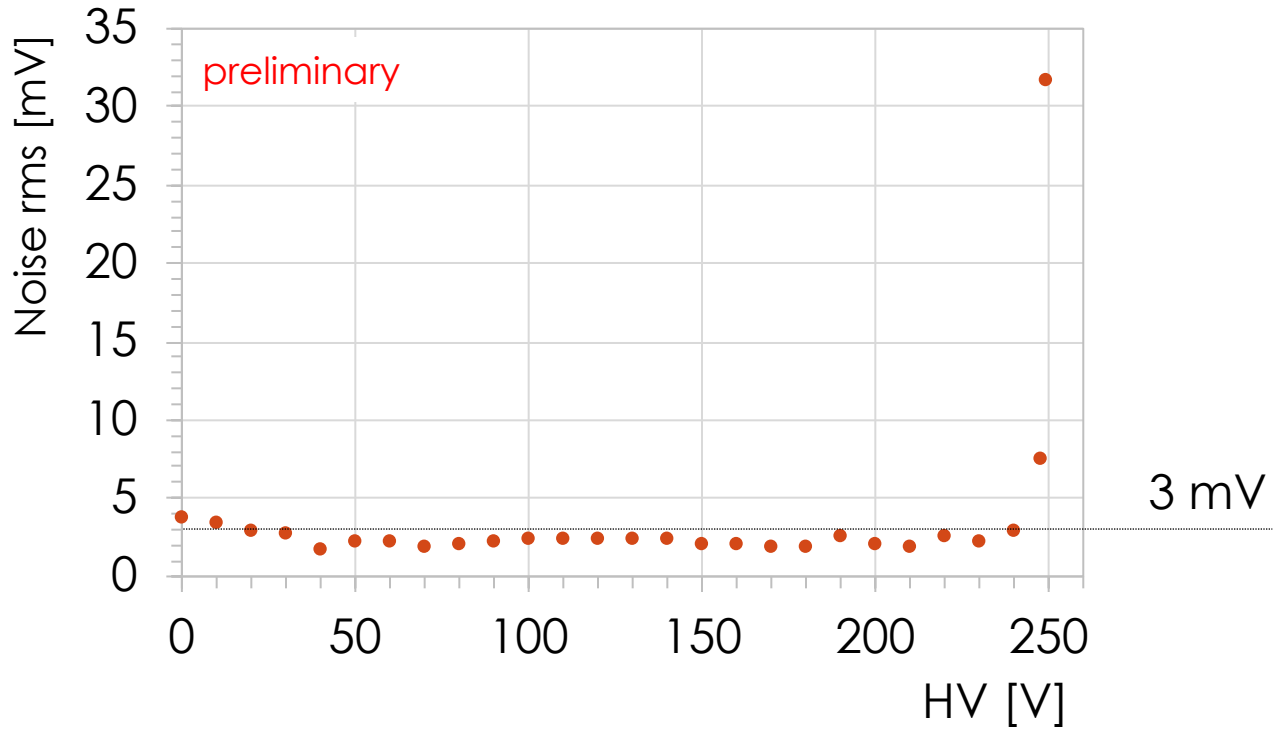


- Noise can be measured in the peak signal (1) or in the baseline (2)
- Noise is measured by performing a threshold scan in CH0 of EVO1. 1000 pulses are injected for each threshold and the number of pulses detected by the chip are counted by the FPGA
- According to the S-curve, **noise in the peak is 6.7 mV** (expected 6.2 mV)
- **Noise measured in the baseline** does not require the injection of pulses
- Noise mesured in the baseline is **1.5 mV** and is lower than what expected 3.1 mV. The gain may be different from what expected

Noise measurements (II)

FAST + HPK 3.1
ALTIROC sensor 5X5 (1.3x1.3mm^2)

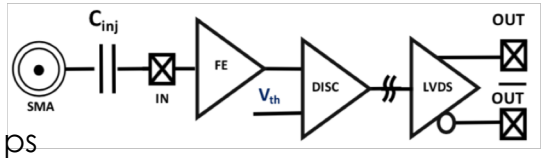




- Noise of EVO2 is measured for different sensor bias
- Sensor depleted @ 50V has a **capacitance of 3.8 pF**
- Noise is almost constant and around 3 mV even if the sensor capacitance changes
- Noise increases only @ **250 V** due to the **sensor breakdown**

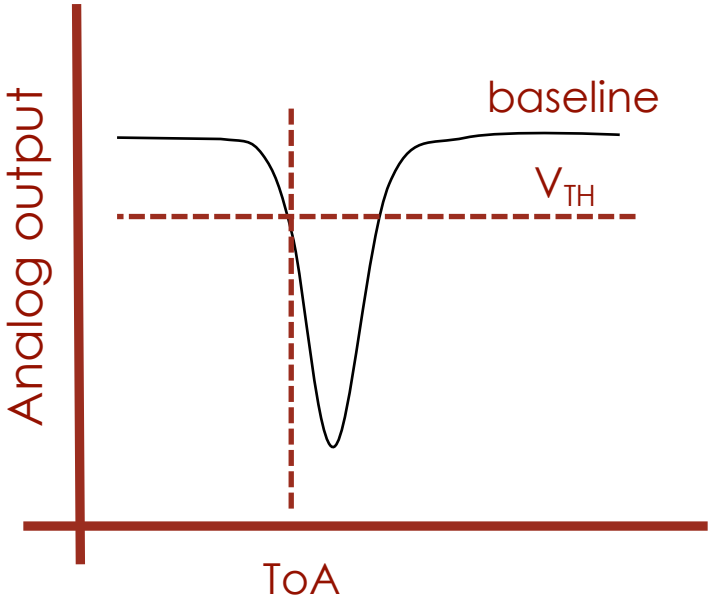
Rise time measurement

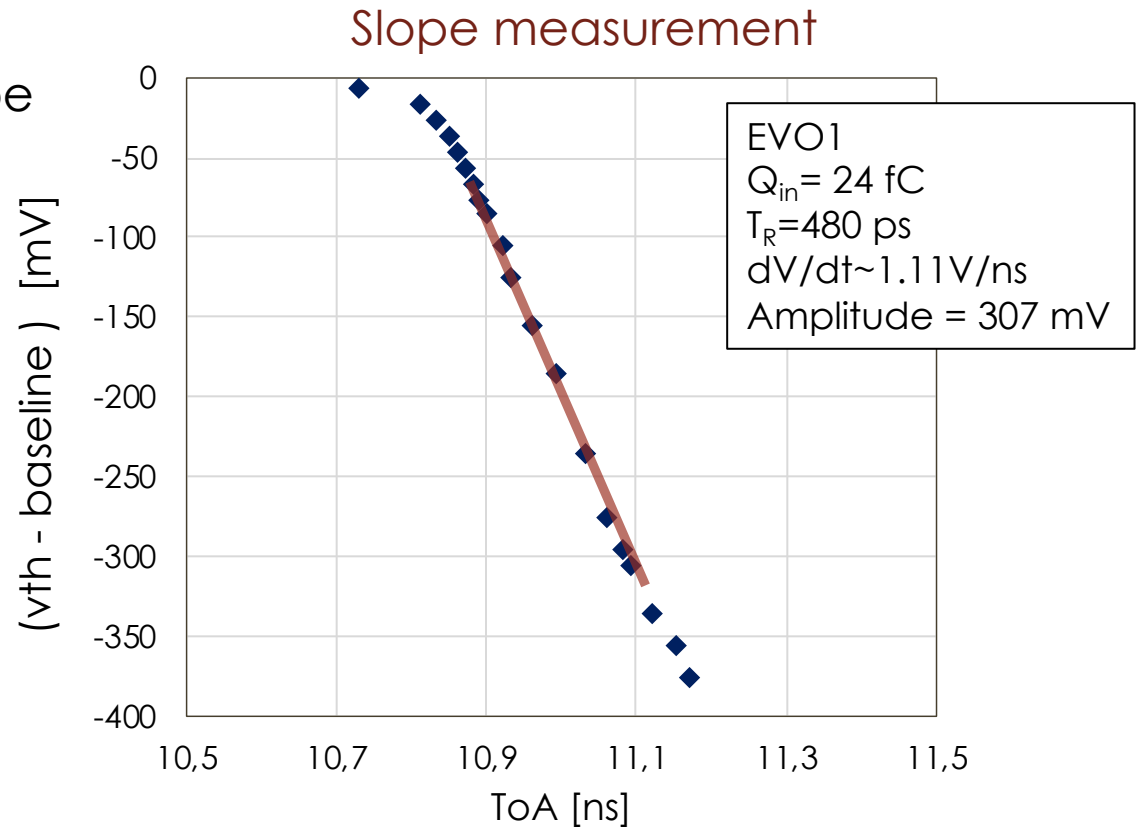
Pulser



Diff. probe

Pulser rise time = 500 ps





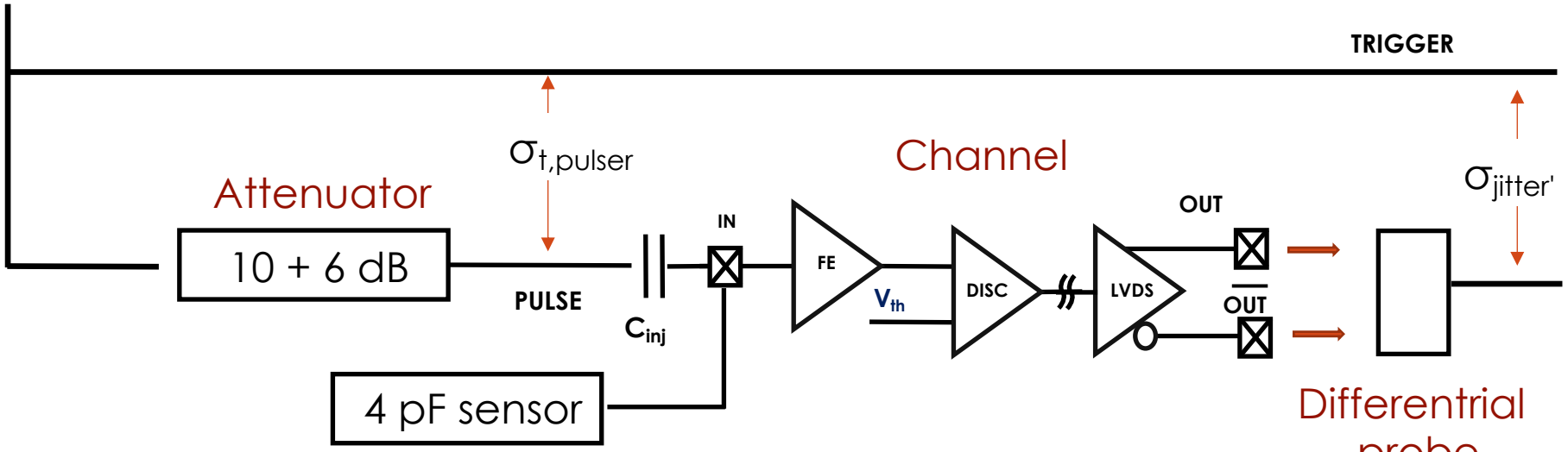
- Time of arrival (ToA) vs threshold measurement is done in EVO1 to measure the rise time T_R and the signal slope
- Injecting 24 fC through a 500 fF capacitance, the measured **rise time T_R is 480 ps** and the **slope is ~1.11 V/ns**
- Considering a noise of 3 mV, the **noise to slope ratio is 2.7 ps**
- **The signal amplitude** is measured to be around **307 mV** and sets the **front end gain** to **12.7 mV/fC**

Jitter measurement

Pulse generator

$$\sigma^2_{jitter} = \sqrt{\sigma^2_{jitter'} - \sigma^2_{t,pulse}}$$

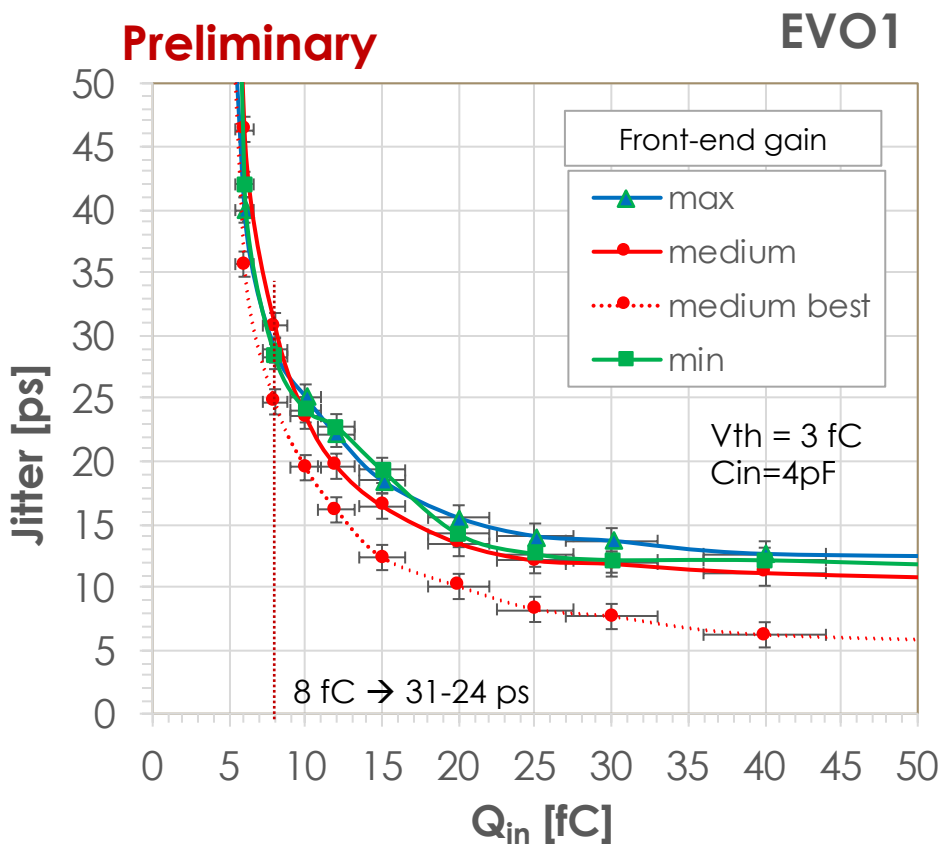
$\sigma^2_{t,pulse} \sim 2 - 15$ ps

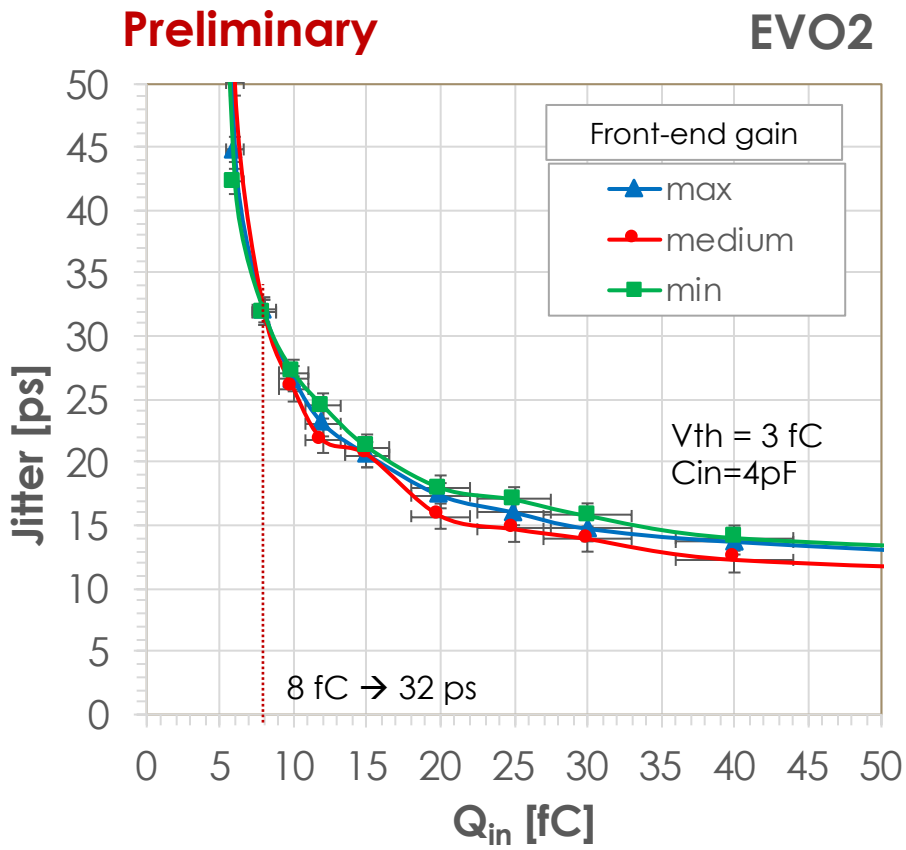


oscilloscope

- Only one channel of the pulser is used to provide both trigger signal and the pulse injection. This reduces the pulser contribution in the final jitter to few ps
- Trigger signal is sharp and has a large amplitude
- C_{det} is quite large (500 fF ±10%) and thus an attenuator in needed to inject charge around 8 fC

Jitter vs input charge





- **Different** values of front-end **gain** give the **same resolution** as expected from simulations
- **EVO1 and EVO2 are very similar** and they reach a minimum jitter of 12 ps
- **Electrical noise in the room** may affect the measurement. Data "medium best" shows an example of measurement in low noise condition. Jitter saturates to **5 ps at 50 fC**

6/6

Conclusions and future steps

- Three flavours of FAST have been designed in 110 nm CMOS technology exploring **different front-end amplifiers.** The prototypes have been received on **October 2019**
- Several simulations of the FAST chip coupled with UFSD have been carried out **including the most important contributions in time resolution**. Results are promising and fit the **30 ps time resolution also with 6 pF sensors**
- A **custom PCB has been designed** taking into account important design choices for high precision time measurements
- A dedicated data acquisition system has been developed for the full characterization. It is based on a Kintex-7 FPGA and a software developed in LabView (many thanks to R. Wheadon)
- Measured jitter in EVO1 and EVO2 for **8 fC** is around **30 ps** and can improve paying some attantion in noise in the setup. **Minimum jitter measured is around 5 ps**
- For the future:
  - Extend the characterization to more samples
  - **Time resolution measurements** by using laser sources and active sources
  - A test beam is planned on 2020

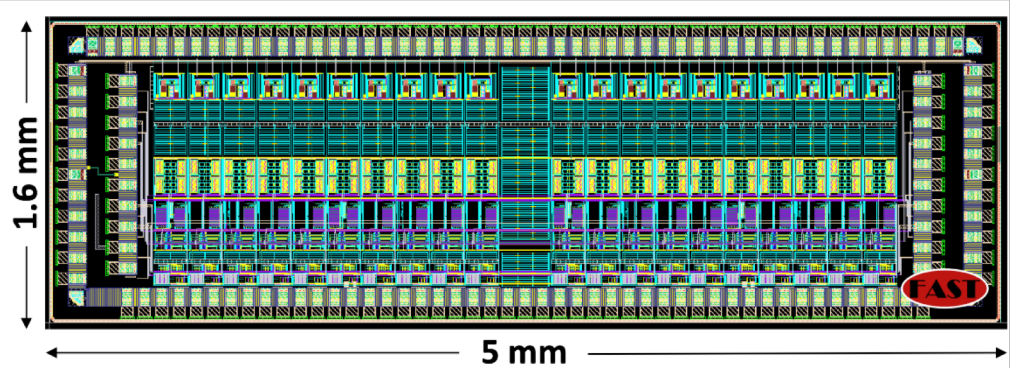
6/6

We kindly acknowledge the following funding agency:
Horizon 2020 Grant URC 669529 Ministero degli Affari Esteri, Italy, MAE

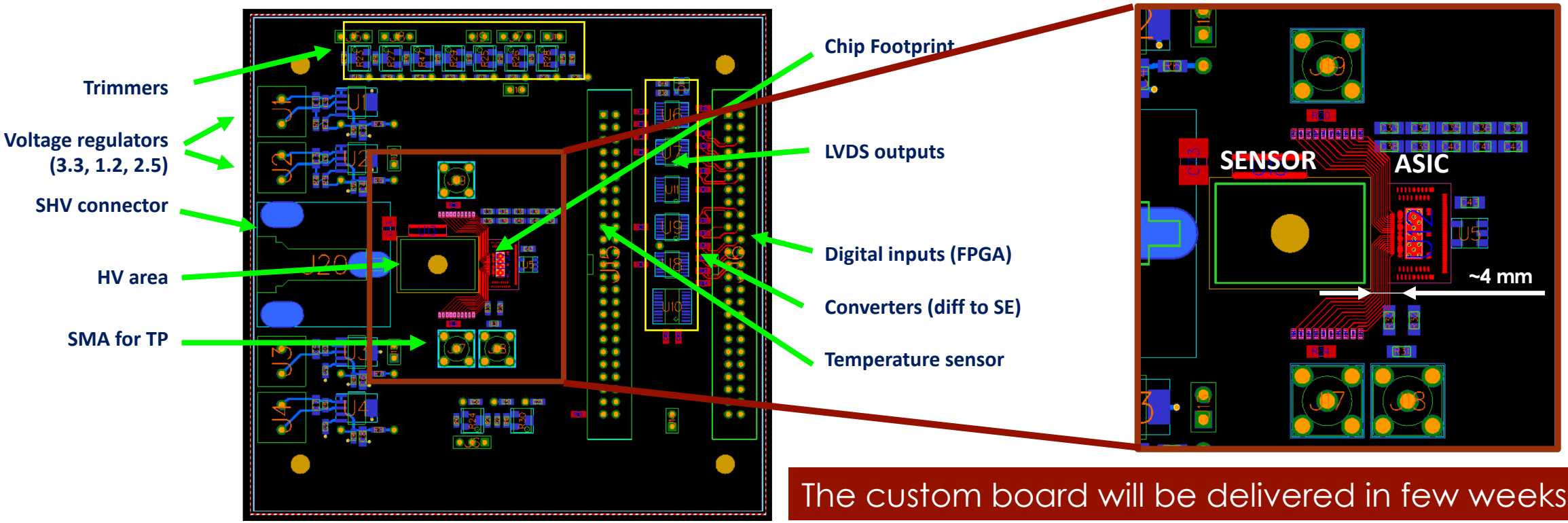
Thank you for your attention

Backup slides

Custom board for FAST

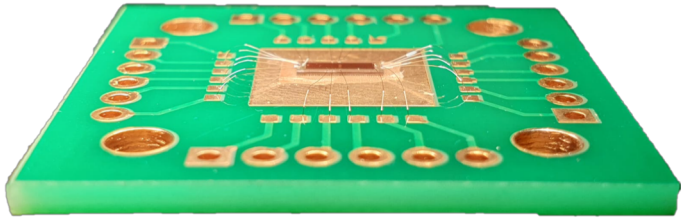


- Number of PADs: 140 (46 for the POWER)
- **Particular attention during the design** to reduce parasitics:
  - → wire bonding lenght <0.5 cm
  - → wire diameter of 25 µm
  - → 2 bondings/PAD can be done

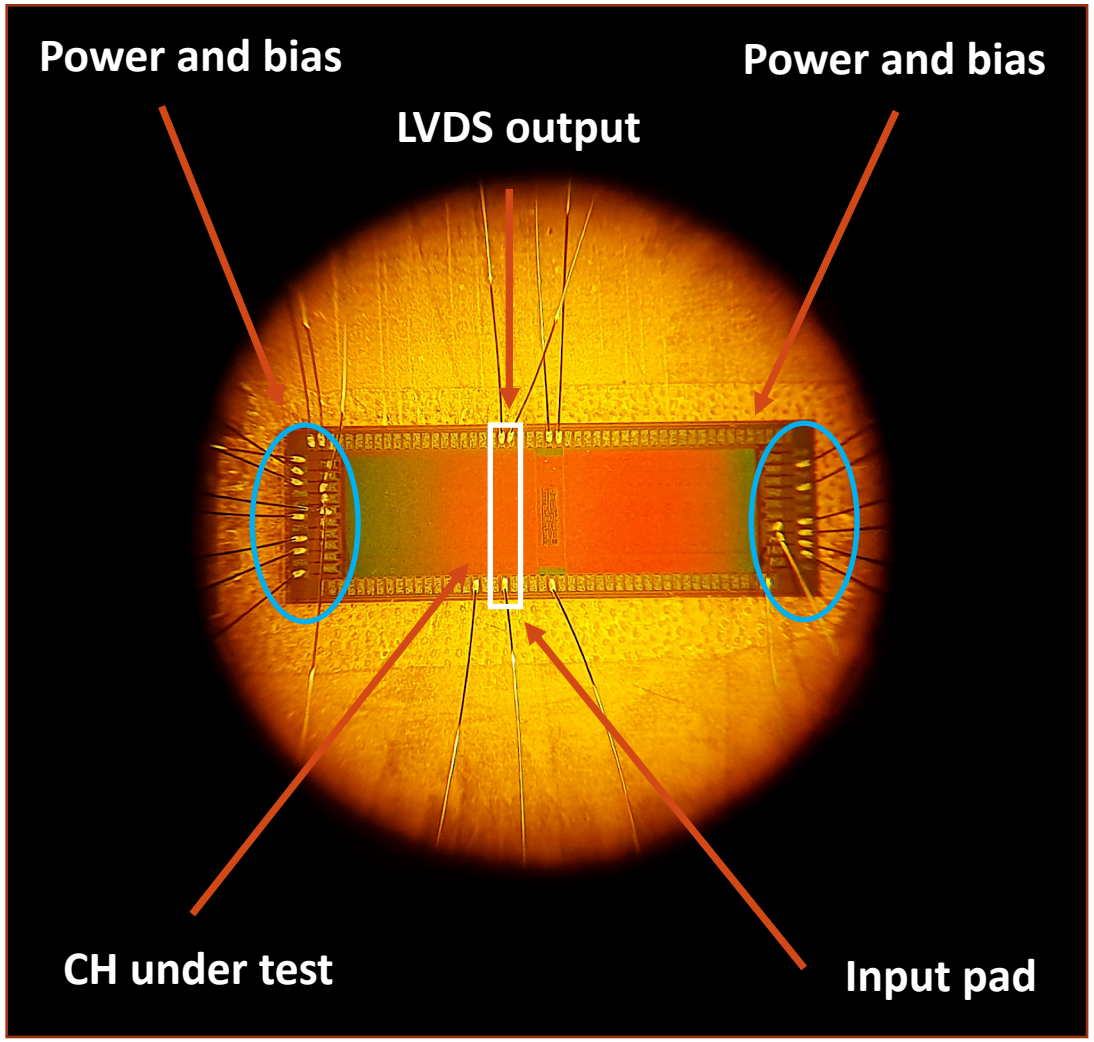


The custom board will be delivered in few weeks

First basic setup with FAST



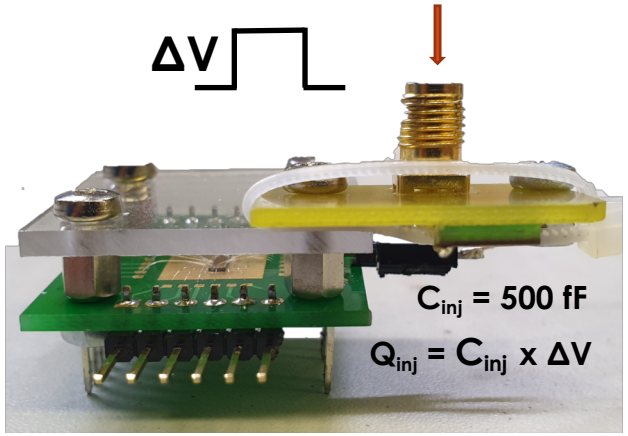
- FAST prototypes delivered on October 2019
- A general purpose board has been used for the first basic tests
- Connection for basic tests:
  Power lines: 1.2 V (ANA and DIG) and 2.5 V (IO)
  Biases: I & V
  IN/OUT of a channel

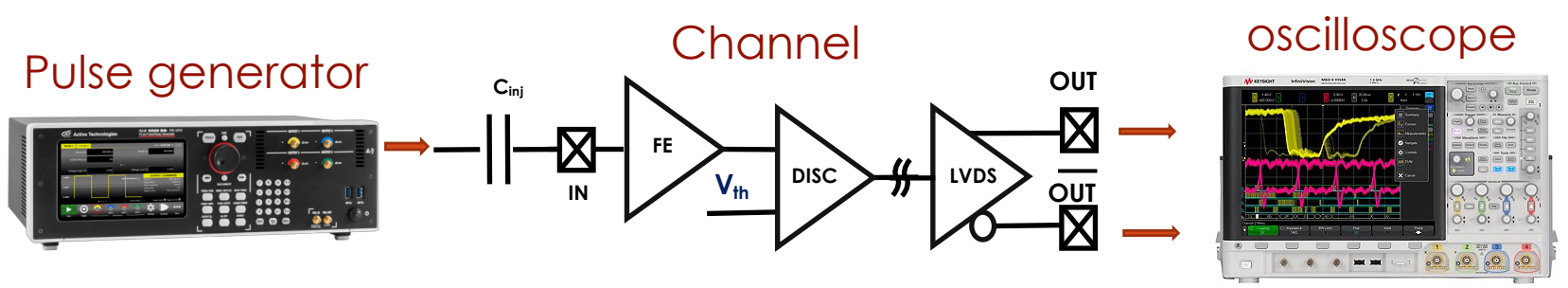


Power consumption

Domain	Expected	Measured
Anag & Dig 1.2V	62 mA	60 mA
IO 2.5 V	18 mA	20 mA

Test with charge injection





- A small carrier board is used to mount C_{inj} and a SMA connector
- Vth is provided by one pin on the PCB

Voltage response to a injected pulse

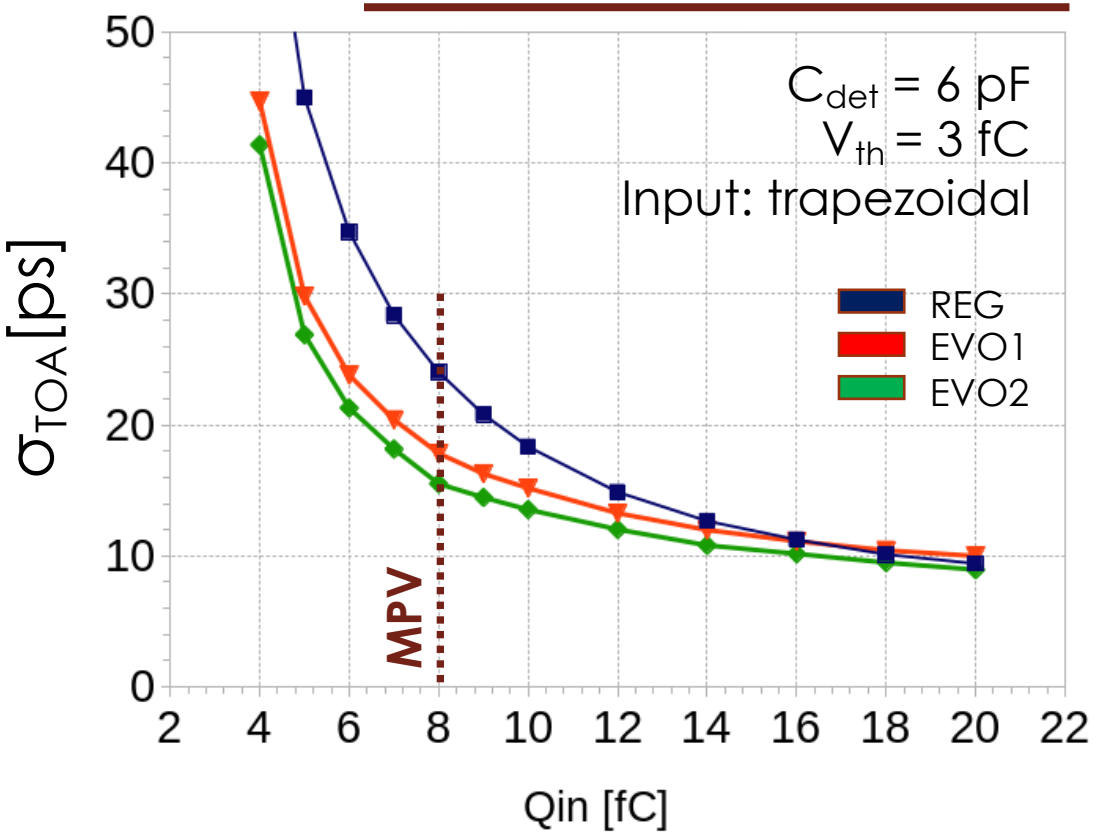
- First threshold scan shows a **peak-to-peak noise of 10 mV** in good agreement with simulations
- The first test allows to see that the entire chain is properly working
- The system has a lot of **antennas** (to be optimized), so interference should be reduced
- The setup is enough to test some block of FAST but not to measure time resolution

Jitter vs Charge

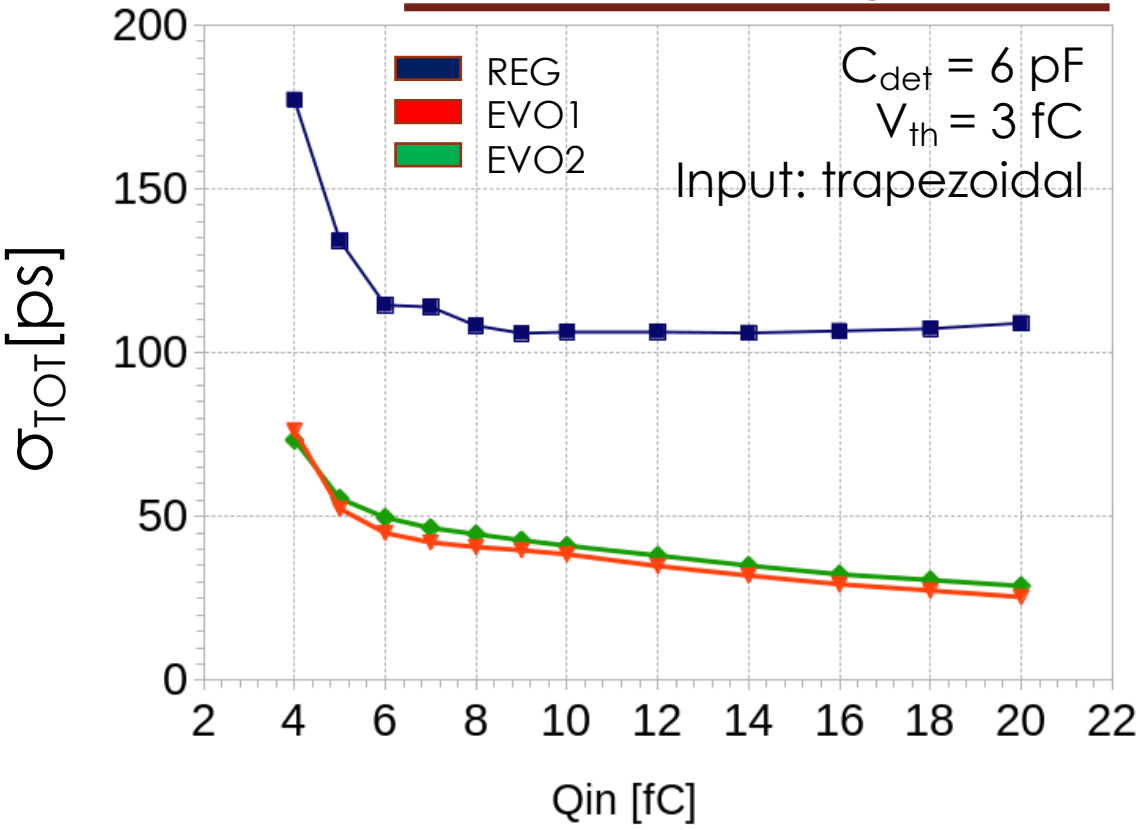
Dependency from input charge

- 1 proton MIP release Q in silicon according to **the Landau distribution**
- LE-discriminator is used, ToA and then also jitter depend on Q_{in} → a corretion is needed

jitter vs Q_{in}



σ_{TOT} vs Q_{in}

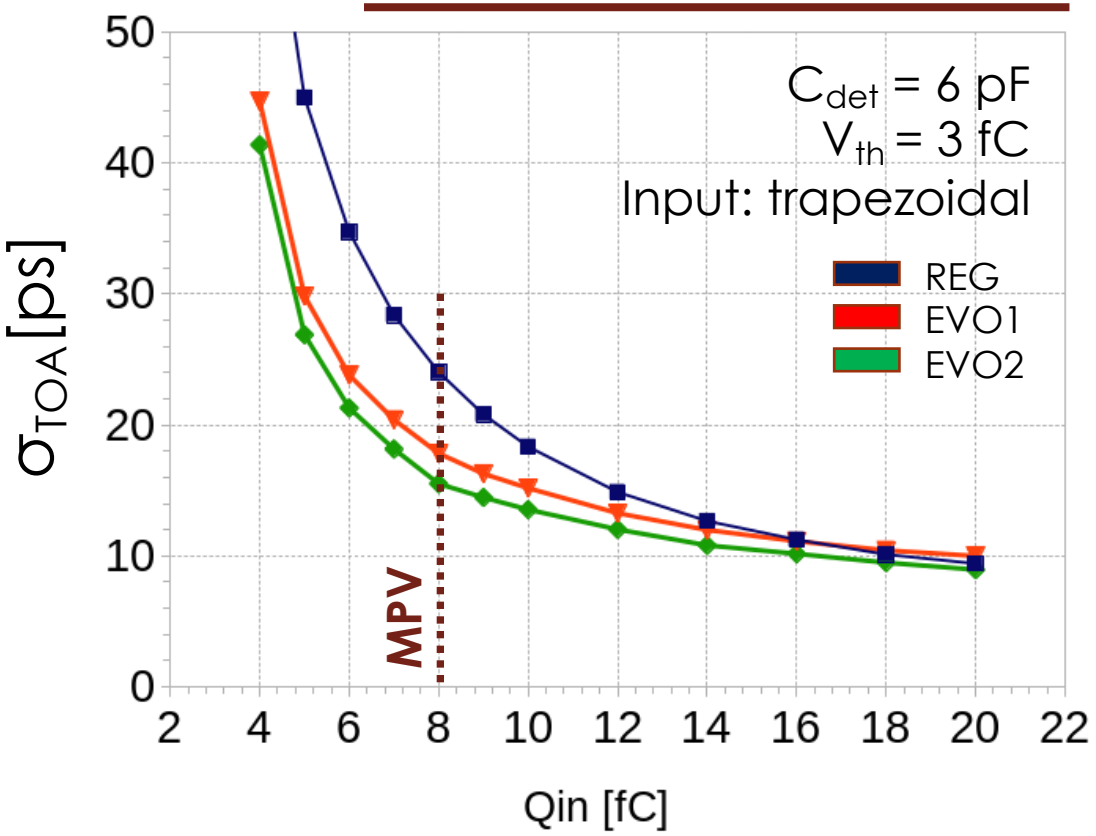


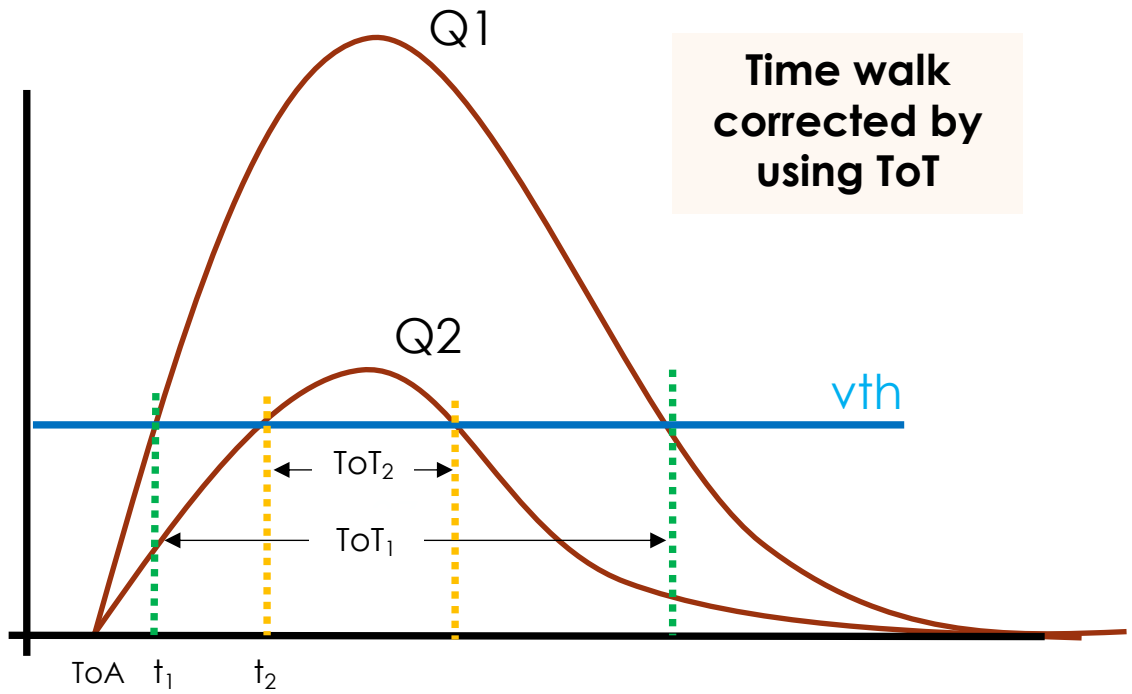
Front-end outputs comparison

Dependency from input charge

- 1 proton MIP release Q in silicon according to **the Landau distribution**
- LE-discriminator is used, ToA and then also jitter depend on Q_{in} → a corretion is needed

jitter vs Q_{in}





Time walk corrected by using ToT

ToT should be measured with good accuracy to make a precise correction → **Short tails are preferred**

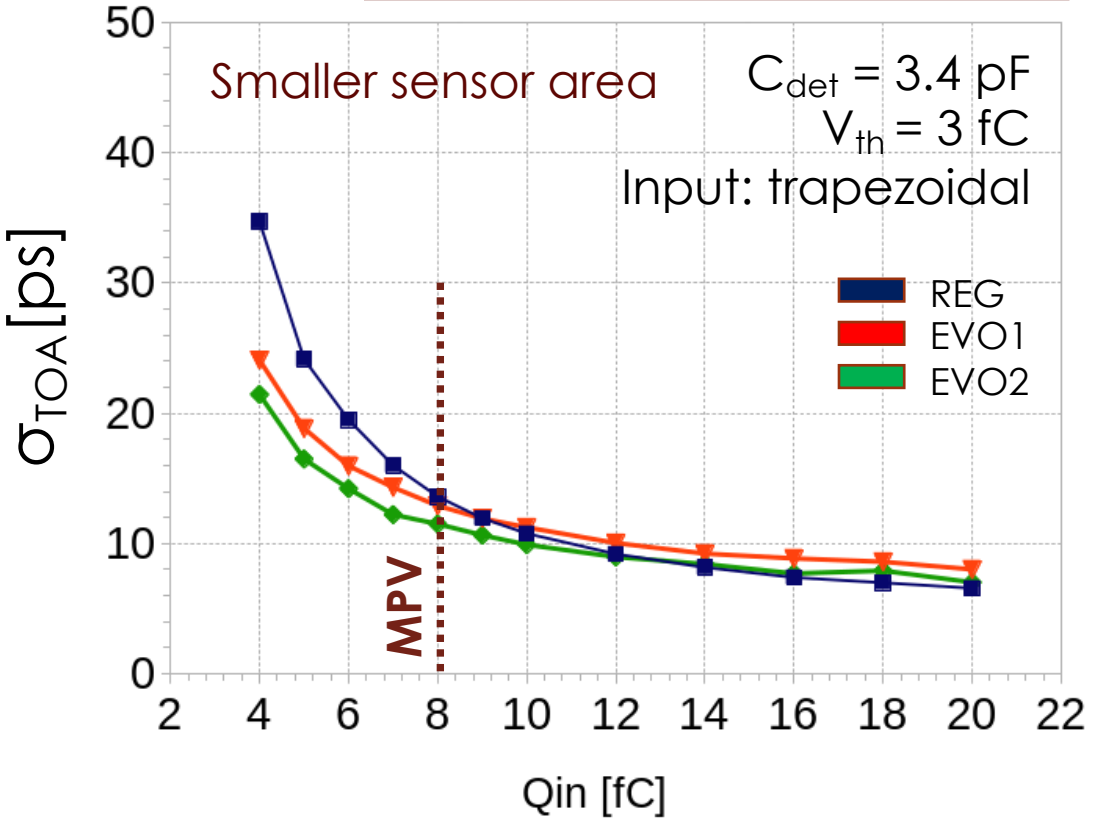
Front-end outputs comparison

Dependency from input charge

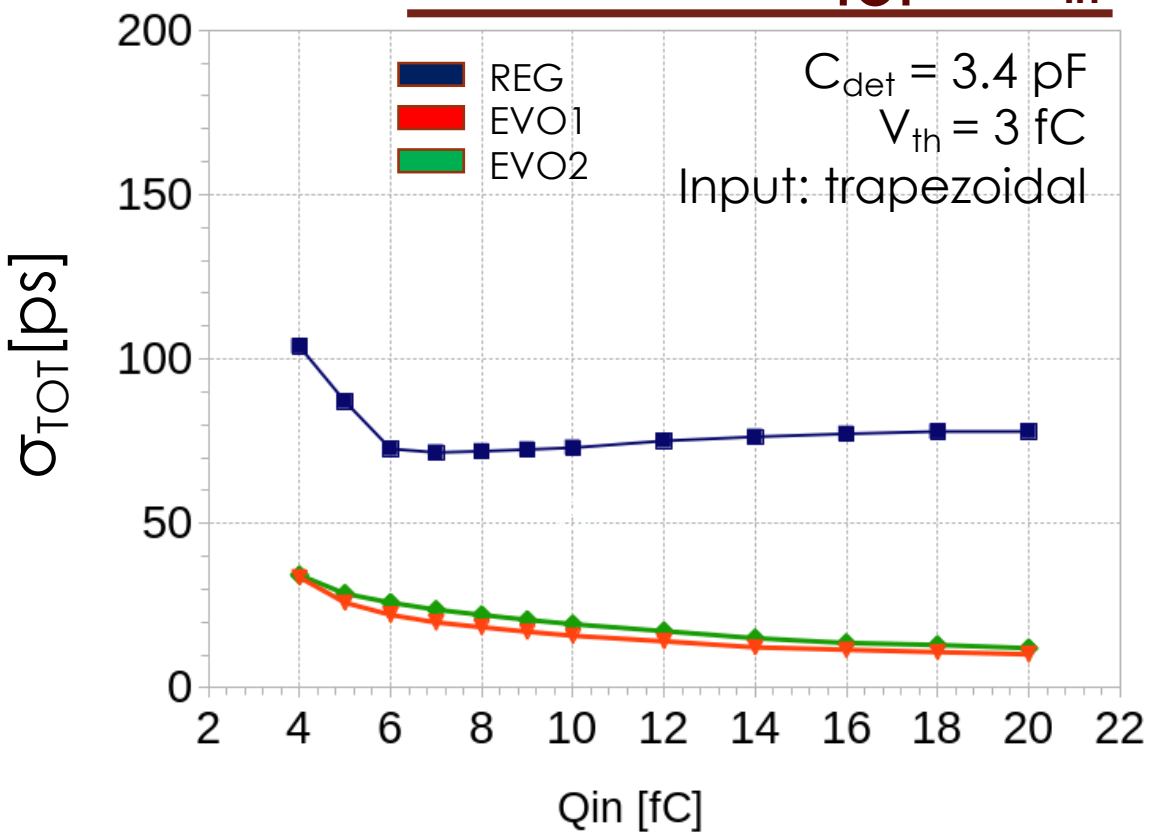
Smaller is the sensor, smaller is the jitter

- 1 proton MIP release Q in silicon according to **the Landau distribution**
- LE-discriminator is used, ToA and then also jitter depend on Q_{in} → a corretion is needed

jitter vs Q_{in}



σ_{TOT} vs Q_{in}

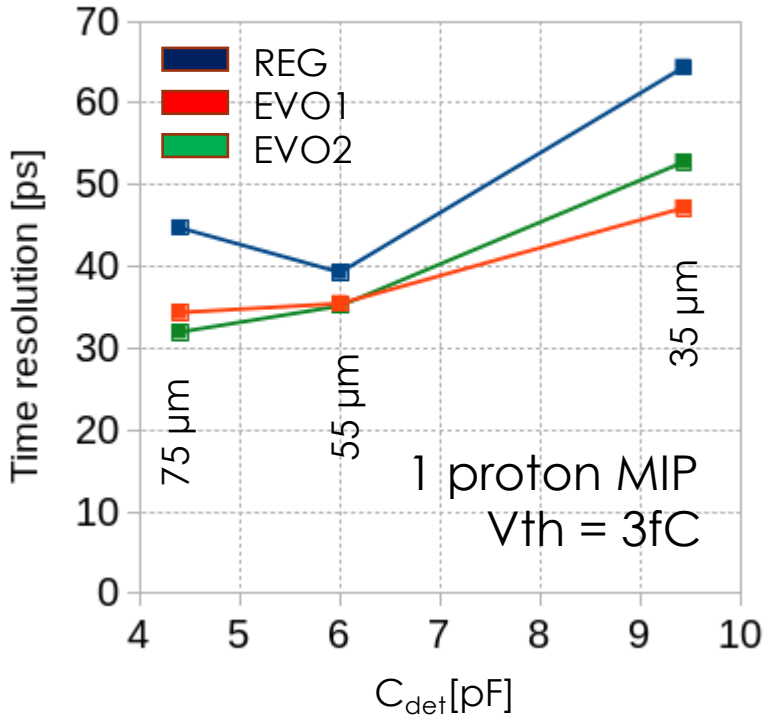


Time resolution vs sensor area and thickness

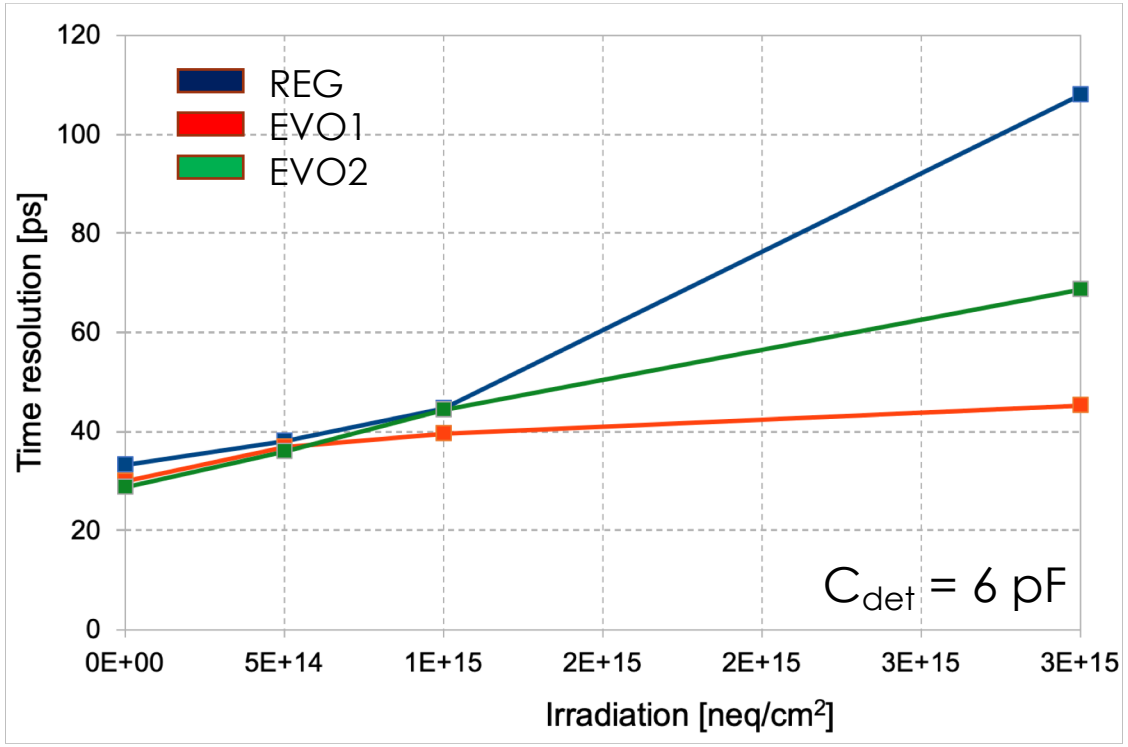
- Study done playing with three important parameters:
  - → **Sensor thickness**: 35 µm, 55 µm, 75 µm
  - → **Sensor geometry**: 1x1 mm^2, 1.3x1.3 mm^2 and 1x3 mm^2
  - → **Front-end**: REGULAR, EVO1 and EVO2

→ 3 values of C_{det}

Area = 1x3 mm^2



Time resolution with irradiated sensor

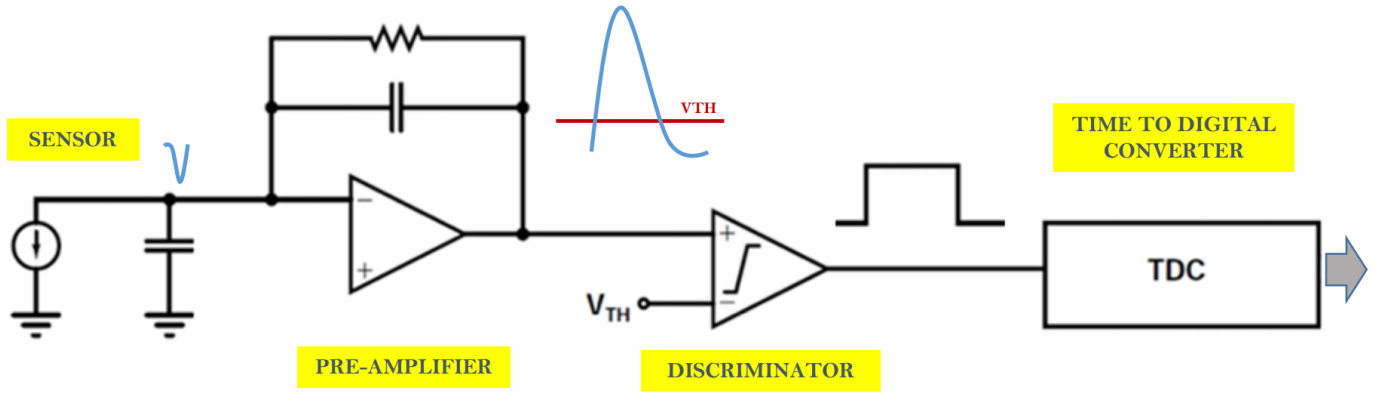


FBK 55 μm (Boron + Carbon)

- The effect of radiation in silicon affects the collected charge. This effect is taken into account
- **Time resolution for non-irradiated sensors** is around **30 ps**
- EVOs measure always time more precicely than REG
- FAST + FBK allows to maintain a time resolution below 50 ps up to $1x10^{15}$ n_{eq}/cm^2
- Leakage current is not included in this simulations

Picosecond time resolution: what is needed?

Fast front-end electronics



- **Jitter** is minimized minimizing noise and increasing the dV/dt term
- Noise can be minimized in case: $\mathbf{T_{rise} \sim T_{collection}}$
- Noise depends on several factors like: **sensor cap**, **bandwidth**, **front-end topology**
- Electronics contribution: front-end, TDC and the time walk

Front end TDC Sensor

$$\sigma_t^2 = \left(\frac{N}{\frac{dV}{dt}}\right)^2 + \left(\frac{\delta_{Bin}}{\sqrt{12}}\right)^2 + \sigma_{Time\ Walk}^2$$

- The contribution from TDC is very small compared to the other terms
- **Time walk** can be reduced by using **CFD** or it can be corrected offline with particular techniques
- Going to the transistor level, time resolution is technology dependent

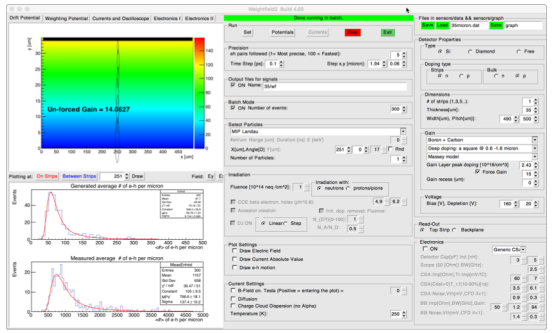
Time resolution simulations

System level simulation

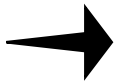
$$\sigma_t^2 = \sigma_{LANDAU\ NOISE}^2 + \sigma_{DISTORTION}^2 + \sigma_{JITTER}^2 + \cancel{\sigma_{TDC}^2} + \sigma_{TIME\ WALK}^2$$

- **Simulations include effects on silicon** like Landau noise and signal distorsion (Weightfield2)
- Weightfield2 in combination with EDA tools to simulate the entire system

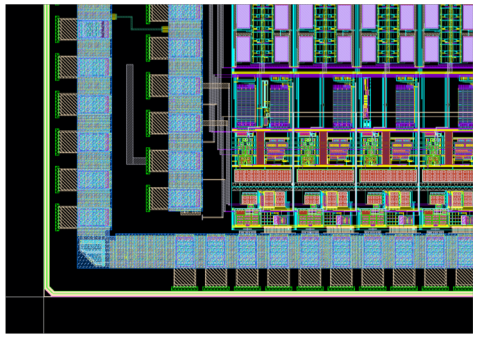
Weightfield



Skill language



EDA tools



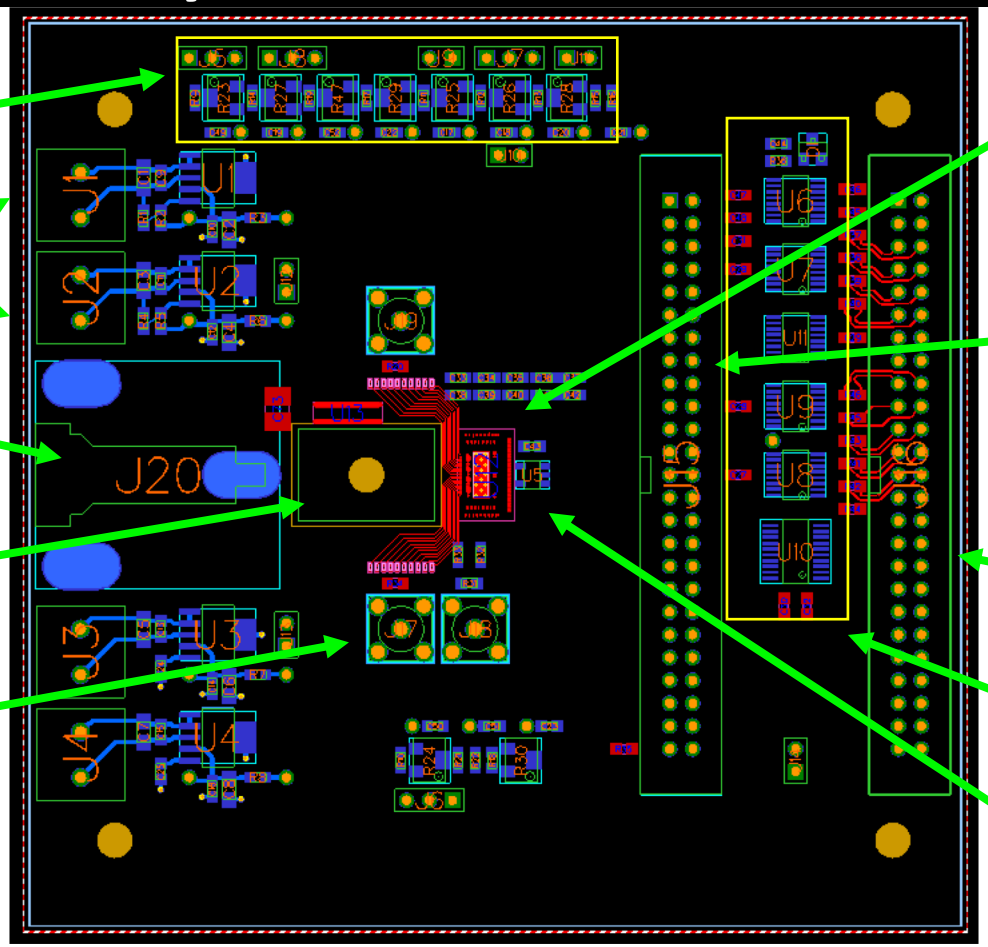
What is included in this simulations?

- Landau distributed input signal
- Transient noise simulations
- R-C-CC parasitics included
- 2 different tools used for the parasitic extraction

- Time walk is corrected offline
- The TDC contributes with a systematic effect

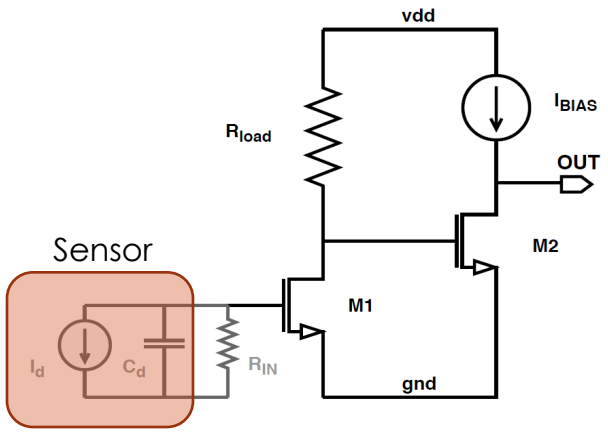
Custom PCB for FAST

PCB layout

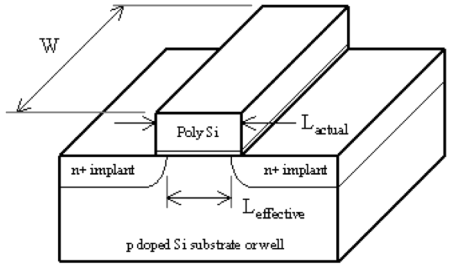


The technology choice in timing applications

Broad-band amplifier

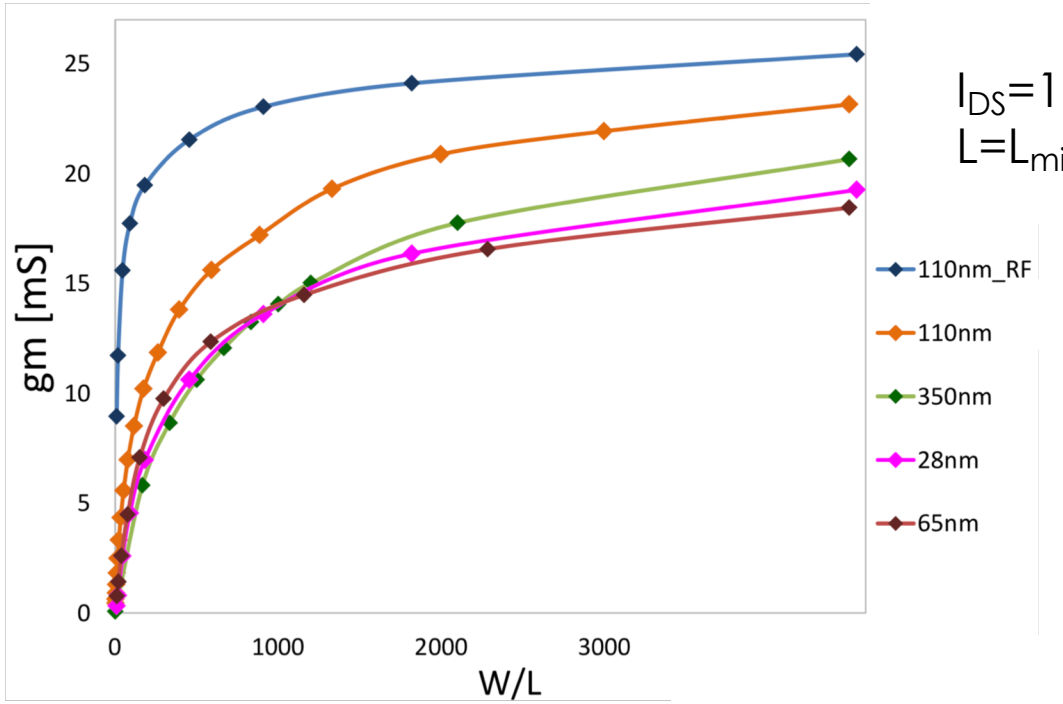


$$\sigma^J_t = \frac{C_d}{Q_{in}} \sqrt{\frac{2KT}{g_{m1}}}\, t_d$$



- Jitter depends on the **trasconductance g_m**
- g_m in general is not a technological parameter, but it can be consider a good parameter to compare different tecnologies fixing some parameters like power consumption
- The comparison shows that fixing the power consumption to 1 mW, the gm is higher in 110 nm CMOS technology

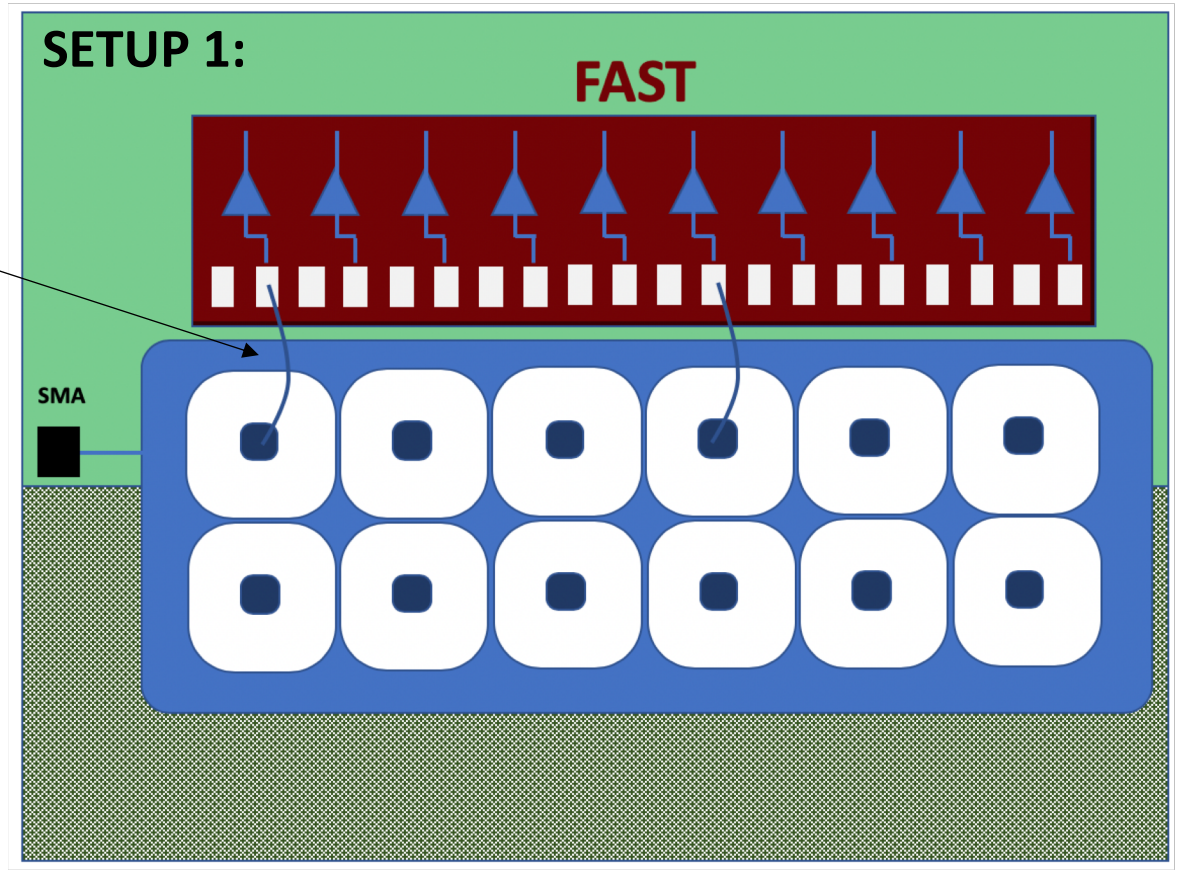
Comparison between CMOS tecnologies



I_{DS}=1 mA
L=L_{min}

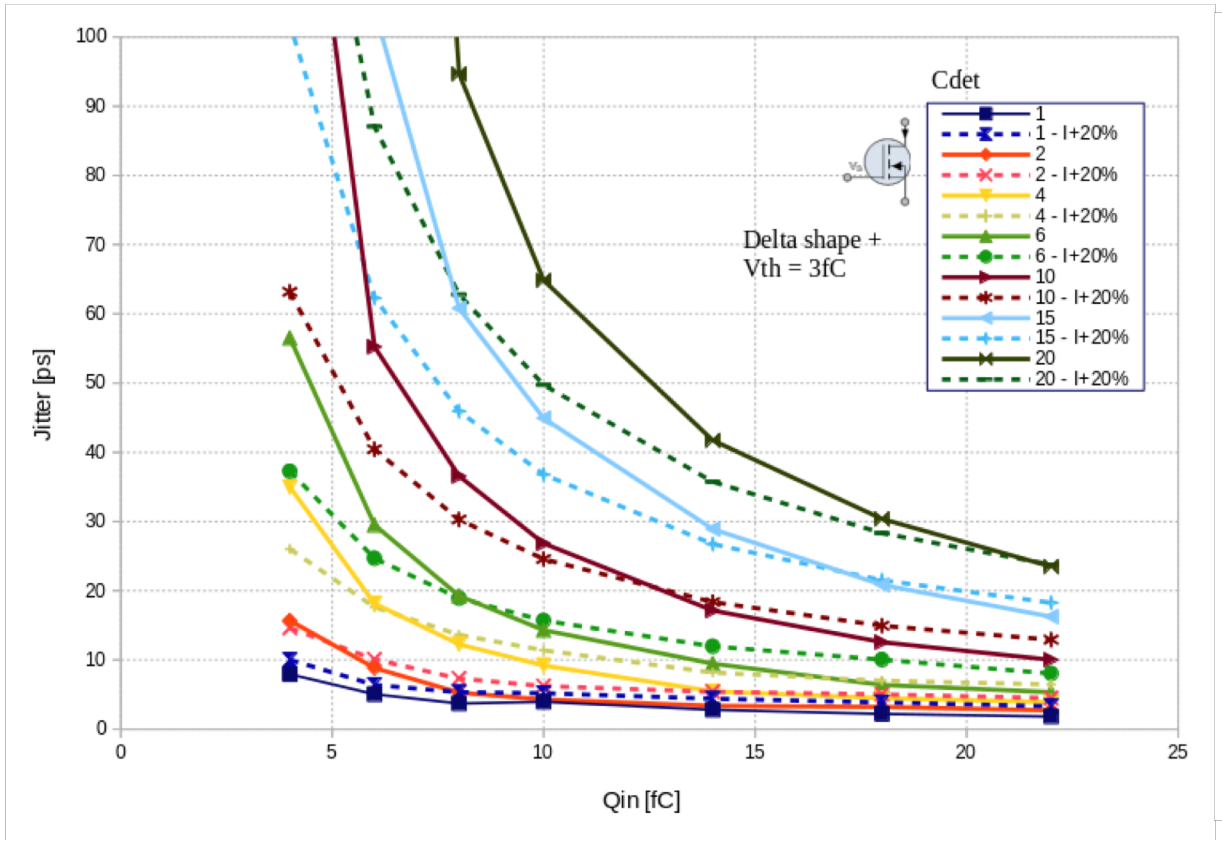
Scheme for wire bonding

PCB for FAST: INPUT PADs

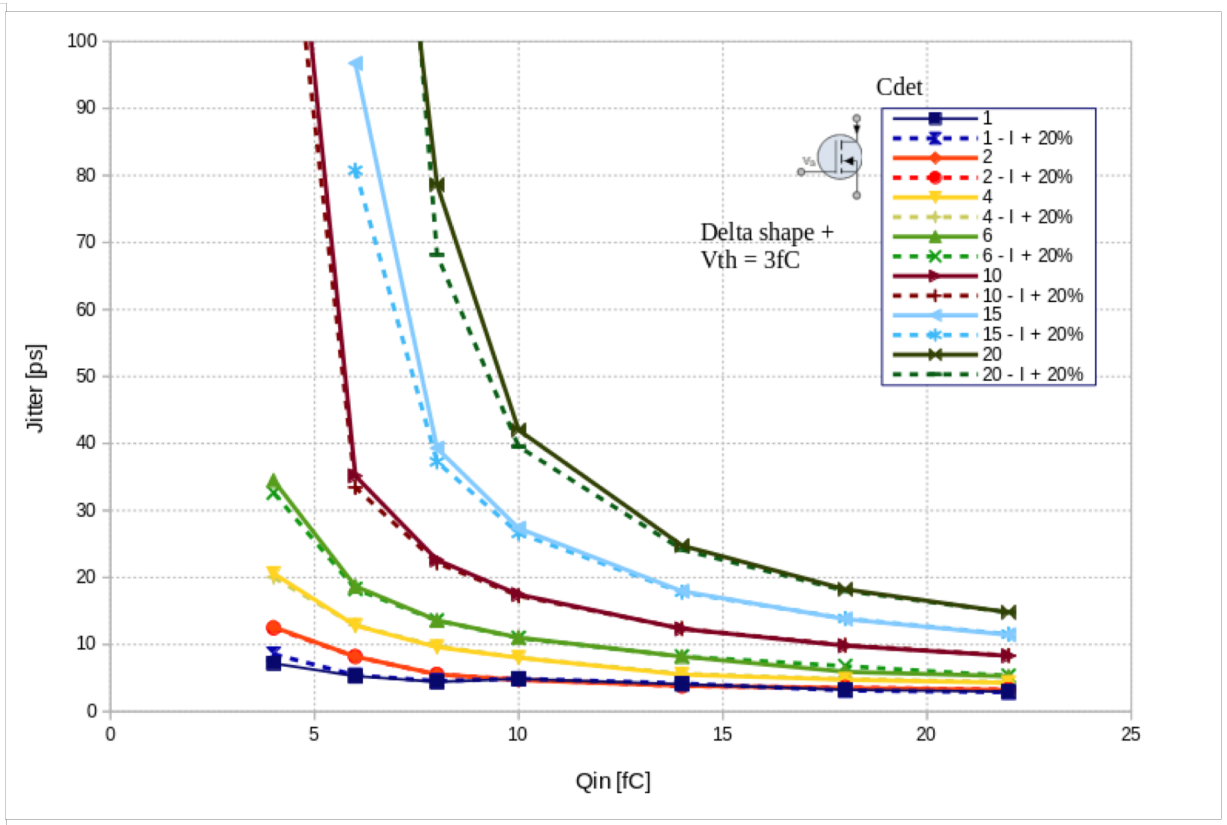


Jitter vs input charge in case of extra power

FAST REG



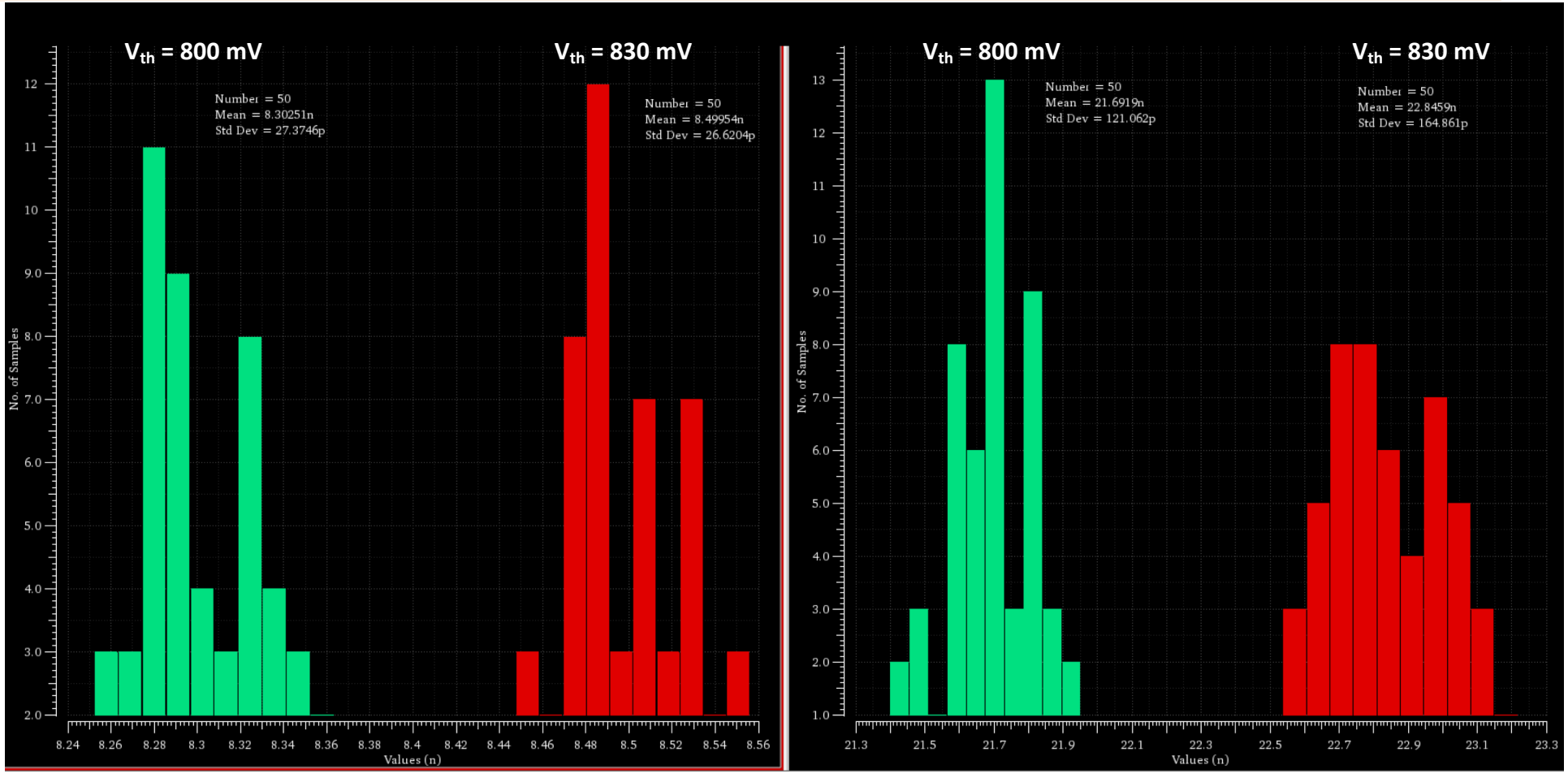
FAST EVO1



1 2 3

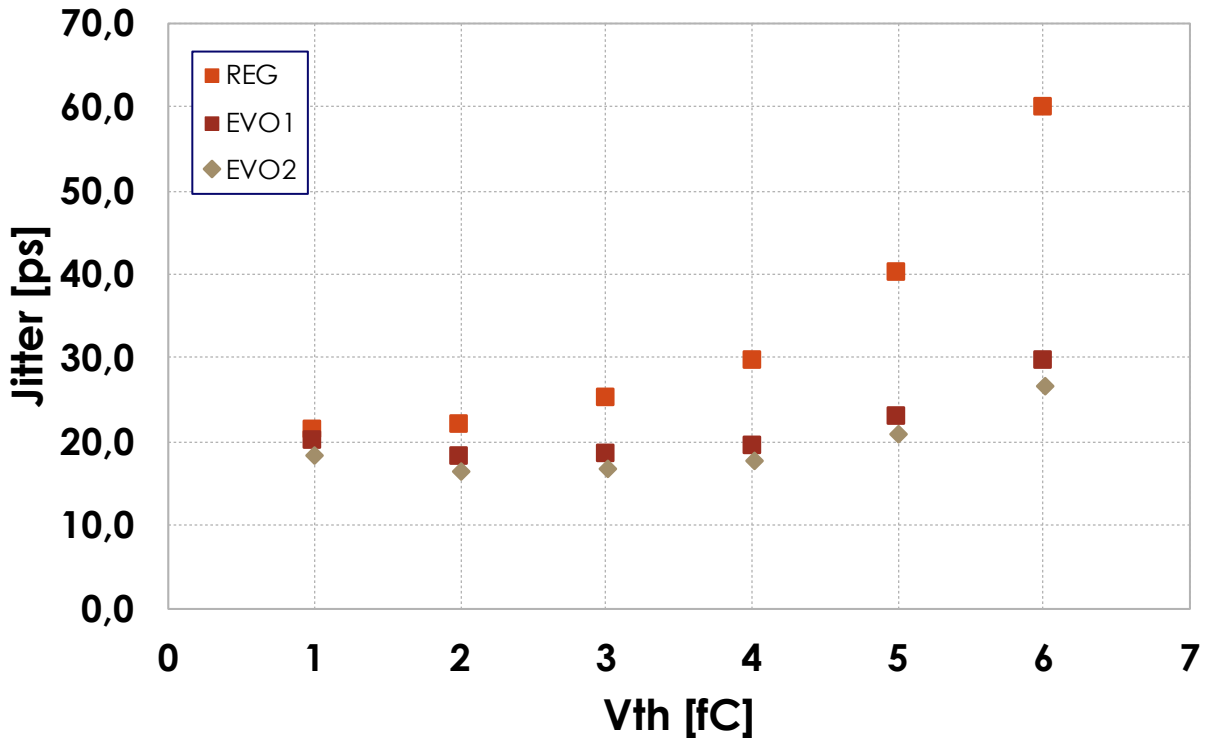
ToA

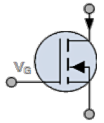
ToT



- The time resolution in this condition is 26 - 27 ps. The optimum for the MPV must be find
- More than 50 runs are required to estimate the resolution with good accuracy
- Wire bonding is modeled by means of an inductance of 2 nH (worse case)

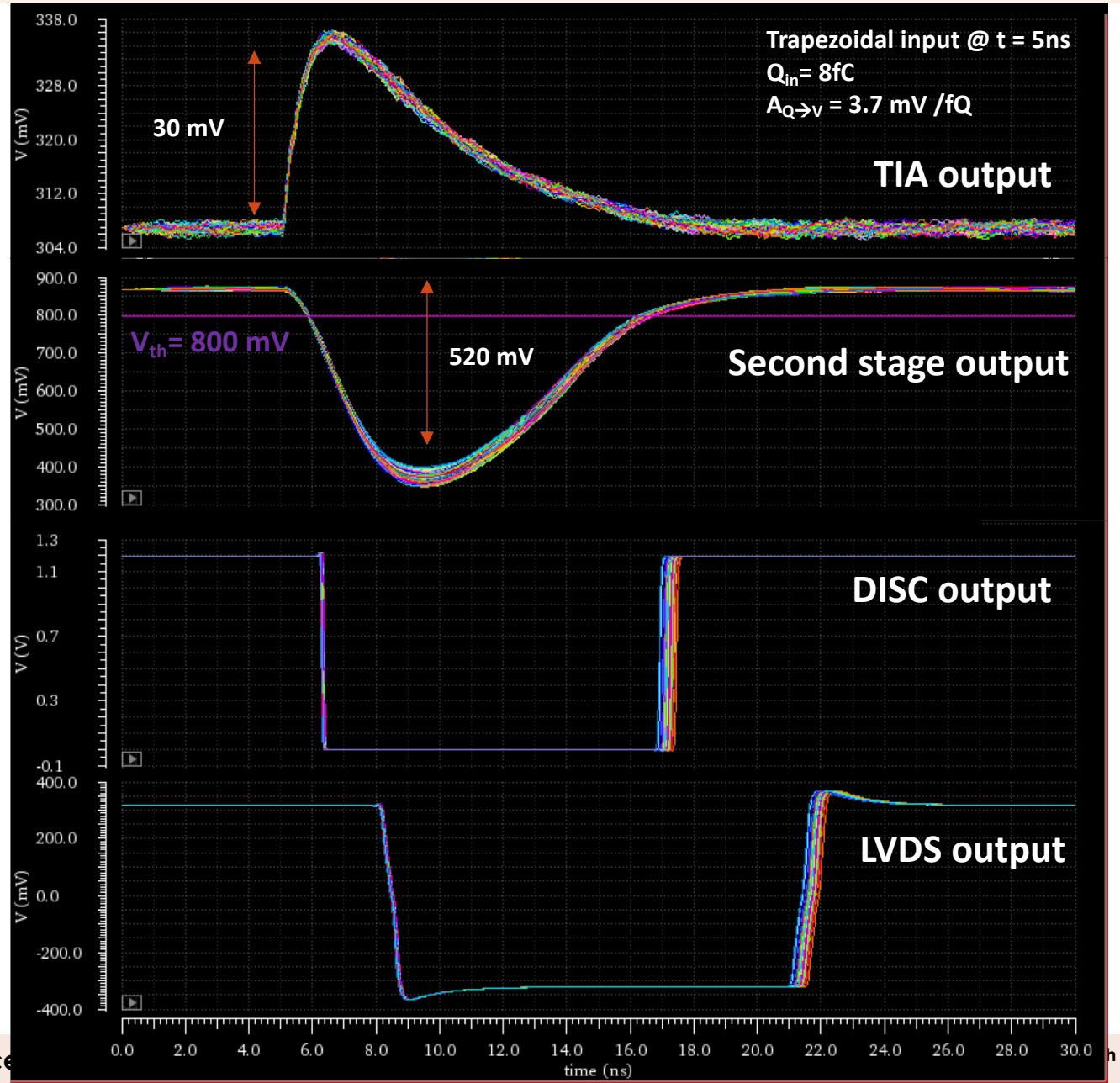
Jitter vs threshold



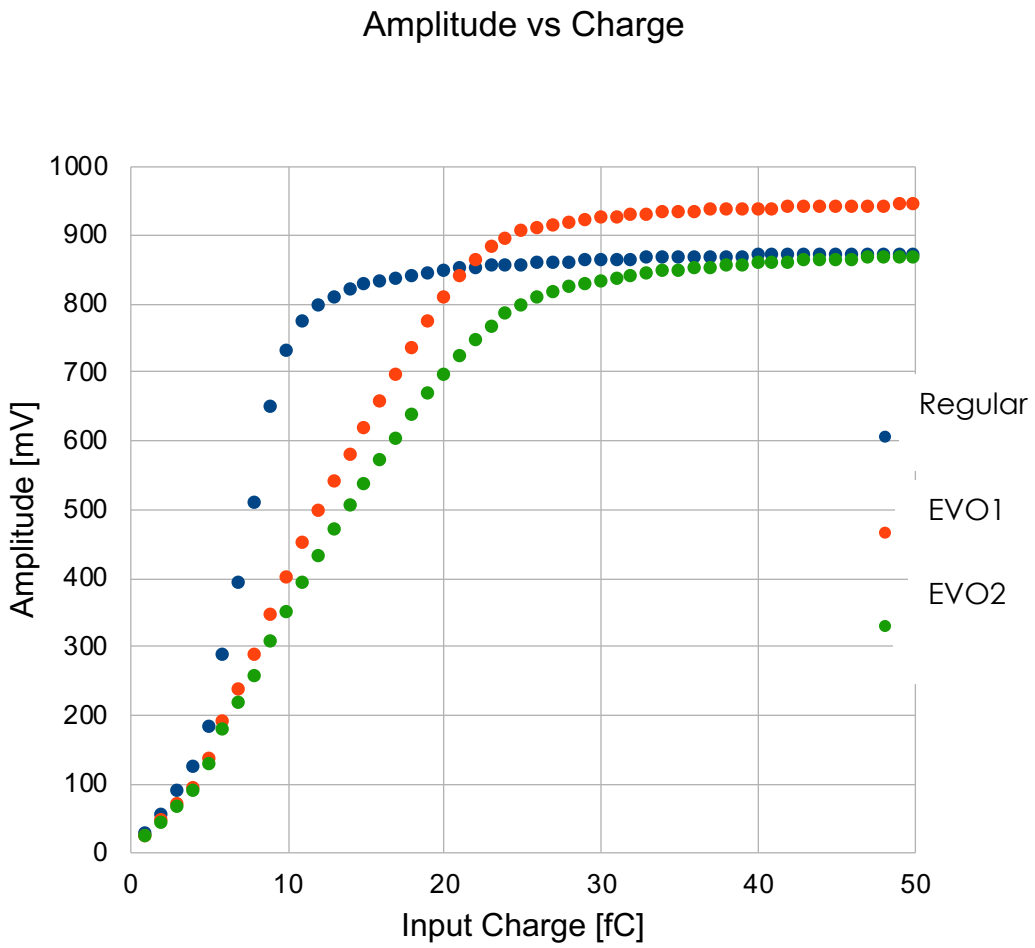


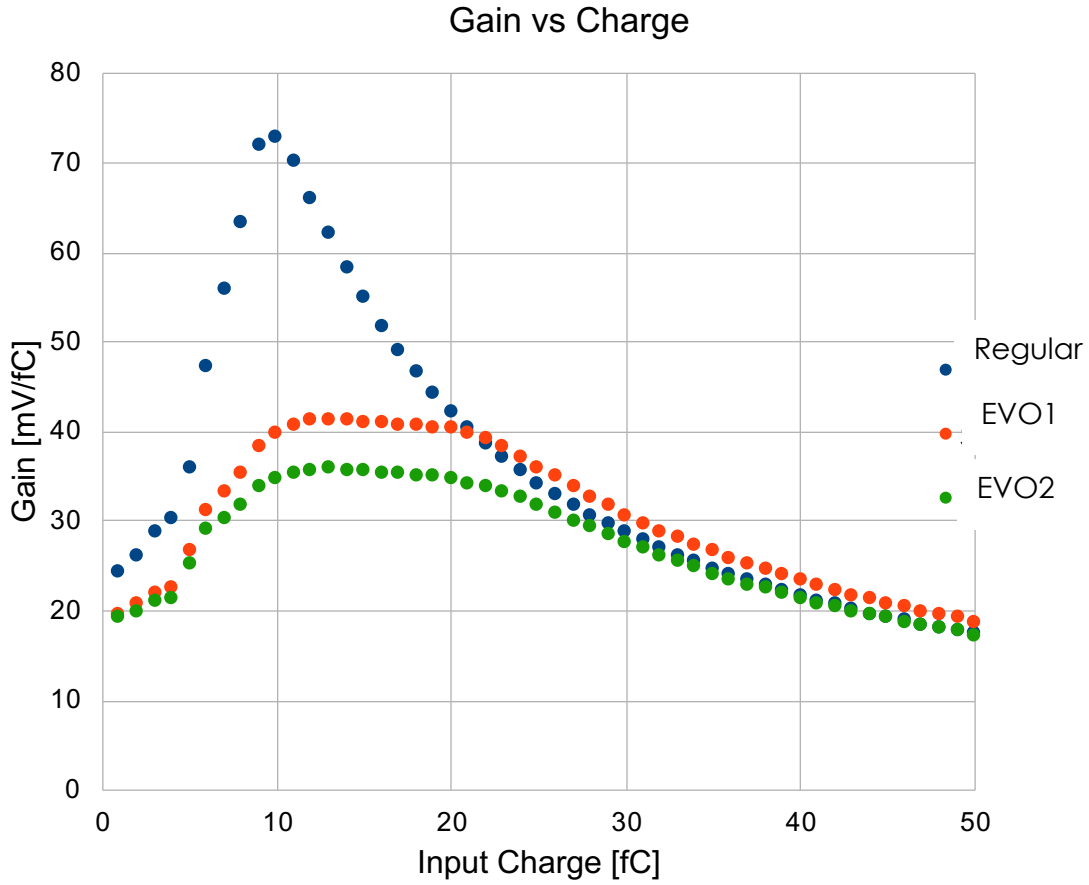
Cdet = 6 pF
Qin = 8 fC (trapezoidal)
Ibias = 1mA
T = 27 °C
Regular Rf = 20 K
EVO Rf = 11.6 K

Transient noise with R-C-CC-L parasitics

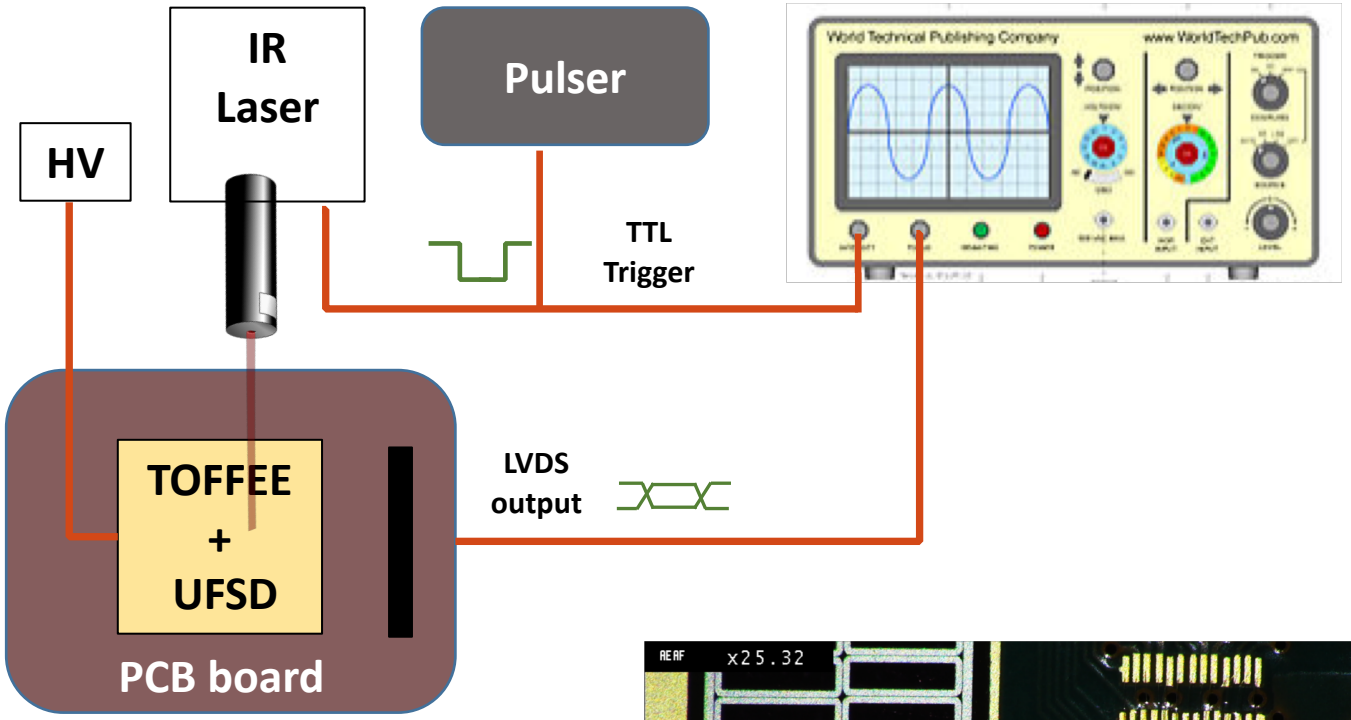


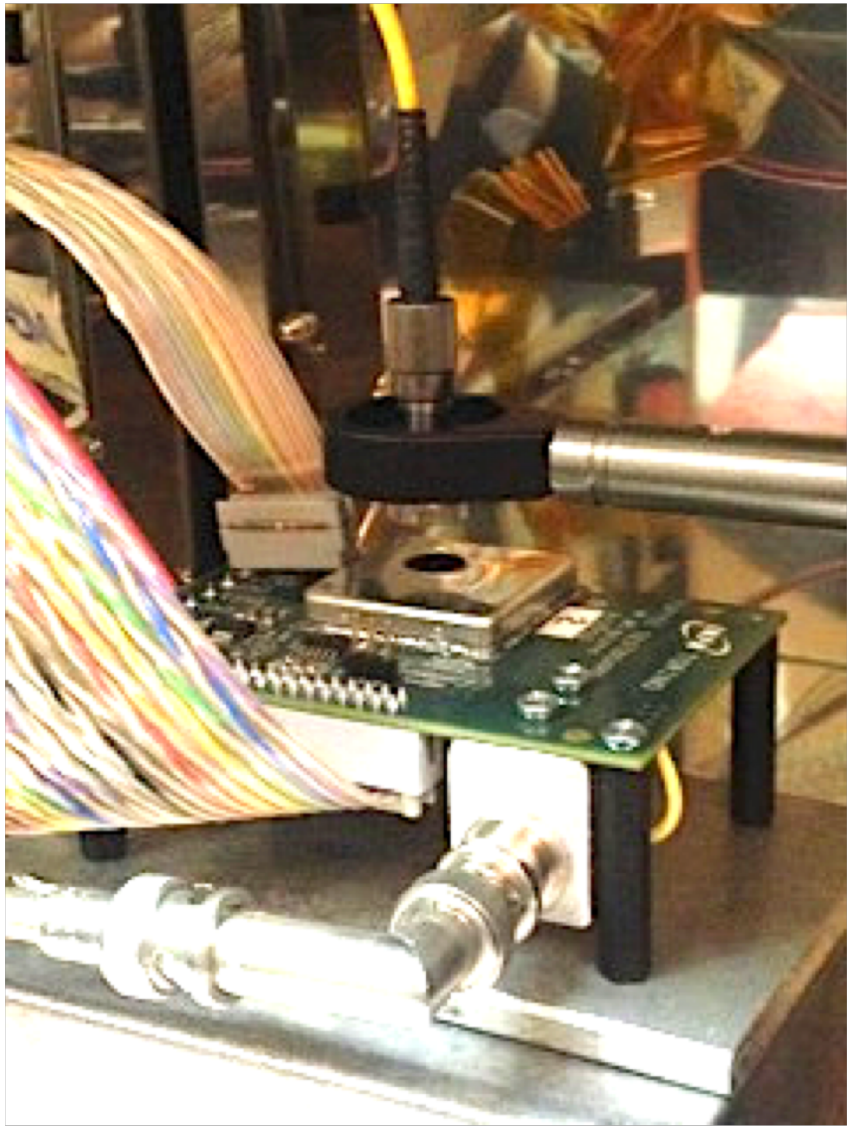
Front-end gain comparison



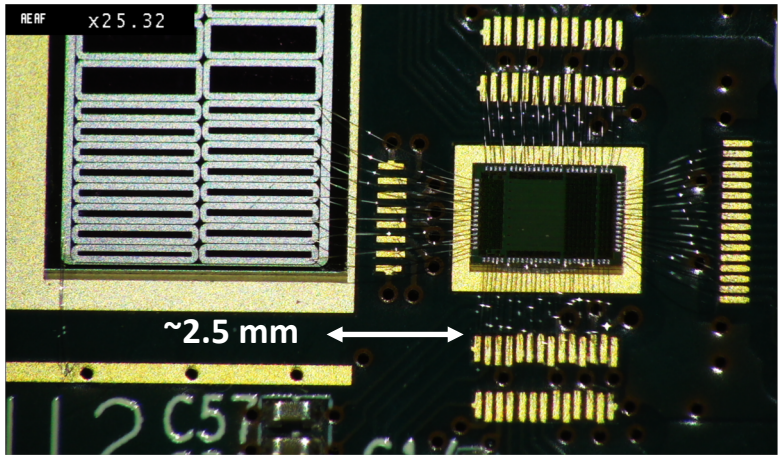


ASIC for UFSD sensors: TOFFEE



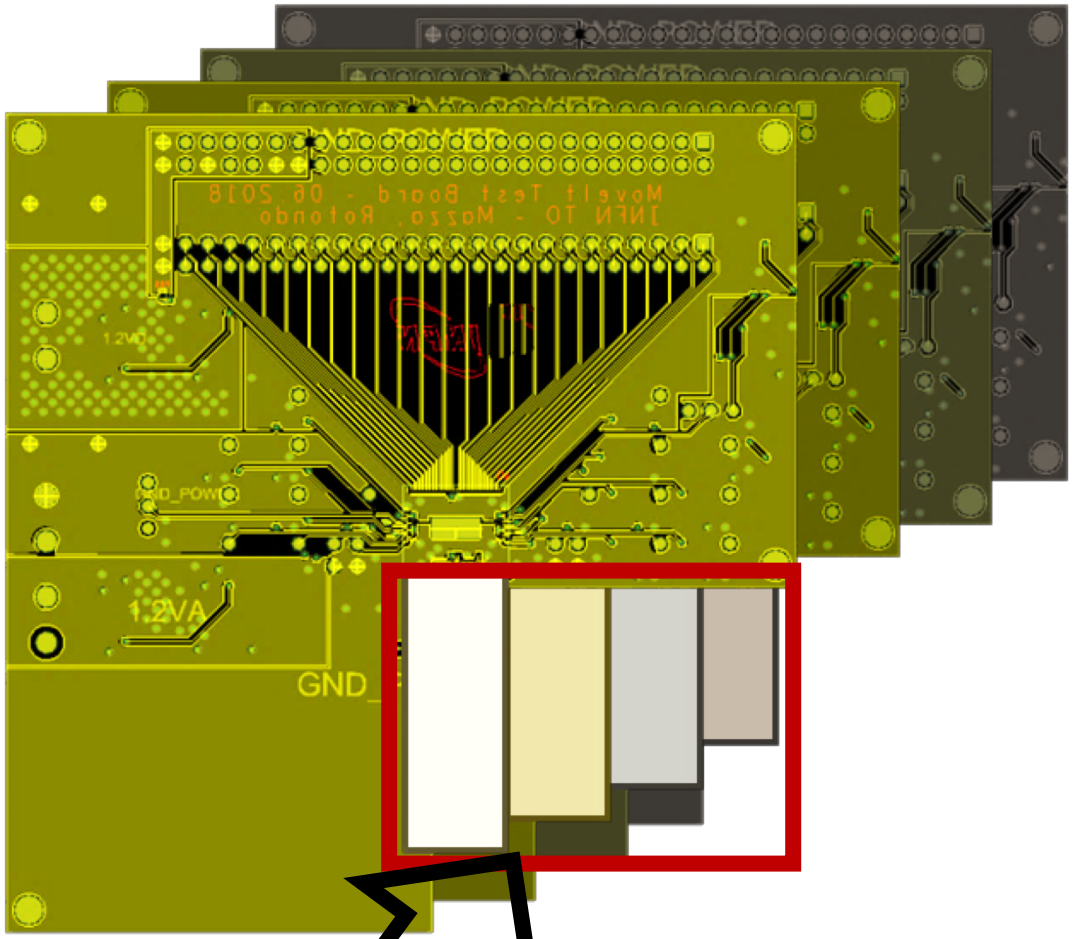


- Direct connection between CT-PPS module and the ASIC
- Climatic charmber used to reduce external interference
- Sensors depleted with ~200 V



ASIC for UFSD sensors: ABACUS

Active area extension:



Particle beam

Some examples from test beams

- **CMS HGCAL:**

  PIN diode thickness 300 μm A=25 mm2

  Cd = 8 pF en = 1 nV/√Hz td = 3 ns σ = 420 ps/Q(fC)

  1 MIP = 3.8 fC => σ = 110 ps/#MIP

  ~200 ps measured

- **ATLAS HGTD:**

  LGAD diode thickness 50 μm A= 2 mm2 G = 10

  Cd = 2 pF en = 2 nV/√Hz td = 0.5 ns σ = 50 ps/Q(fC)

  1 MIP = 5 fC (G=10) => σ = 10 ps/#MIP

  ~40 ps measured

- **NA62 tracker:**

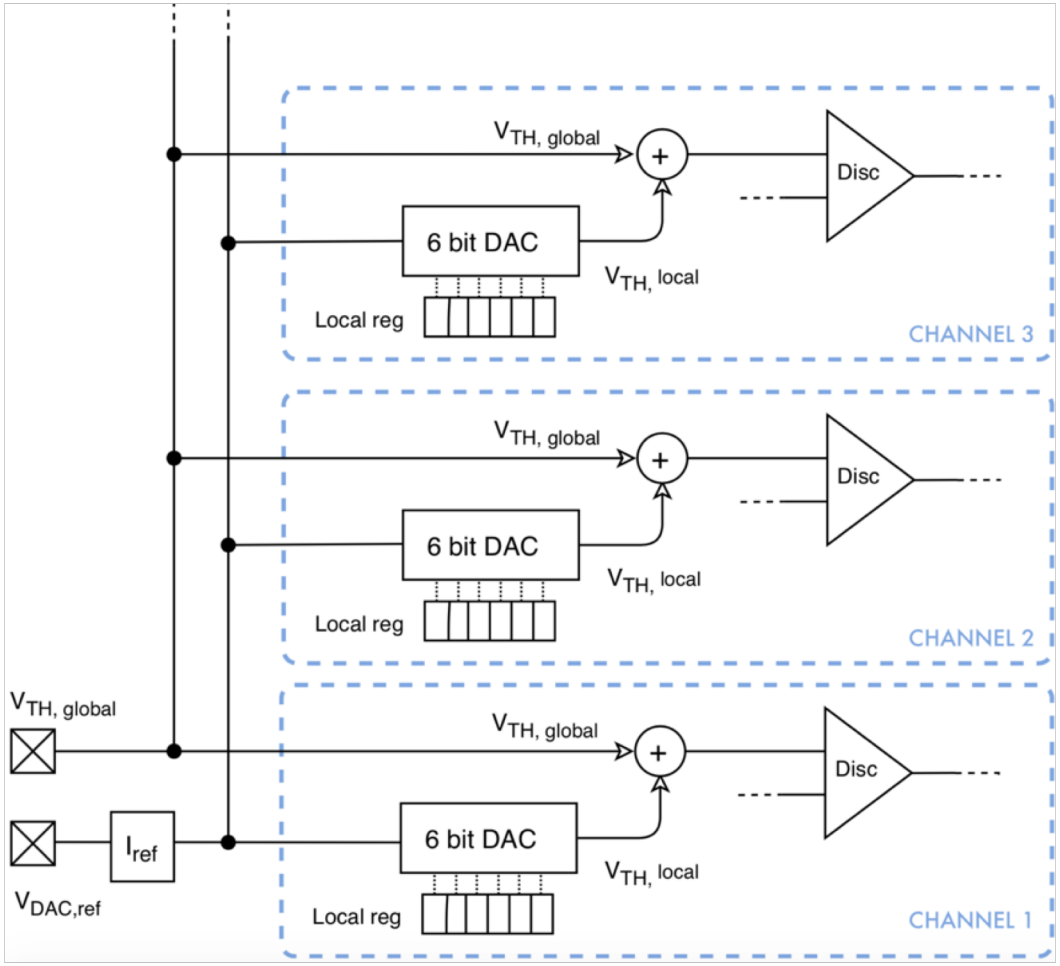
  PIN diode thickness 300 μm, A=0.09 mm2

  Cd = 0.1 pF en = 11 nV/√Hz td = 3 ns σ = 60 ps/Q(fC)

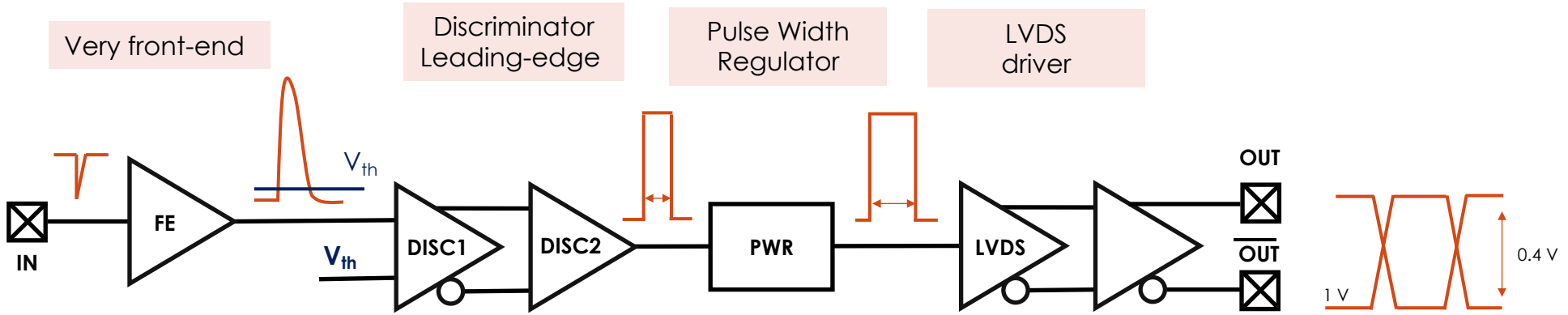
  1 MIP = 3 fC => σ = 20 ps/#MIP

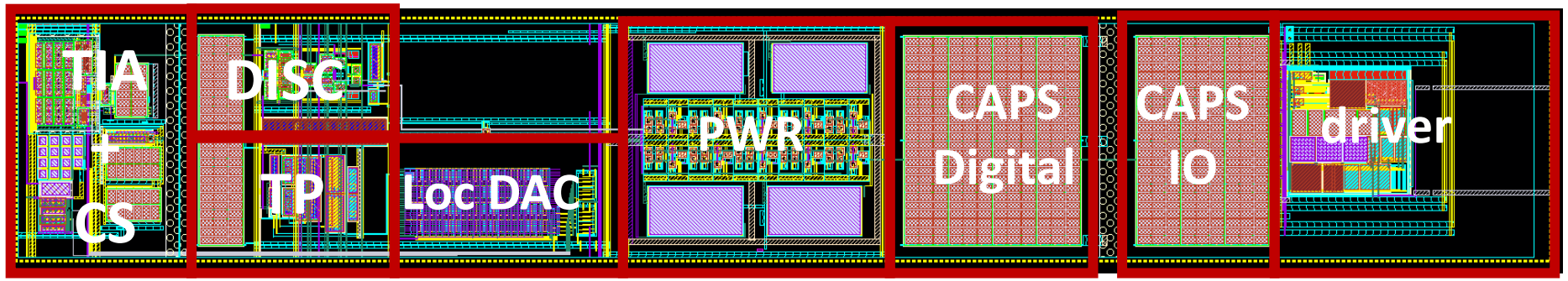
  ~60 ps measured

Threshold voltage generation

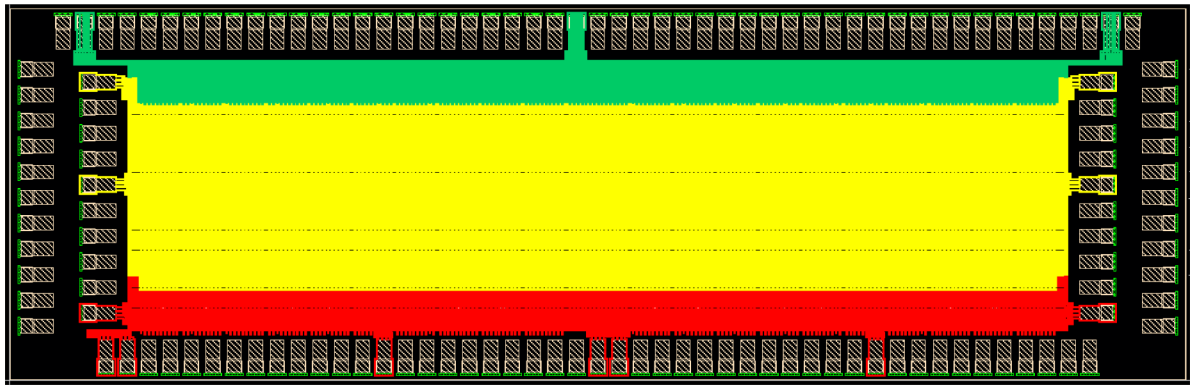


The channel of FAST

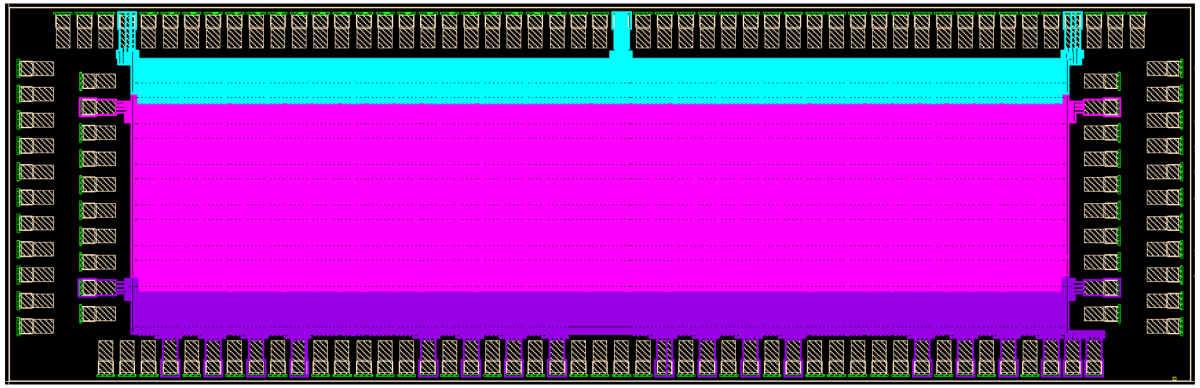




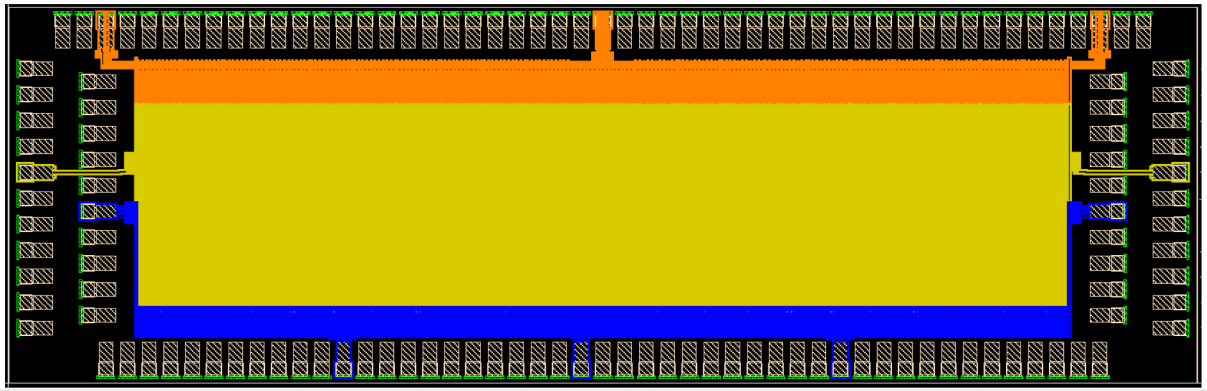
Power distribution: vdd, gnd, sub



VDD
2 (+6) + 4 + 3



GND
2 (+ 18) + 2 + 3



SUB
2 (+3) + 2 + 3