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FAST: a front-end readout ASIC for picosecond time resolution applications with UFSD

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Measurements of Time of Arrival of particles in detectors with picosecond time accuracy is becoming fundamental for several applications worldwide. The future upgrade of High Luminosity LHC (HL-LHC) is one example where these measurements will be exploited to mitigate the pile-up effects generated by the increase of luminosity. Thanks to this tool, events overlapped in space but separated in time will be distinguished increasing the overall detector efficiency. Dedicated timing layers for performing picosecond measurements are under construction. Examples are the MIP Timing Detector in the CMS experiment and the High Granularity Timing Detector in the case of the ATLAS experiment. In parallel, several R&D projects started worldwide to fabricate dedicated sensors and electronics to grow the technology required to build these new detectors.
This level of accuracy requires specific sensors able to provide signals with large amplitudes and short duration. Ultra Fast Silicon Detectors are an example of optimized silicon devices suitable to reach 30 ps time resolution. Concerning the electronics coupled to sensors, very strict requirements (like power consumption) make it difficult reaching this kind of resolutions. Also having large sensors in the order of 6 pF or greater represents an additional complexity to deal with.

In this work we present FAST, a low power multichannel ASIC developed for high precision timing measurements with UFSD sensors. The target of FAST is reducing the jitter contribution to the time resolution below 30 ps with 6 pF sensor capacitance. The channel architecture consists of a Trans-Impedance Amplifier (TIA), a second amplification stage based on a common source amplifier, a two stages leading edge discriminator, a Pulse Width Regulator to tune the digital output duration and a LVDS driver. The most critical part is the trans-impedance amplifier. The power consumption of this block is 1.2 mW. Three flavors of FAST have been developed to explore more front-end architectures. According to the post-layout simulations, the flavors of FAST exhibit a time resolution below 30˜ps when coupled to sensors with capacitance up to 10 pF. First measurements with one flavor show a jitter of 25 ps of the typical signal generated by UFSD (8 fC). These preliminary data show a 14 ps jitter saturation starting from 30 fC injected charges.

The ASIC has been produced in September 2019 and several tests are ongoing. Simulation and characterization results showing the timing performance of the prototype will be presented at the conference.

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