THE MONOPIX DETECTORS - CMOS PIXEL DETECTORS WITH LARGE AND SMALL ELECTRODES

NORBERT WERMES (UNIVERSITY OF BONN)
OUTLINE

- Setting the stage
- The Monopix developments at UBonn (in coll. w/ CERN, CPPM, IRFU)
- Results on LF-Monopix1 and TJ-Monopix1
- The Monopix2’s
- 2024 - 27++: Phase 2 ATLAS/CMS completely replace their trackers to face the very fierce environment

- ATLAS:
  ~ 165 m² silicon strips
  ~ 12 m² silicon pixels (currently 2m²)

- CMS:
  ~ 220 m² silicon strips
  ~ 5-6 m² silicon pixels (currently 2m²)
FIERCE ENVIRONMENT AT THE HL-LHC (PP)

Solution: pixels as much as possible / affordable / buildable in time

Dominating objectives to meet:
Radiation levels, hit rates and 25 ns bunch structure

Strip layers
- NIEL ≈ 10^{14} \text{n}_{\text{eq}}/\text{cm}^2
- TID ≈ 10\text{Mrad}
- rate ≈ 30 \text{MHz} / \text{cm}^2
- Large area O(100\text{m}^2)

Outer pixel layers
- NIEL ≈ 10^{15} \text{n}_{\text{eq}}/\text{cm}^2
- TID ≈ 100 \text{Mrad}
- rate ≈ 300 \text{MHz} / \text{cm}^2
- Larger area O(10\text{m}^2)

Inner layers
- NIEL ≈ up to 2\times10^{16} \text{n}_{\text{eq}}/\text{cm}^2
- TID ≈ 1 \text{Grad}
- rate ≈ 3-4 \text{GHz} / \text{cm}^2
- Smaller area O(1\text{m}^2)

Trento WS, Vienna, 18.02.2020, N.Wermes
### Hybrid Pixel Detectors

#### MONOLITHIC PIXEL DETECTORS

**ARE THE FUTURE!**
- for particle physics
- also high energy pp
- for pCT
- for imaging appl.
- other ...

<table>
<thead>
<tr>
<th>RHIC STAR</th>
<th>ALICE-LHC</th>
<th>ILC / CLIC</th>
<th>HL-LHC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Req. time resolution [ns]</td>
<td>110</td>
<td>20 000</td>
<td>350 / 156</td>
</tr>
<tr>
<td>Particle Rate [MHz / cm$^2$]</td>
<td>0.4</td>
<td>&lt; 10</td>
<td>&lt; 3</td>
</tr>
<tr>
<td>Fluence [n$_{eq}$/ cm$^2$]</td>
<td>&gt; $10^{12}$</td>
<td>&gt; $10^{13}$</td>
<td>&lt; $10^{12}$</td>
</tr>
<tr>
<td>Ion. Dose [MRad]</td>
<td>0.2</td>
<td>&lt; 3</td>
<td>&lt; 1</td>
</tr>
</tbody>
</table>

**Outer**
- 25
- 100-200
- $10^{15}$
- 80

**Inner**
- 25
- 2000
- $2 \times 10^{16}$
- > 1000

**MAPS (e.g. ALPIDE)**

**Hybrid pixels -> DMAPS rejected**

**HL-LHC devm’t:** radhard (TID & NIEL) + fast response time + fast readout => Q coll. by drift & full R/O arch.

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Malta ARE THE FUTURE ! § for particle physics § also high energy pp § for pCT § for imaging appl. § other ...

Page dimensions: 726.0x408.0

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INTRODUCING DMAPS

Hybrid detector

Depleted monolithic active pixel sensor (CMOS)

No need for fine pitch bump bonding between sensor and readout circuitry.

1. **Easier to produce and easier to test (one detector entity)**
2. **Large cost reduction: sensor + R/O chip + BB → one chip**
3. **Plus all the advantages that large CMOS Fabs may offer, including fast turn around, large wafer sizes, large throughput**
Electronics **inside** charge collection well

- **large** collection electrode
  - => little low field regions
  - => on average **short(er) drift** paths
  - => less trapping -> **radiation hard**

- **Larger** sensor **capacitance** (pw & dnw!)
  - => noise & speed/power penalty
  - => possible x-talk (digital to sensor)

Electronics **outside** charge collection well

- **small** electrode
  - => **very small sensor capacitance** (< 5fF)
  - => lower analog power budget (noise, speed)
  - => less prone to x-talk

- on average **long(er) drift distances** and potentially low field regions
  - -> **radiation hardness needs process mods**
**E.G. PROCESS MODIFICATION – TOWERJAZZ 180 NM CMOS**

**Standard process**

- **ALICE ITS type**
- **High res. p-type epi.** (> 1 kΩ·cm)
  
  => thickness typ. **25 µm**

- Quadruple-well
  
  => deep pwell shields nwell => **full CMOS**

- **Reverse bias** typ. -6V
  
  => enhanced (but not yet full) depletion

  => some charge collected by diffusion only => slow

**Modified process**

- Additional planar medium dose **N implant**
  
  => depletion from **two junction** boundaries

  full volume can be depleted

  better charge collection in lateral direction

- **Maintain small capacitance**

- **No significant circuit/layout changes**

  W. Snoeys et al. DOI: 10.1016/j.nima.2017.07.046
LARGE WORLDWIDE INTEREST IN DEPLETED CMOS PIXELS

... and more

LF  TJ
Bonn  CEA/IRFU  CERN  CPPM
large electrode   small electrode
THE TWO DEVELOPMENT LINES

CCPD_LF
- Subm. Sep. 2014
- Fast R/O coupled to FE-I4

LF-CPIX (DEMO)
- Fast R/O coupled to FE-I4

LF-Monopix1
- Fast column drain R/O

LF-Monopix2
- Subm. April 2020
- 50 x 150 µm² pixels
- Full height matrix
- Fast column drain R/O

ALICE ALPIDE

INVESTIGATOR
- 2016
- 8 x 8 pixel submatrices

MALTA
- 36.5 x 36.5 µm²

MALTA (asynchronous) & TJ-Monopix1 (column drain)
- subm. 2018
- large matrices
- fast asynchr & col. drain R/O

miniMALTA
- subm. 2018
- measures for rad. hardness

TJ-Monopix2
- 33 x 33 µm² pixels
- Full height matrix
- Fast column drain R/O

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Different electrode (large/small) approaches lead to different
**ANALOG FRONT-ENDS - CSA VS. VOLTAGE AMPLIFIER**

- large electrode

**Charge Sensitive Amplifier**

- Choice for large electrode design
  - Gain (ideally) independent of $C_D$
    - $G \sim 1/C_f$ (typ. $C_f \sim 5\, \text{fF}$)
  - $\tau_{CSA} \propto \frac{C_D}{g_m C_f}$, $ENC^2_{\text{therm}} \propto \frac{kT C_D^2}{g_m \tau}$
    - requires larger $g_m$ (power) for large $C_D$
    - typ. power $30 – 40\, \mu\text{W}$ per pixel

- Threshold trimming is advised and is a standard in typical implementations
• small electrode

Voltage amplifier (ALPIDE like)
- => Profit from small sensor capacitance
  => large voltage signal $Q/C_D$ @ input node
- Very compact design
  => amplification + shaping in one stage
  => simple inverter as discriminator
  => no threshold trimming used (see later)
- Optimized power for required timing
  => $\sim 1 \mu W$/pixel for 25 ns peaking time

$$\frac{S}{N} \propto \frac{Q}{C_D} \sqrt{g_m} \propto \frac{Q}{C_D} \sqrt{P}, \quad P \propto \left(\frac{C_D}{Q}\right)^m$$

$2 \leq m \leq 4$
DMAPS
READOUT ARCHITECTURE CHOICES

- Small pixels
- High logic (memory) density
- Fast shaping
- High data transmission bandwidth
WE CHOSE A “COLUMN DRAIN” ARCHITECTURE

**Synchronous readout => time stamping in matrix**

- BC ID (40 MHz) distributed in the column
- Hit timing stamped in pixel
  - LE: leading edge
  - TE: trailing edge
  => Time of arrival: LE
  => Ana. info. from ToT
- Hits read out sequentially, following a token passing scheme on a shared column bus

- Well established scheme in ATLAS – FE-I3 like (current pixel detector)
- Demonstrated rate capability for the addressed goal (ITk outer pixel layers)
- Affordable in-pixel logic (storage & digital R/O)
- Challenges: preventing digital cross talk, pixel size, C_D (for large electrode design)
WE CHOSE A “COLUMN DRAIN” ARCHITECTURE

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- Hits read out sequentially, following a token passing scheme on a shared column bus

shown to be suitable for ITk OL rates

100 MHz/cm²
ALTERNATIVE: ASYNCHRONOUS READOUT SCHEMES

DMAPS with asynchronous matrix => time stamping at periphery
=> Hits transferred to periphery immediately => calls for massive parallelism

A) One to one connection

B) Shared bus by pixel groups

- Two high speed buses w/ short pulses (~1ns)
- Complicated balancing for multibit data to arrive simultaneously at bottom
- GHz synchronization needed

• Challenge: avoid data collisions

o(400) lines in two metal layers; larger periphery
THE “MONOPIX1” CHIPS

- Two large scale DMAPS chips were developed targeting data rates and radiation levels expected at ATLAS ITk outer layers
  - Following both, large and small electrode sensor designs employing two CMOS technologies
  - and using the “column drain” architecture for the R/O matrix

- Simplified “downstream” data processing, e.g. no data buffering & triggering, no Gbps-link

![Diagram of Monopix1](image)

**LF-Monopix1**
50 × 250 μm² pixels

**TJ-Monopix1**
36 × 40 μm² pixels
RESULTS ON LFOUNDRY 150 NM DESIGNS

- **CCPD_LF**
  - Pixel size: 33 μm × 125 μm
  - Chip size: 5 mm × 5 mm
  - Fast R/O with FE-I4
  - Thickness: 750/300/100 μm
  - Design by Bonn/CPPM/KIT

- **LF-CPIX**
  - Pixel size: 50 μm × 250 μm
  - Chip size: 10 mm × 10 mm
  - Fast R/O with FE-I4
  - Thickness: 750/200/100 μm
  - Design by Bonn/CPPM/IRFU

- **LF_Monopix1**
  - Pixel size: 50 μm × 250 μm
  - Chip size: 10 mm × 10 mm
  - Integrated column drain R/O
  - Thickness: 750/200/100 μm
  - Design by Bonn/CPPM/IRFU
LFOUNDRY 150 NM
LARGE ELECTRODE (55% FF)

LFA150:
• LFoundry 150 nm process (deep N-well/P-well)
• Quadrupel well
• 7 metal layers
• Resistivity > 2 kΩ·cm
• Backside processing
• Voltages > 350 V
- Pixel size 50 µm × 250 µm
  - ~ 55% = coll. electrode/pixel area
  - “rounded” corner to minimize field

- Careful layout / precautions required to prevent cross talk from circuit layer to sensing electrode through psub/dnw capacitance
  1. Separated analog/digital power domains
  2. Digital “bulk” (in a separate pwell) is separated from digital ground
  3. Full custom in-pixel digital design, optimising transient signal switching
• Good radiation hardness of large electrode sensor proven in various prototypes

LFoundry 150 nm CMOS
P-substrate > 2 kΩ·cm
Bias 100 - 400 V
7 metal layers

T. Hirono et al., DOI: 10.1016/j.nima.2016.01.088
P. Rymaszewski et al., DOI: 10.1088/1748-0221/11/02/C02045

Passive sensor

I. Mandić, et al.,
DOI: 10.1016/j.nima.2018.06.062

see talk by
D.-L Pohl

LFoundry sensor structure
200µm fully depleted

2 × 10^{15} \text{n}_{\text{eq}}/\text{cm}^2

1.14 × 10^{15} \text{n}_{\text{eq}}/\text{cm}^2

~100%
IRRADIATED ACTIVE SENSORS OF LF_MONOPIX1

- Guard ring structure essential for high breakdown voltage (up to 300 V)
- Full depletion voltage @ 100 µm: unirr. $V_{dep} = 7$ V, irradiated $V_{dep} = 130$ V
**TID PERFORMANCE (100 MRAD)**

- LF-CPIX X-ray irradiated to **100 Mrad**
  - Irradiated and measured at room temperature
  - Tunable thresholds with **almost unchanged dispersion**
  - **Gain degradation <5%**
  - **Noise increase ~25%**

(probably largely due to $i_{\text{leak}}$ increase after irrad.)

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**Threshold dispersion (LF-CPIX)**

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**Normalized gain and ENC (LF-Monopix1)**

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T. Hirono, et. al, DOI: 10.1016/j.nima.2018.10.059
**LF-MONOPIX1: IN-PIXEL DIGITAL LOGIC**

- **Preamp + Discriminator**
- **R/O Logic**

**Outputs of all CSAs**

**Output of one CSA**

- **8-bit time stamp & ToT @ 40 MHz** (gray encoded)
- **Full-custom digital circuit**
• **High and uniform efficiency also after irradiation**

- Noise occ. < 1.2 Hz/pix  
  < 10^{-7}/25 ns/pixel
- 1% masked pixels
- Dry ice cooling
- Bias -200 V
- Thres \( \sim \)1800 e-
- \( \varepsilon = 99.7 \pm 0.1 \) %

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**Before irrad.**

![Image](before_irrad.png)

**After \( 10^{15}n_{eq}/cm^2 \) (neutrons)**

![Image](after_irrad.png)

- Noise occ. < 0.1 Hz/pix  
  < 10^{-8}/25 ns/pixel
- 0.2% masked pixels
- Dry ice cooling
- Bias -130 V (this sensor!)
- Thres \( \sim \)1700 e-
- \( \varepsilon = 98.9 \pm 0.1 \) %

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M. Barbero et al., arXiv:1911.01119, submitted to JINST

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RESULTS ON TOWER JAZZ 180 NM DESIGNS

TowerJazz 180 nm CMOS CIS
- Deep pwell allows full CMOS in pixel
- 6 metal layers
- High res. epi-layer: $1-8 \, \text{k} \Omega \cdot \text{cm}$
  => epi thickness: $18 - 40 \, \mu\text{m}$
- Modified process to improve lateral depletion

Derived from ALICE development (led by CERN)
TJ – MALTA AND TJ - MONOPIX

Small electrode designs

- Sensor design is identical
- Front ends similar (different biasing schemes)
- R/O architectures very different

MALTA
asynchronous R/O
no clock distrib.
targeting low power

MONOPIX1
column drain architecture

“MALTA” Full ATLAS size

TJ MonoPix
TJ-MONOPIX1: PIXEL LAYOUT

- Pixel size $36 \times 40 \, \mu m^2$
- $2 \, \mu m$ collection diode + $3 \, \mu m$ spacing
- Separated digital & analog region, several
- Full-custom digital design
  - 6 bit ToA & ToT
  - Minimized area for small pixel size

Four equal sectors with different pixel/periphery designs
$(4 \times 224 \times 112$ pixels)
Good noise performance 10 - 15 e⁻
-> Increased by ~10 e⁻ after $10^{15}$ $n_{eq}/cm^2$

- Thres. dispersion 30 - 40 e⁻
  -> 50 - 65 e⁻ after $10^{15}$ $n_{eq}/cm^2$

Better noise & threshold tuning needed!

Long tail likely due to RTS noise in

I. Caicedo et al., DOI: 10.1088/1748-0221/14/06/C06006
CHARGE COLLECTION WITH SMALL ELECTRODES

- epi thickness 20-30 µm
- Field strength and shape under DPW in pixel corners is critical
  - Full depletion under the DPW and ...
  - ... operation at low threshold is essential
  - Transverse field components in corners essential for radiation hardness

Irradiated $10^{15}$n/cm$^2$ @ 350e- threshold
2x2 pixel at 36 µm pitch
OPTIMATIONS FOR RADIATION HARDNESS

1. Structuring underneath dpw

2. Lower thresholds and noise -> mods to analog electronics

3. high resistivity substrate (pCz ... next slide)

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MiniMALTA test chip
36x36µm²
after $10^{15}$ n_{eq}/cm²

measures 1 plus 2

M. Dyndal et al., 2020_JINST_15_P02005

M. Munker 10.1088/1748-0221/14/05/C05013
n-irradiated (IJS) to $2\times 10^{15}$ $n_{eq}/cm^2$ followed by DESY beam test
Full-size MALTA sensor with original front-end design on HR pCz (i.e. only measure no. 3)
FROM MONOPIX1
TO MONOPIX2
GOALS LF-MONOPIX2

- Smaller cell size -> 50 × 150 µm²
- Reduce detector capacitance from 400 fF -> 250 – 300 fF
- Optimise digital design for minimum dig./ana. coupling
- New amplifier design for faster timing
- Keep conservative and safe design (e.g. wide power metals, guard rings) to ensure high breakdown tolerance

- 340 × 56 pixels
- 50 × 150 µm²
# LFOUNDRY MONOPIX2 (LARGE ELECTRODE DESIGN)

<table>
<thead>
<tr>
<th></th>
<th>LF-Monopix1</th>
<th>LF-Monopix2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel size</td>
<td>50 × 250 µm²</td>
<td>50 × 150 µm²</td>
</tr>
<tr>
<td>C(d)</td>
<td>~ 400 fF</td>
<td>250 – 300 fF</td>
</tr>
<tr>
<td>Analog power/pixel (CSA + Discr.)</td>
<td>15 µA + 5 µA = 20 µA</td>
<td>10 µA + 2 µA = 12 µA</td>
</tr>
<tr>
<td>Noise</td>
<td>~150 e⁻ - 200 e⁻</td>
<td>100 ~150 e⁻</td>
</tr>
<tr>
<td>LE/TE time stamp</td>
<td>8-bit</td>
<td>6-bit</td>
</tr>
<tr>
<td>ToT @ 6 ke⁻</td>
<td>---</td>
<td>200 – 250 ns</td>
</tr>
<tr>
<td>Max. ToT</td>
<td>---</td>
<td>400 ns</td>
</tr>
<tr>
<td>(rms) thres. dispersion</td>
<td>(~ 100 e⁻)</td>
<td>(80 e⁻)</td>
</tr>
<tr>
<td>Min. threshold</td>
<td>1500 e⁻</td>
<td>1000 e⁻</td>
</tr>
<tr>
<td>In-time threshold</td>
<td>~ 2000 e⁻</td>
<td>1500 e⁻</td>
</tr>
</tbody>
</table>

Tape out: April 2020

- 340 × 56 pixels
- 50 × 150 µm²
GOALS TJ-MONOPIX2

Large 2x2 cm² sensor featuring

- Larger signal
  - high resistivity pCz material

- More efficient charge collection
  - modified sensor geometry (n-gap, extra dpw)
  - optimum (smaller) cell size for given electronics

- Lower noise and threshold operation
  - improved front end
    - gain increase
    - RTS noise reduced
    - less threshold dispersion
    - threshold trimming

- 512 × 512 pixels
- 33.04 × 33.04 µm²

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**TOWERJAZZ MONOPIX2 (SMALL ELECTRODE DESIGN)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>TJ-Monopix1</th>
<th>TJ-Monopix2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip Size</td>
<td>1x2 cm² (224x448 pix)</td>
<td>2x2 cm² (512x512 pix)</td>
</tr>
<tr>
<td>Pixel size</td>
<td>36 × 40 µm²</td>
<td>33.04 × 33.04 µm²</td>
</tr>
<tr>
<td>Noise</td>
<td>≅ 11 e⁻</td>
<td>&lt; 10 e⁻ (improved FE)</td>
</tr>
<tr>
<td>LE/TE time stamp</td>
<td>6-bit</td>
<td>7-bit</td>
</tr>
<tr>
<td>Threshold Dispersion</td>
<td>≅ 30 e⁻ rms</td>
<td>&lt; 20 e⁻ rms (improved FE + tuning)</td>
</tr>
<tr>
<td>Minimum threshold</td>
<td>≅ 300 e⁻</td>
<td>&lt; 150 e⁻</td>
</tr>
<tr>
<td>In-time threshold</td>
<td>≅ 400 e⁻</td>
<td>250 - 300 e⁻</td>
</tr>
<tr>
<td>Efficiency</td>
<td>≅ 70 % (irradiated)</td>
<td>&gt; 95% (irradiated)</td>
</tr>
</tbody>
</table>

Tape out: April 2020
CONCLUSIONS

- Development of DMAPS with full R/O needs time (and care)
- MONOPIX developments with large and small electrode can be considered as viable options for HL-LHC trackers
- Col-drain architecture meets Layer 4 rates with a (x10) margin
- **Large electrode**
  - high beak down voltage
  - large signal
  - high efficiency after $10^{15} \text{n}_{\text{eq}}/\text{cm}^2$
- **Small electrode**
  - low capacitance, low noise
  - low power, large Q/C
  - ways towards radiation hardness identified
- Stay tuned for large MONOPIX2 chips
Thanks to the DMAPS collaboration
