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The ATLAS ITk Strip Detector System for the Phase-II LHC Upgrade

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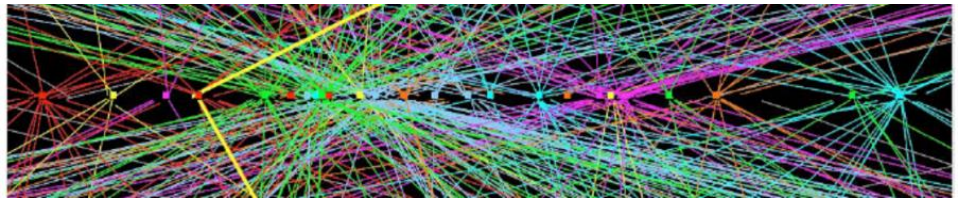
on behalf of the ATLAS ITk Strip Community

17th February 2020

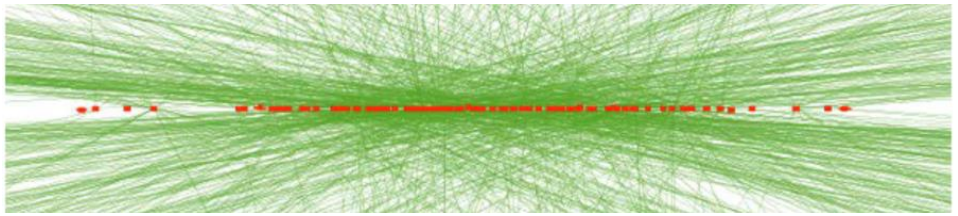
Introduction

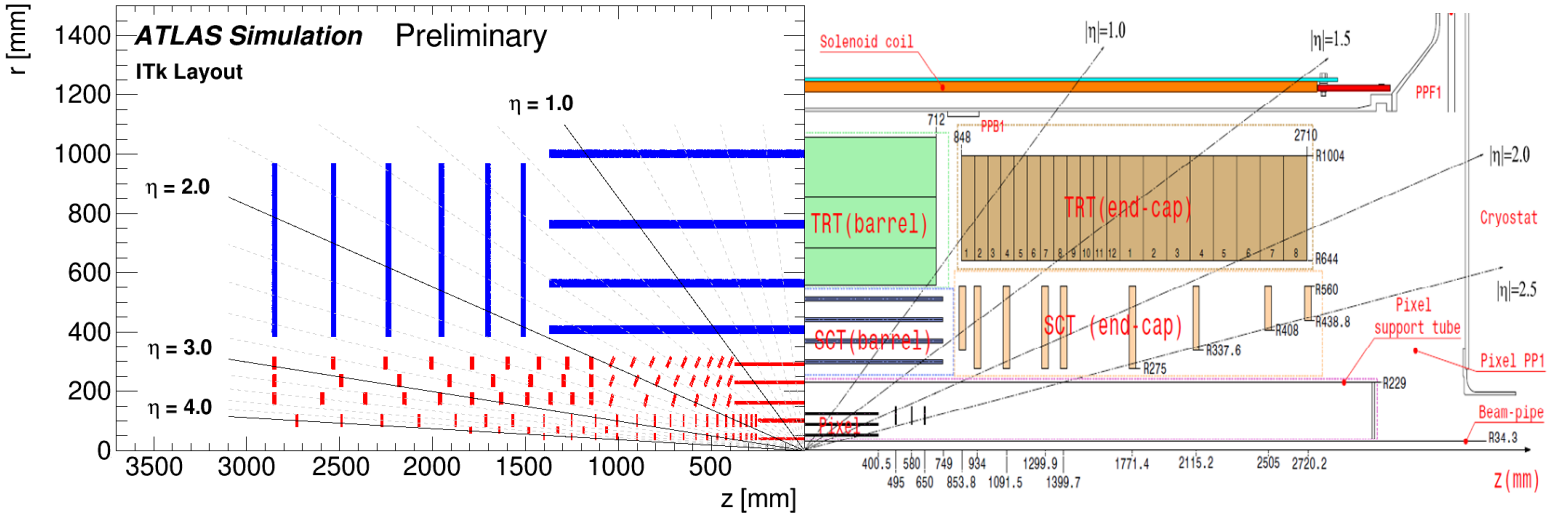
- All new silicon tracker to be installed in LS3
- Tracking coverage up to $|\eta|$=4.0
  - Hybrid pixel modules at inner radii
    - Not discussed here
  - Hybrid strip modules at outer radii
    - 1 x strip barrel:
      - 2 double sided layers of short (2.5cm) strips
      - 2 double sided layers of long (5.0cm) strips
    - 2 x strip end-caps:
      - 6 double sided discs of 1.8-6.0cm strips

LHC (25 vertices)



HL-LHC (200 vertices)





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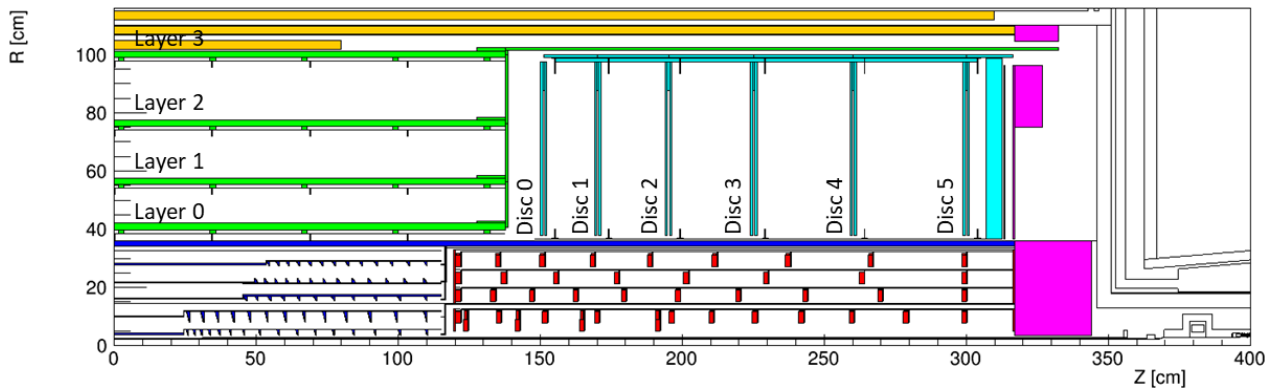
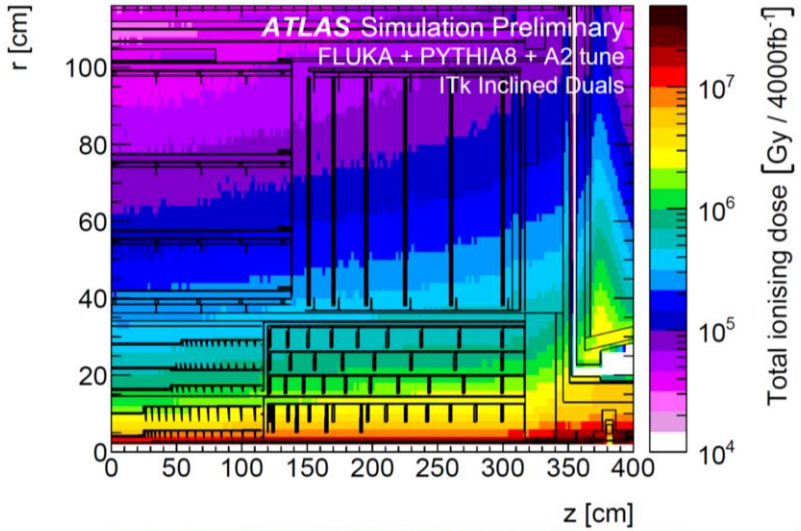
Radiation Tolerance

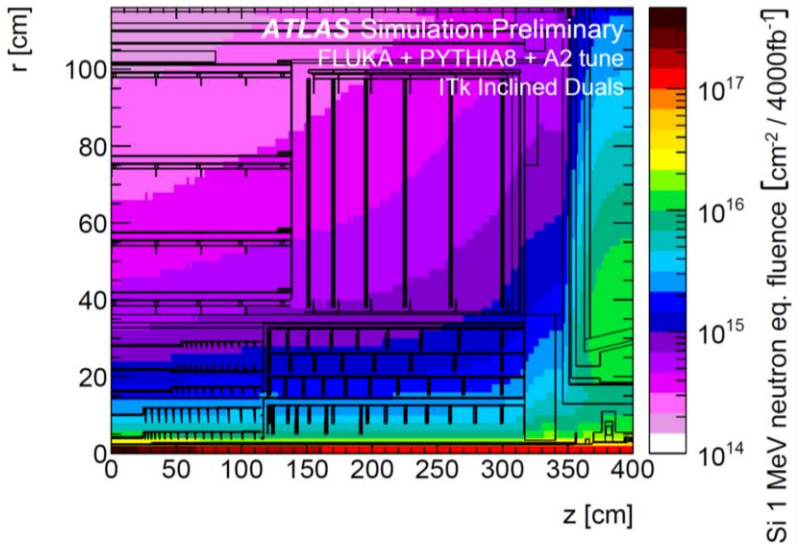


Position	1 MeV neq [10^{14} cm^{-2}]	Total Ionising Dose [MGy]
Layer 0	6.51	0.28
Layer 1	4.64	0.16
Layer 2	3.44	0.09
Layer 3	2.69	0.05
Disc 0	6.79	0.32
Disc 1	6.93	0.33
Disc 2	7.16	0.34
Disc 3	7.65	0.37
Disc 4	8.55	0.42
Disc 5	10.9	0.46

4000 fb^{-1}
No safety factors

Design to:
0.7 MGy
1.6x10^{15} neq
Safety factor of 1.5x





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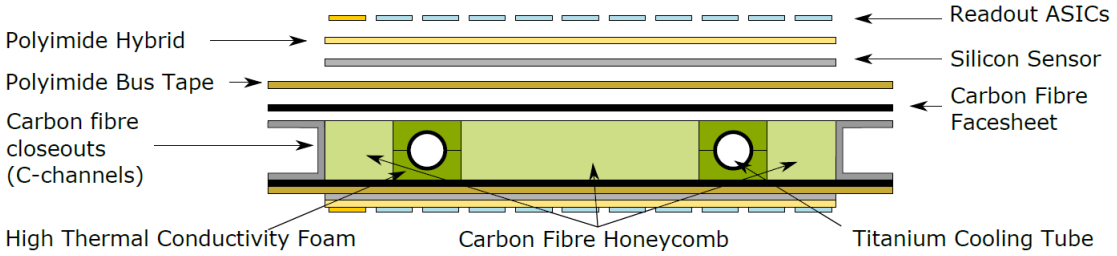
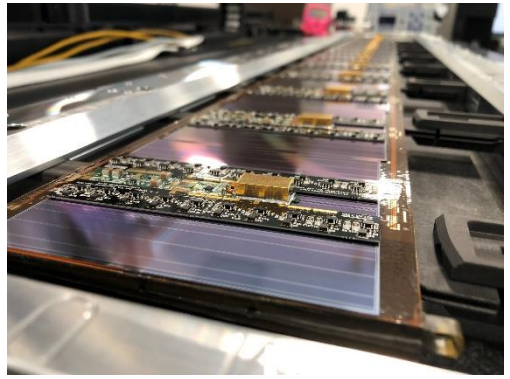
The local support concept

- Detector assembled from “medium” size local support objects
  - Staves in the barrel
  - Petals in the end-cap
- Each stave/petal is a standalone system-level object providing:
  - Mechanical support
  - Geometric location control
  - Cooling
  - Power (LV & HV)
    - 1 LV bus per side
    - 4 HV buses per side
  - Trigger, control, clock signals
  - Data readout
    - Electrical-to-optical conversion done by End-of-Substructure (EoS)
    - Electrical within local support
    - Optical outside local support
  - T, V, I monitoring





Numerology of ITk strips

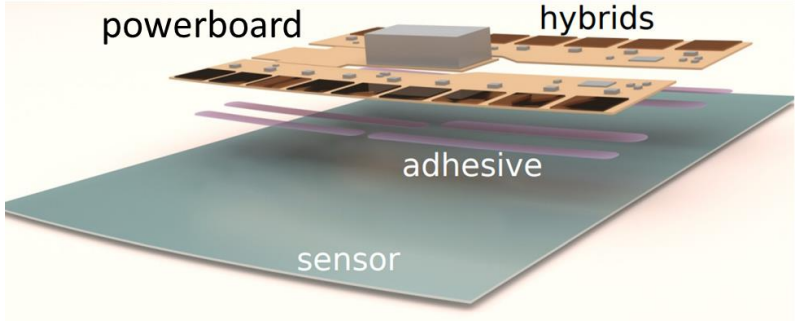
Barrel Layer:	Radius [mm]	# of staves	# of modules	# of hybrids	# of of ABCStar	# of channels	Area [m^2]
L0	405	28	784	1568	15680	4.01M	7.49
L1	562	40	1120	2240	22400	5.73M	10.7
L2	762	56	1568	1568	15680	4.01M	14.98
L3	1000	72	2016	2016	20160	5.16M	19.26
Total half barrel		196	5488	7392	73920	18.92M	52.43
Total barrel		392	10976	14784	147840	37.85M	104.86
End-cap Disk:	**z-pos. [mm]**	**# of petals**	**# of modules**	**# of hybrids**	**# of of ABCStar**	**# of channels**	**Area [m^2]**
D0	1512	32	576	832	6336	1.62M	5.03
D1	1702	32	576	832	6336	1.62M	5.03
D2	1952	32	576	832	6336	1.62M	5.03
D3	2252	32	576	832	6336	1.62M	5.03
D4	2602	32	576	832	6336	1.62M	5.03
D5	3000	32	576	832	6336	1.62M	5.03
Total one EC		192	3456	4992	43008	11.01M	30.2
Total ECs		384	6912	9984	86016	22.02M	60.4
Total		**776**	**17888**	**24768**	**233856**	**59.87M**	**165.25**

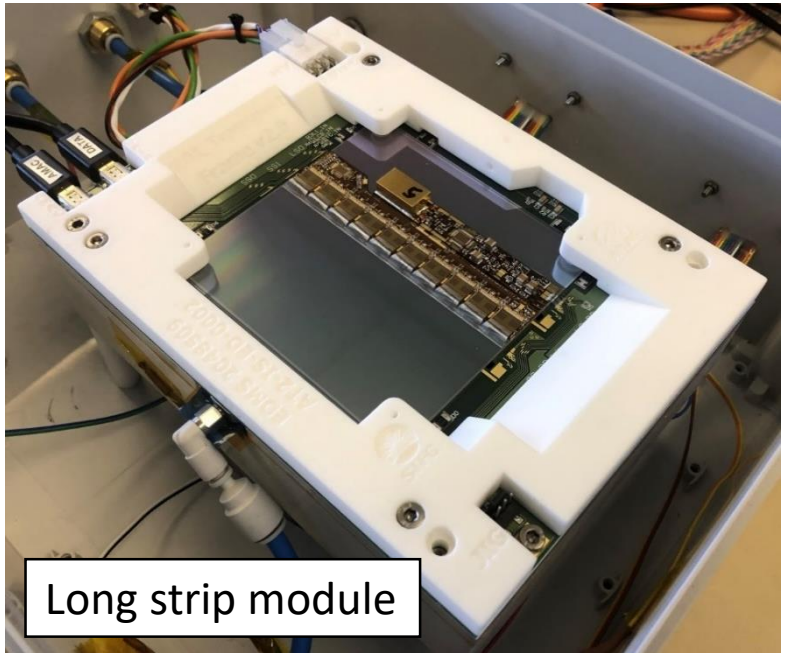
10 module assembly sites across US, UK & China

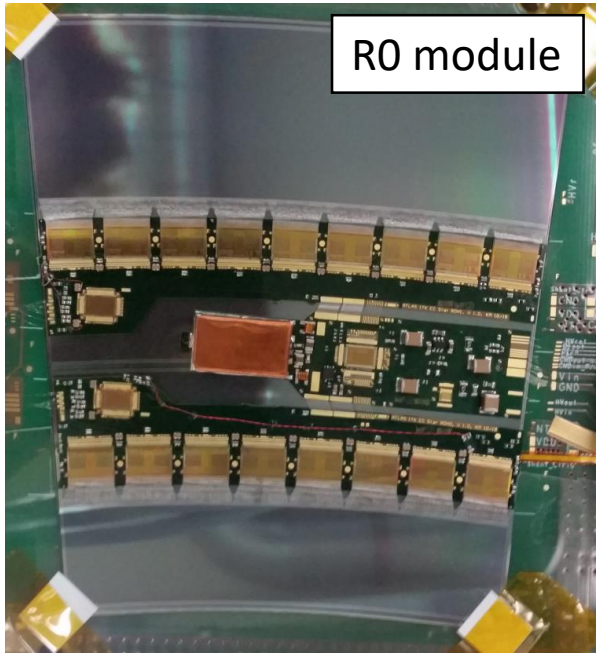
11 module assembly sites across Germany, Canada, Czechia, Spain, Scandanavia and Australia

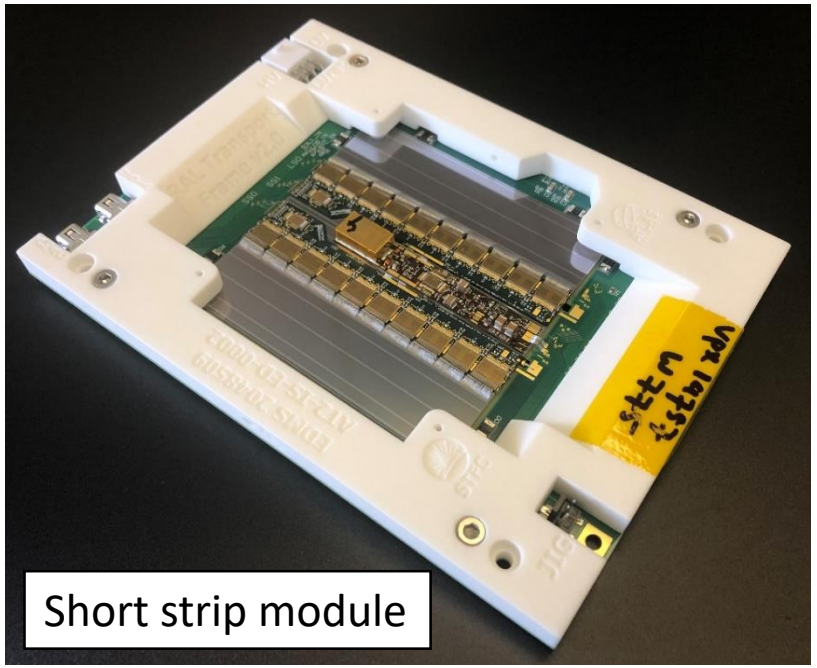
Strip modules

- Modules based around large area n-in-p strip sensors
  - see Bart Hommels' talk earlier today
- Hybrids and powerboards are glued directly to the sensor surface
- All interconnects performed using 25um aluminium wire-bonds
  - Low mass, high reliability, connectorless modules
- Modules glued and wire-bonded to stave/petals
- Current "Star" generation of chips (ABCStar, HCCStar, AMACv2) close to the final version

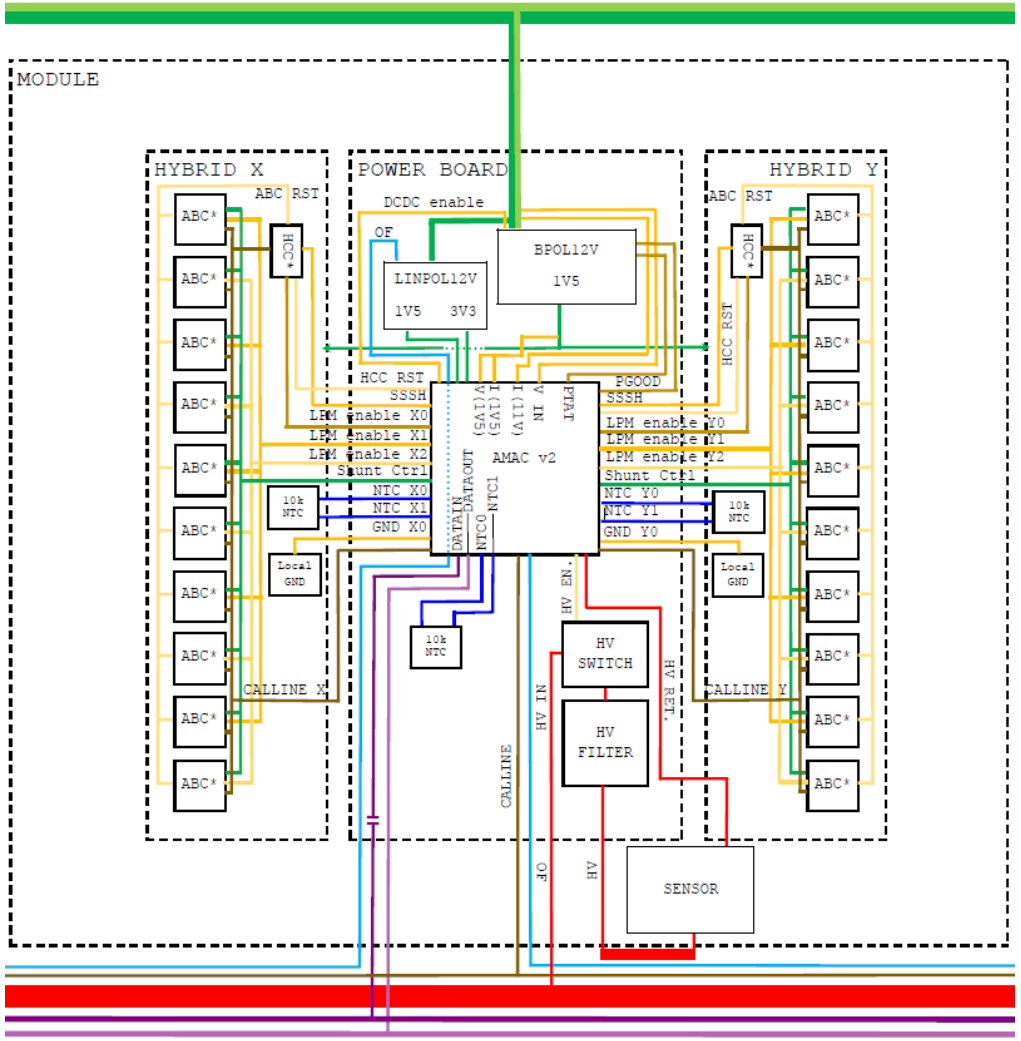








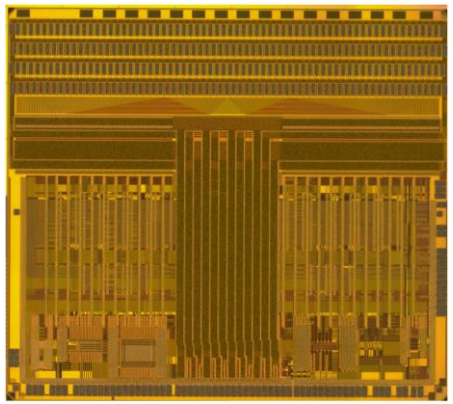
Strip module architecture

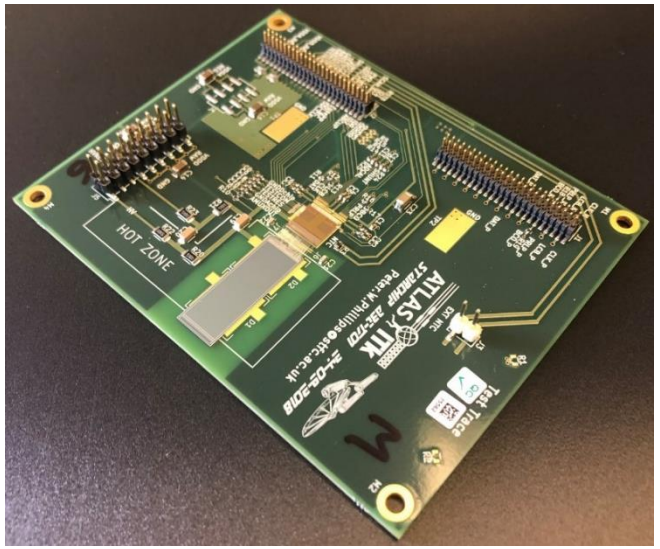


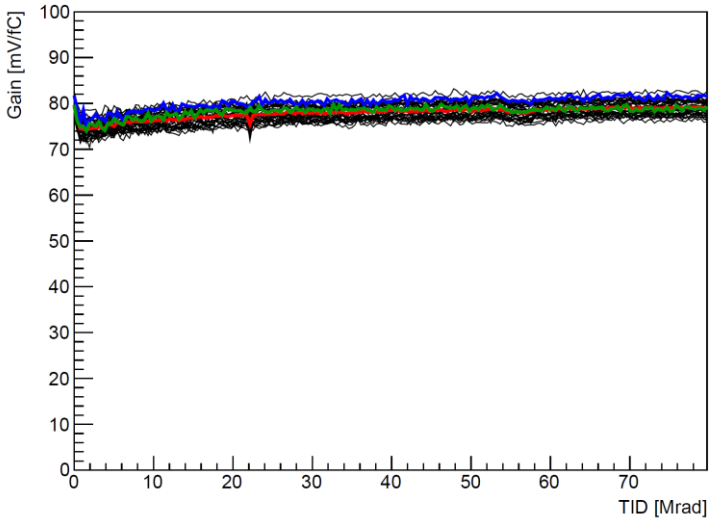
- Powerboard and Autonomous Monitor and Control ASIC (AMAC) are heart of the module
- Powerboard provides
  - LV power for AMAC via LinPoL12V linear regulator
  - LV power for module via BPoL12V DCDC converter
  - HV power for sensor via GanFET based HV switch
- AMAC
  - Measures T, V and I
  - Controls module through reset and enable lines
  - Can autonomously interlock based on readings
    - If used, foreseen as last line of defense

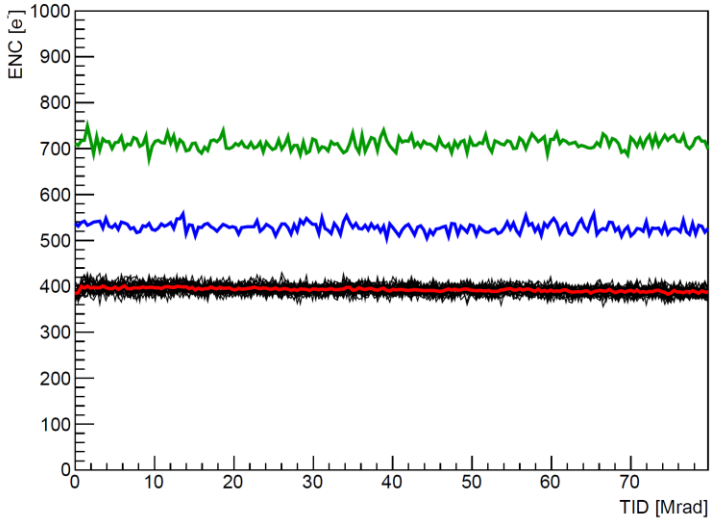
Front end performance

- Front end performance of ABCStar validated on (in order):
  - 32 channel analogue prototype chips
  - ***Full chips (256 channels) on single chip cards***
  - SS, LS and R0 modules
- Validated via noise/gain performance
  - Function of load capacitance
  - Function of TID using tungsten xray tube

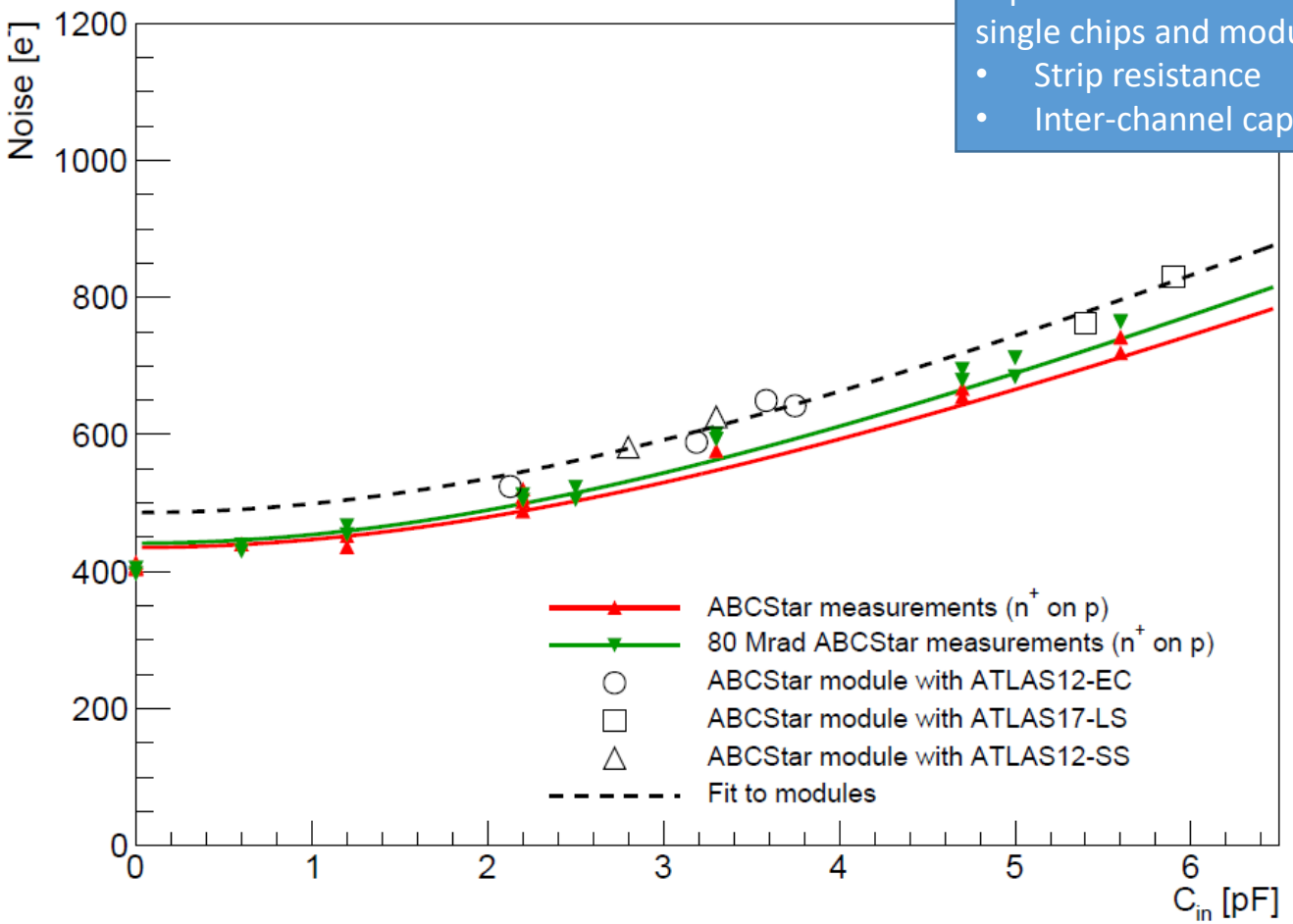








Front end performance

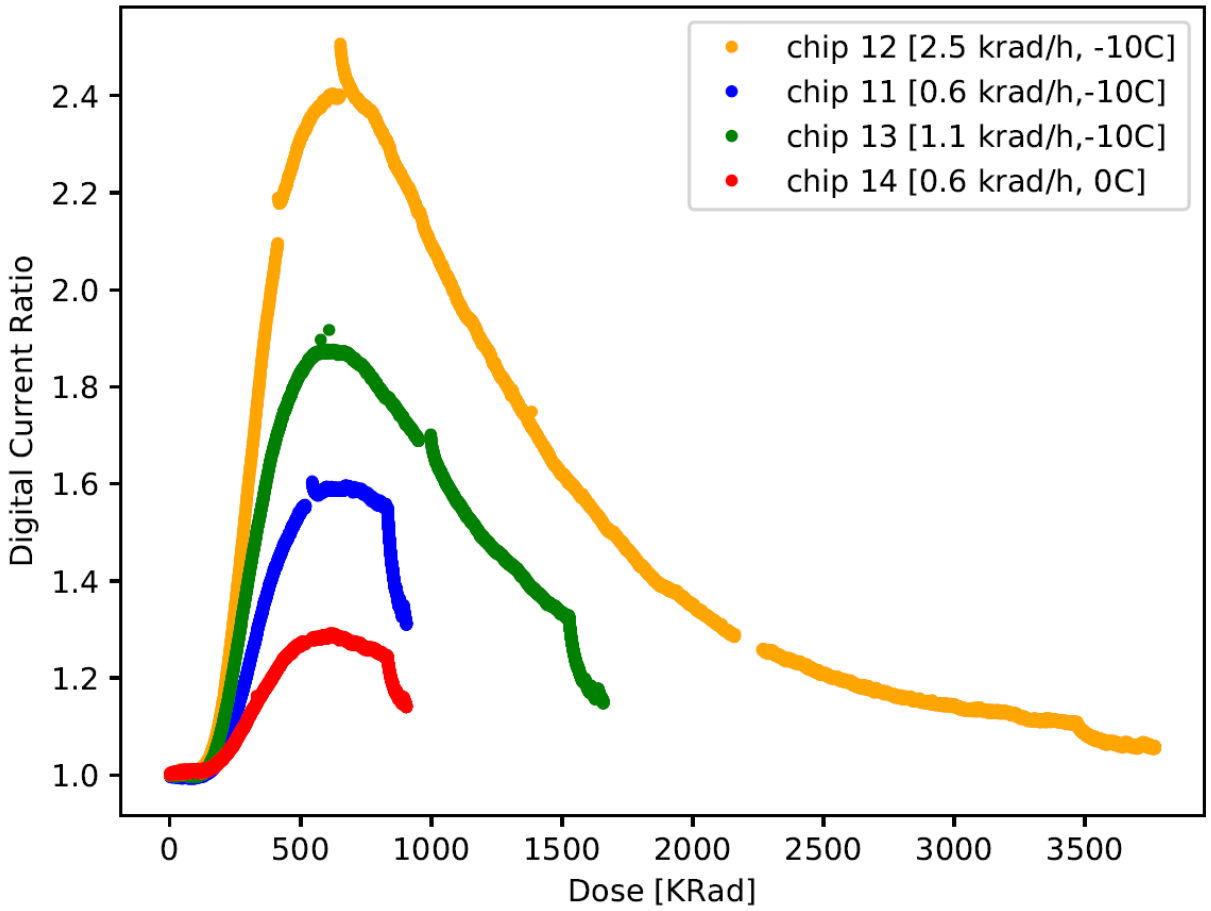


Expect some increase between single chips and modules due to:

- Strip resistance
- Inter-channel capacitance

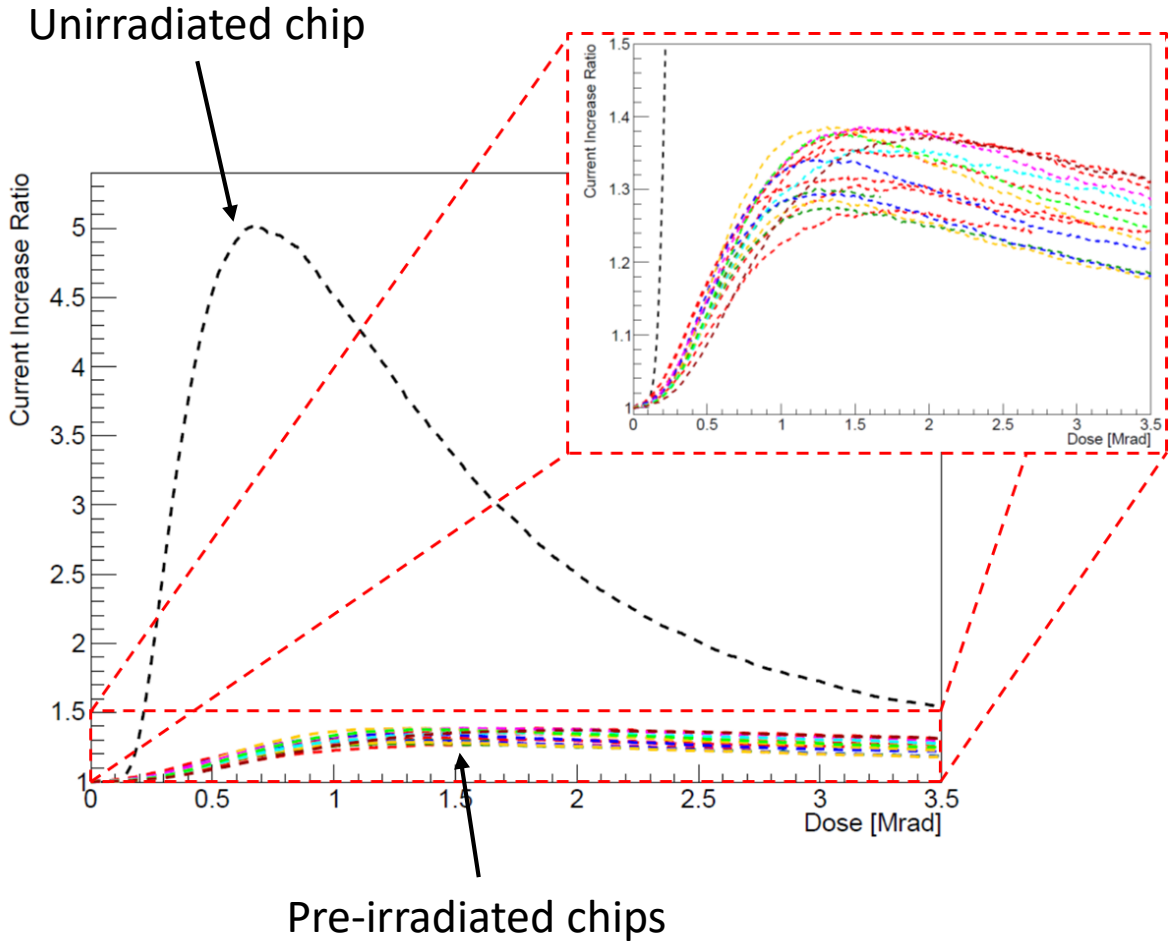
Current vs. Total Ionising Dose (TID)

- The CMOS process used here exhibits increased leakage current as a function of TID
- Was studied extensively with the previous ABC130 generation of ASIC
- Now have results for current generation of ASIC
- Similar temperature and dose rate dependence seen
- Use Co-60 to investigate representative LHC running conditions
  - Look at dose dependence at -10 C with irradiations at **0.6**, **1.1** and **2.5** krad/hr
  - Look at temperature dependence at 0.6 krad/hr at **0** and **-10** C
- These results are then fed into thermoelectric modelling of the system to understand cooling and powering requirements as a function of time



Pre-irradiation?

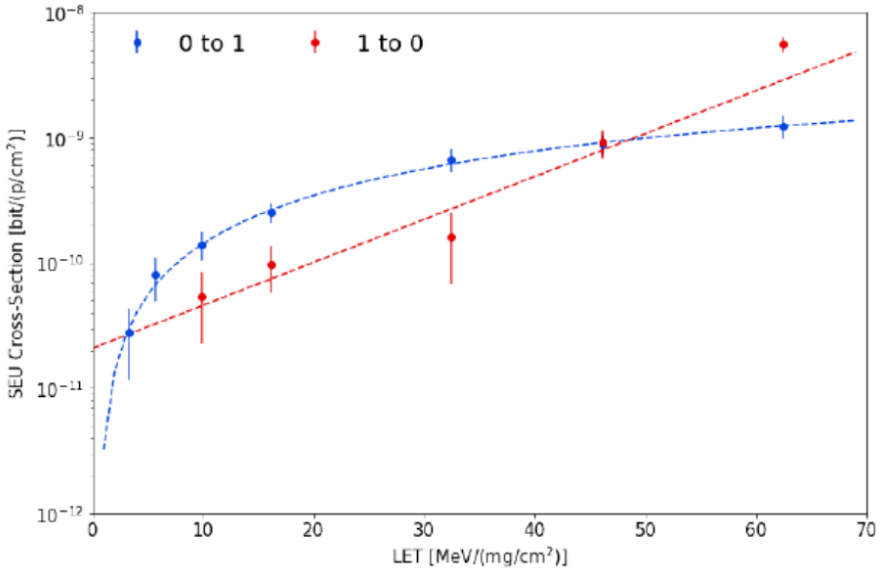
- Pre-irradiation of ASICs has now been baselined by the collaboration
- Chips are irradiated unpowered to 8 Mrad
  - Done on bare die after dicing
- This has been shown to significantly reduce the TID peak observed
  - Pre-irradiated peak 10x smaller
- Peak has been demonstrated to not return even after
  - Up to 14 months in an oven at 80 C
  - Up to 11 months running at room temperature
- These studies were done with ABC130, to be validated with ABCStar shortly



SEE testing

- SEE measurements have been performed on the current prototype chips
  - Protons at TRIUMF
  - Heavy ions at Louvain
- Some design faults found and being fixed
- No destructive SELs
- Results have been extrapolated to HL-LHC environment
  - SEU occurrence much longer than reconfigure time
- Primary SEU cause seems to be SETs in reset lines
  - All resets to be made synchronous
- Weakest link is AMAC interlock and control mechanisms
  - Full triplication of register map and safe control logic in next version
- SEE to be repeated ASAP when next chips become available

Chip	SEU rate across detector	Time to reconfigure
ABCStar	1.6 bit flips / s	6 ms
HCCStar	3.8×10^{-2} bit flips / s	135 µs
AMAC	1.4×10^{-3} bit flips / s	240 ms

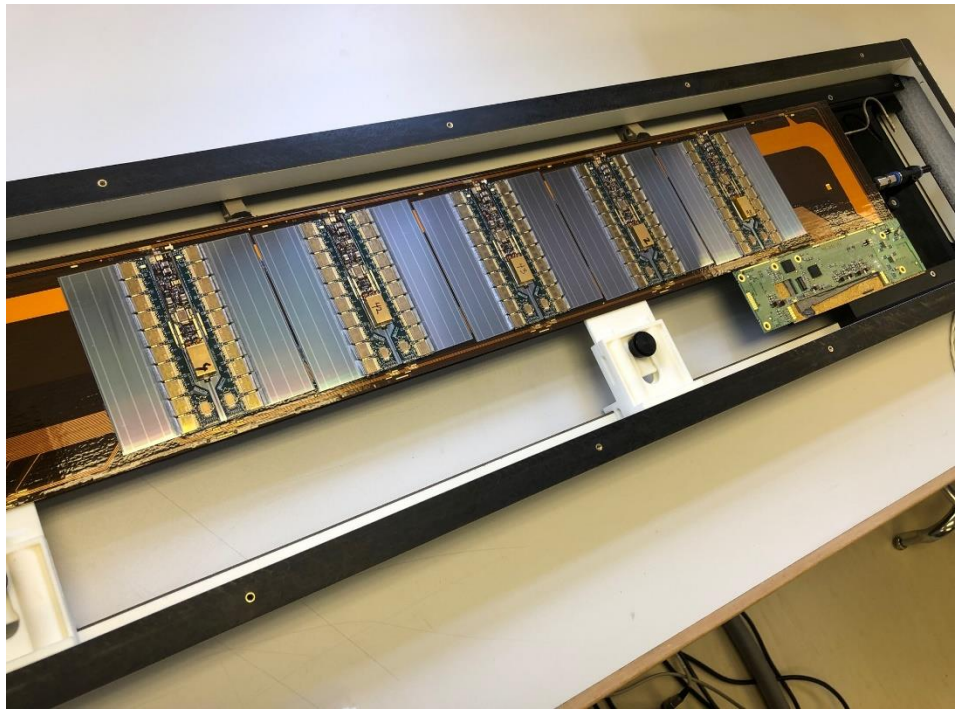


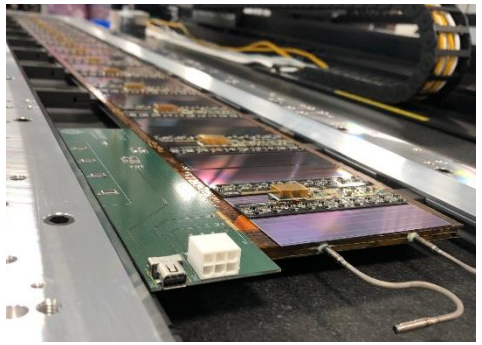
Available particles inside the cocktail:

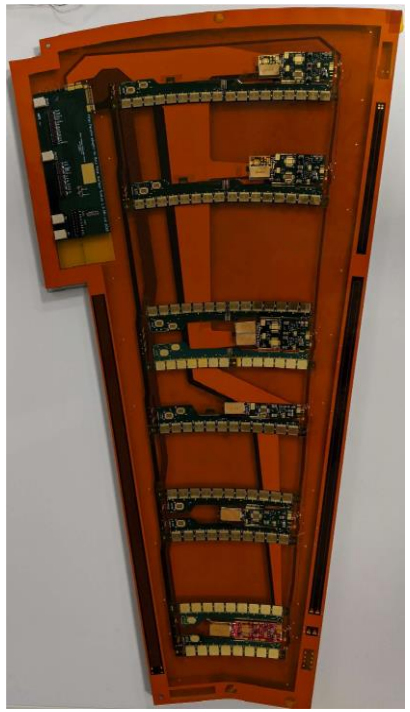
M/Q	Ion	DUT energy [MeV]	Range [µm Si]	LET [MeV/(mg/cm²)]
3.25	$^{13}C^{4+}$	131	269.3	1.3
3.14	$^{22}Ne^{7+}$	238	202.0	3.3
3.37	$^{27}Al^{8+}$	250	131.2	5.7
3.27	$^{36}Ar^{11+}$	353	114.0	9.9
3.31	$^{53}Cr^{16+}$	505	105.5	16.1
3.22	$^{58}Ni^{18+}$	582	100.5	20.4
3.35	$^{84}Kr^{25+}$	769	94.2	32.4
3.32	$^{103}Rh^{31+}$	957	87.3	46.1
3.54	$^{124}Xe^{35+}$	995	73.1	62.5

Prototype staves and petals

- Various stave/petal sized objects have been built with current prototype chips
  - 14 powerboards on stave to validate AMAC communication protocol
  - 5 SS modules on stave to validate heaviest loaded stave segment
  - 28 LS modules on stave to validate full stave electrical performance
  - 28 thermal SS modules on stave to validate mechanical and thermal performance
  - Full petal side of hybrids and powerboards to validate petal performance

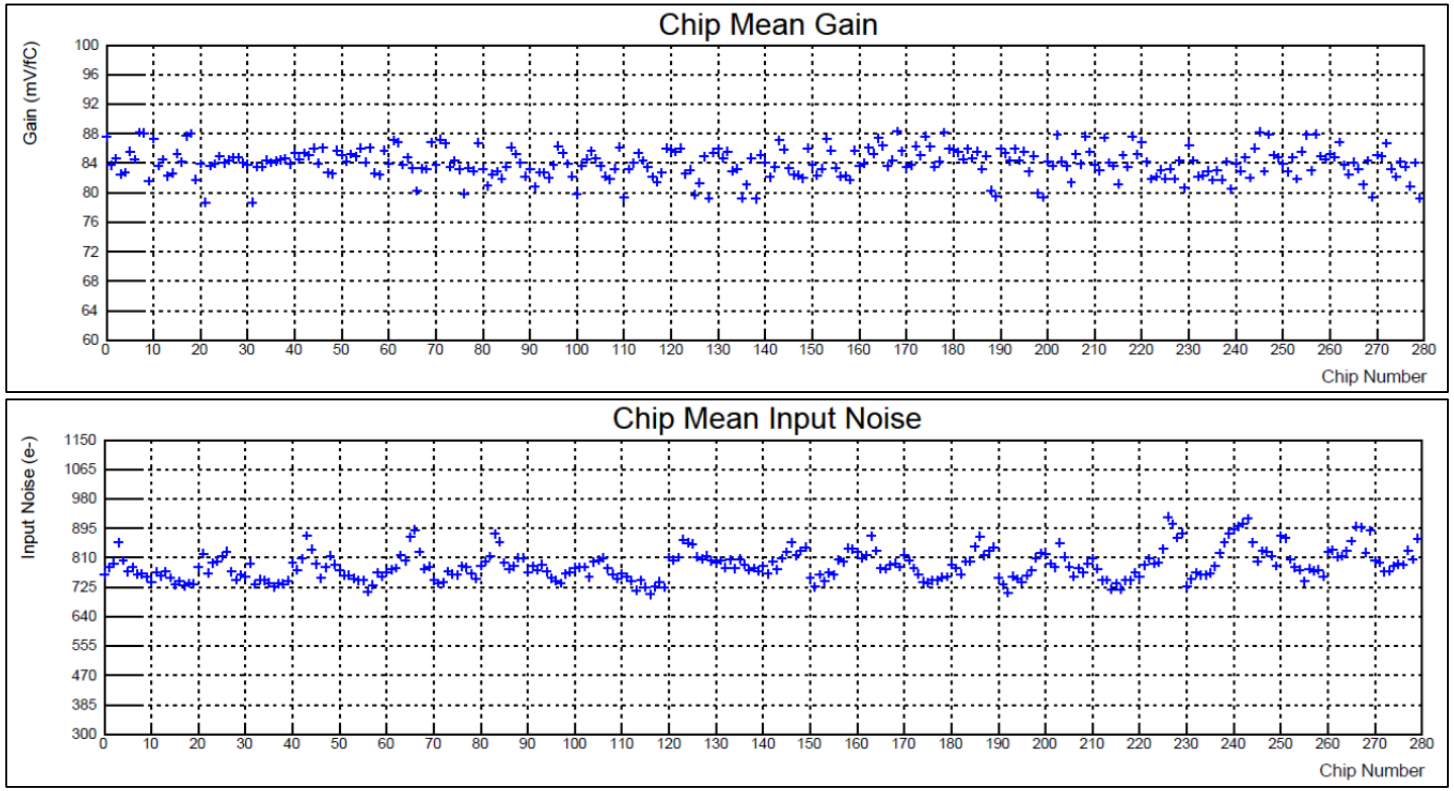


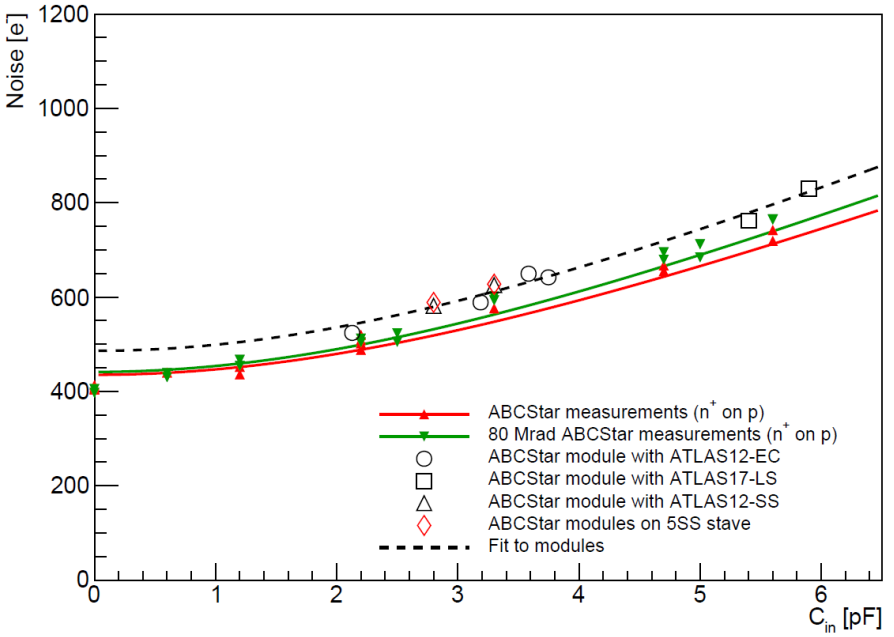




Stave performance

- Look at noise performance of modules on staves
- Module performance consistent with single chip and module level measurements
- No degradation of performance when running modules on stave

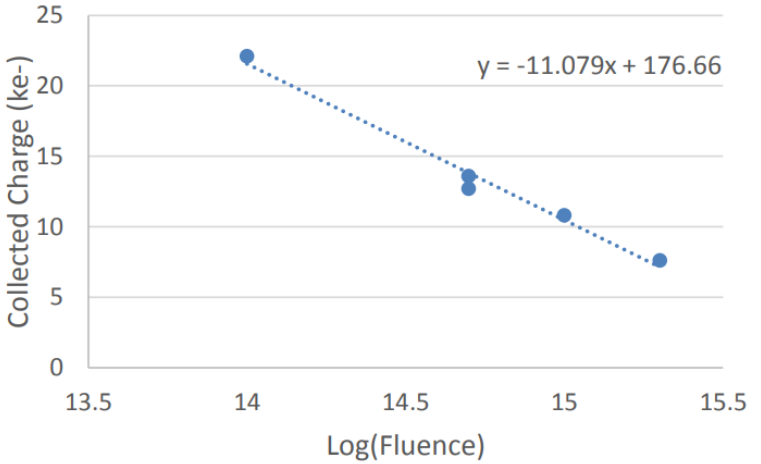


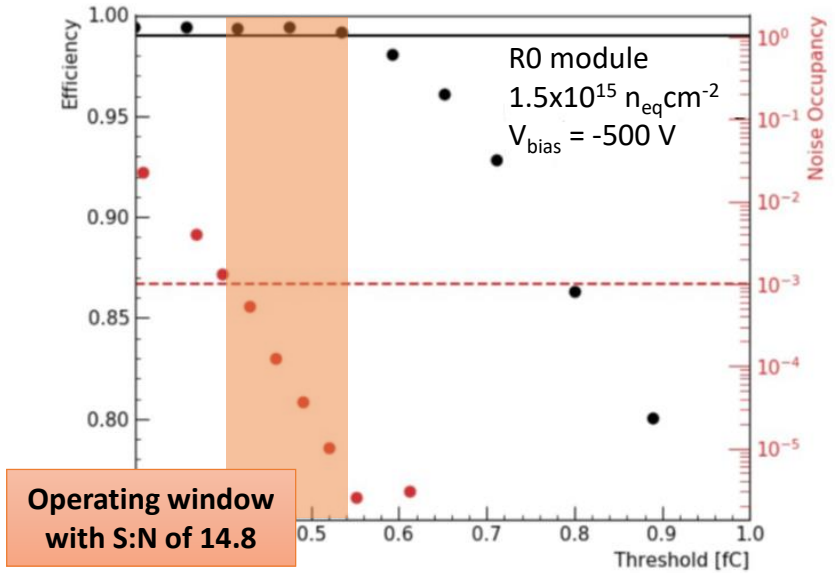


Projected end-of-life performance

- Our performance target is
  - $<10^{-3}$ noise occupancy
  - >99% efficiency
- This has been shown in the past to equate to a S:N of 10:1 at end-of-life
  - Validated in test-beam measurements
- Calculate projected end-of-life S:N using:
  - Charge collection measurements of sensors
  - Noise vs. capacitance measurements on real modules
  - Capacitance per unit length measurements of sensors
  - Calculated shot noise
  - Includes calculated capacitance increase for strips running underneath hybrids
  - Radiation levels taken from latest FLUKA simulations

Layer/Ring	Barrel	Disk 0	Disk 1	Disk 2	Disk 3	Disk 4	Disk 5
0	15.8	15.1	14.8	14.4	13.9	13.3	12.2
1	-	17.3	17.0	16.5	16.0	15.2	14.1
2	16.2	17.9	17.5	17.0	16.4	15.7	14.8
3	-	19.1	18.7	18.2	17.5	16.7	15.7
4	-	15.1	14.8	14.4	13.9	13.4	12.7
5	-	14.8	14.5	14.1	13.6	13.1	12.5





Preproduction, production and beyond

- Prototyping phase of the project is very much wrapping up
  - All Preliminary Design Reviews (PDRs) have been passed
  - Many Final Design Reviews (FDRs) have been passed or are imminent
- Module parts are starting to become available
  - Preproduction sensors starting to arrive
  - Final preproduction ASIC submissions are imminent
  - Hybrid/powerboard tendering processes are well on the way
- The return of diced ASICs initiates the start of module preproduction (July 2020)
  - 5% of the total number of modules (and staves/petals) will be built in 1 year
  - Within this window, sites are qualified to build modules
  - Provides full validation of the production chain
  - Allows us to update yield numbers which are currently “best guess” estimates
  - These parts feed into medium size system test setups
    - Provides final validation of the whole system before production starts
    - Forms stable, long term setups for future DAQ, DCS, DSS developments
- Following preproduction we have one more review, the Production Readiness Review (PRR)
- Then production starts (Q3 2021) and lasts 3.5 years to build 18,000 modules

Conclusions

- The ATLAS ITk Strips project is just coming to the end of the final prototyping phase
  - From arrival of the Star generation of ASICs at the end of 2018 to the completion of double sided 28 module LS stave at the beginning of 2020
  - Given the turn around time of just over a year, an impressive number of results and demonstrations have been completed
    - Many more results which I have not been able to show here!!
- The module design and constituents have been shown to be functional up to the required radiation tolerance
  - In fact parts have been tested well above this!
- Many of the module quality control processes are already in place with the final bits of infrastructure rolling out to sites over the next few months
- Sites are accelerating towards preproduction with PRR and production starting to come over the horizon

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THANK YOU!

QUESTIONS?