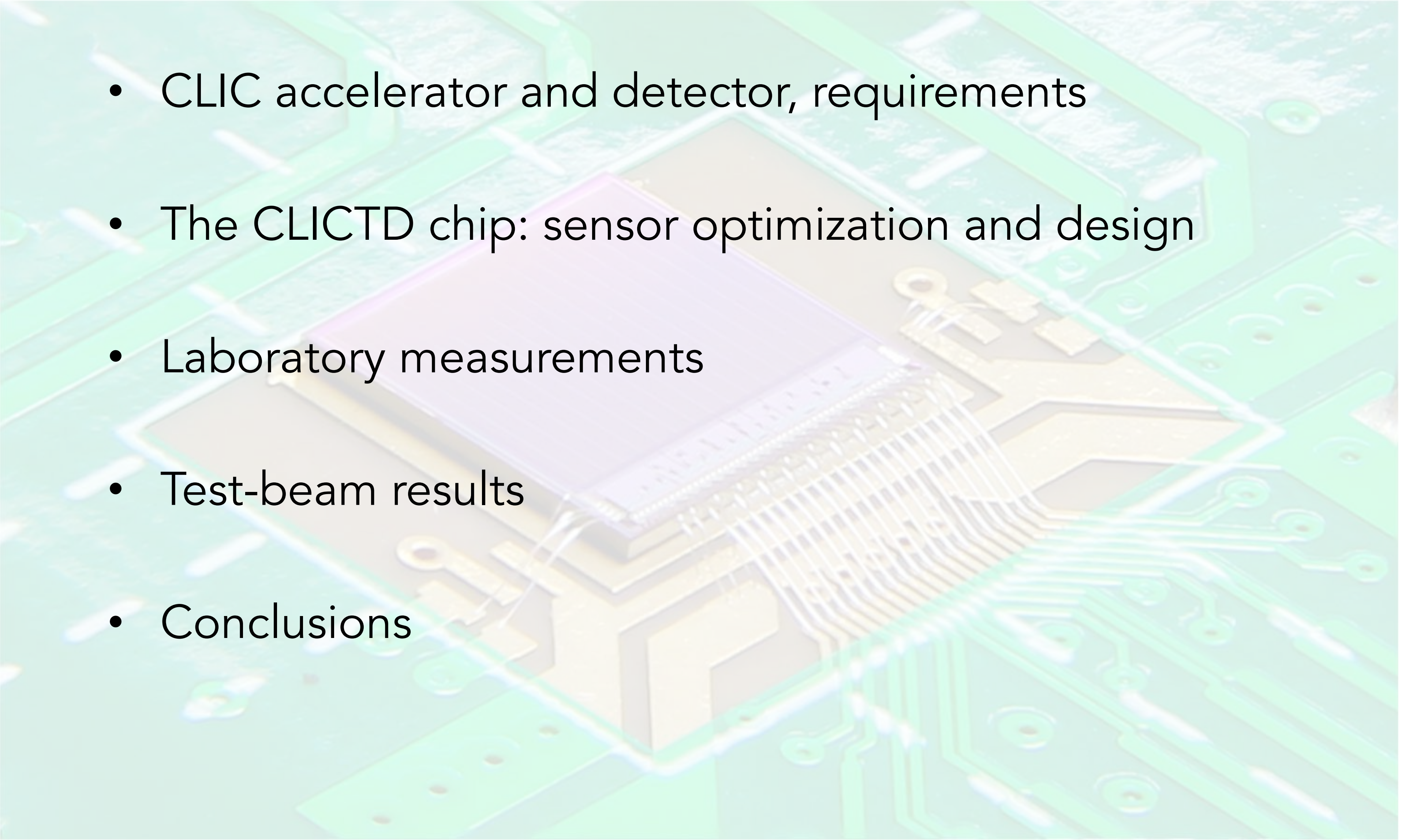
The CLICTD monolithic CMOS sensor for the CLIC tracking detector

TREDI2020, Vienna

February 18th, 2020

Dominik Dannheim (CERN)
on behalf of the CLICdp collaboration

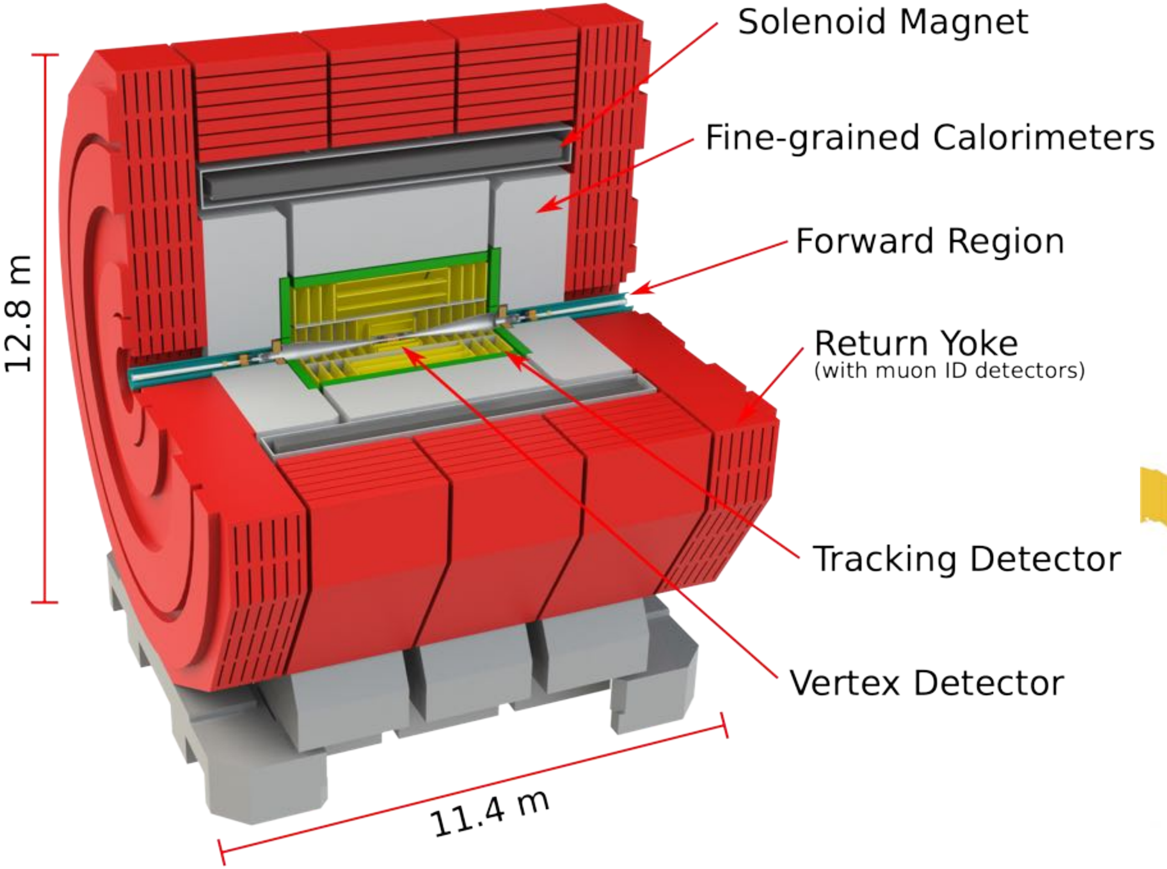
Outline



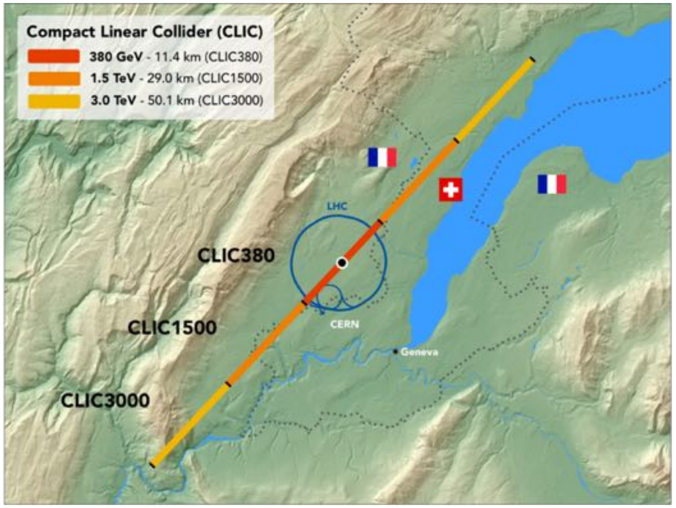
- CLIC accelerator and detector, requirements
- The CLICTD chip: sensor optimization and design
- Laboratory measurements
- Test-beam results
- Conclusions

CLIC accelerator and detector

- CLIC (Compact LInear Collider):
  linear e^+e^- collider concept for post HL-LHC phase
- $\sqrt{s}$ from few hundred GeV up to 3 TeV
  (two-beam acceleration with ~100 MV/m)
- Precision and discovery physics at the TeV scale
- Detector and physics studies within the CLICdp collaboration of 30 institutes



Staged CLIC implementation



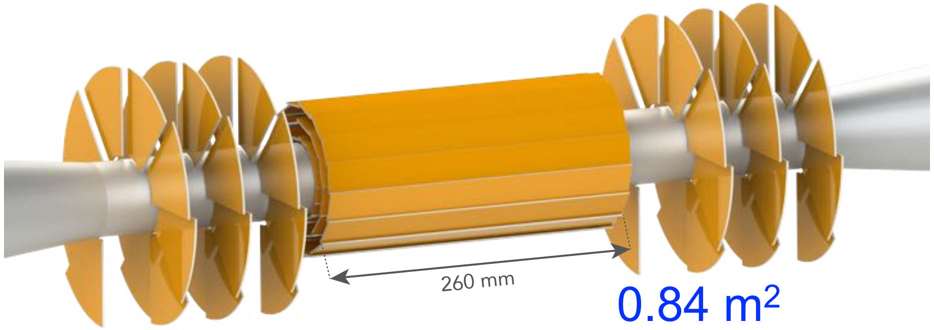
CLICdp collaboration institutes

CLIC vertex- and tracking detector requirements

Vertex detector:

- Efficient tagging of heavy quarks through precise determination of displaced vertices:
  - → Good single point resolution: σ_{SP}~3 μm
    - → Small pixels $\lesssim$ 25x25 μm^2, analog readout
  - → Low material budget: $\lesssim$ 0.2% X_0 / layer
    - → Low-power ASICs + air cooling (~50 mW/cm^2)

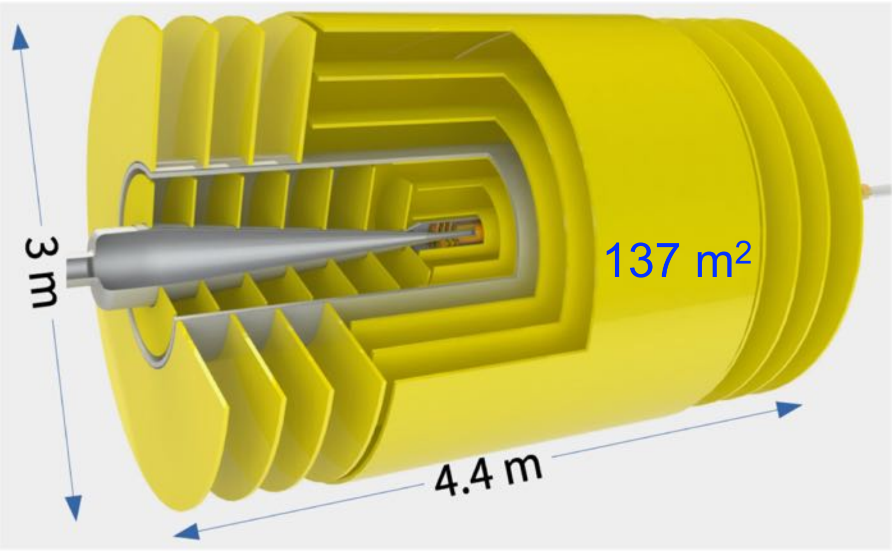
Vertex-detector simulation geometry



Tracker:

- Good momentum resolution: $\sigma(p_T) / p_T^2 \sim 2 \times 10^{-5}$ GeV^{-1}
  - → 7 μm single-point resolution (~25-50 μm Rφ pitch)
  - → Many layers, large outer radius
  - → ~1-2% X0 per layer
    - → Low-mass supports + services

Tracker simulation geometry



Both:

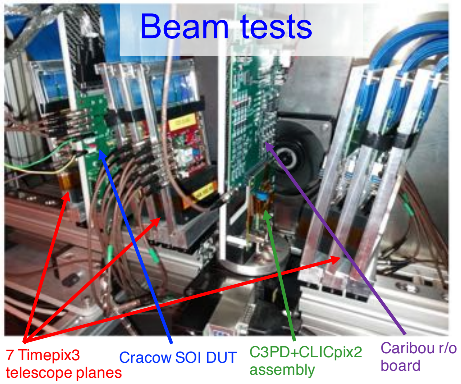
- 20 ms gaps between CLIC bunch trains of 156 ns
  - → Trigger-less readout, pulsed powering
- Few % max. occupancy from beam backgrounds
  - → Sets inner radius and limits cell sizes
  - → Time stamping with ~5 ns accuracy
    - → Depleted sensors (high resistivity / high voltage)
- Moderate radiation exposure (~10^4 below LHC!):
  - NIEL: < 10^{11} n_{eq}/cm^2/y
  - TID: < 1 kGy / year

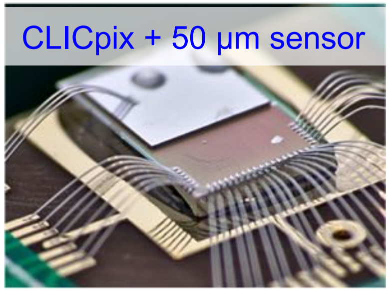
Monolithic sensor technology for large-area tracker

CLIC pixel-detector R&D

Sensor + readout technologies

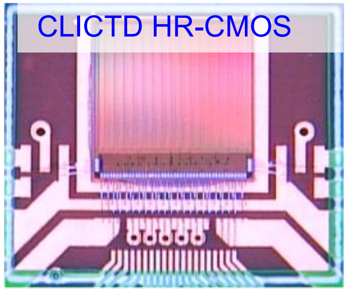
Sensor + readout technology	Currently studied for
Bump-bonded Hybrid planar sensors	Vertex
Capacitively coupled HV-CMOS sensors	Vertex
Monolithic HV-CMOS sensors	Tracker
Monolithic HR-CMOS sensor	Tracker
Monolithic SOI sensors	Vertex, Tracker


Beam tests


CLICpix + 50 µm sensor

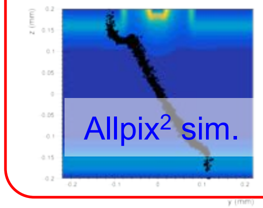

C3PD+CLICpix2 glue ass.

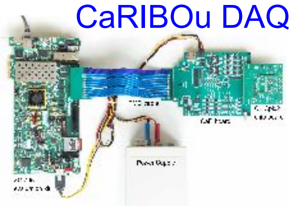

ATLASPIX HV-CMOS


CLICTD HR-CMOS

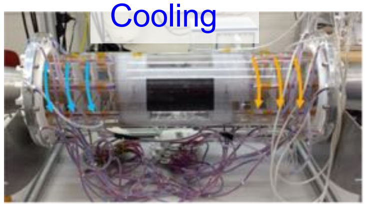

Cracow SOI

Simulation/Characterisation


Allpix^2 sim.

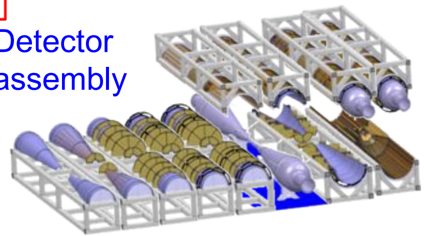

CaRIBOu DAQ

Detector integration


Cooling


Light-weight supports

Detector assembly



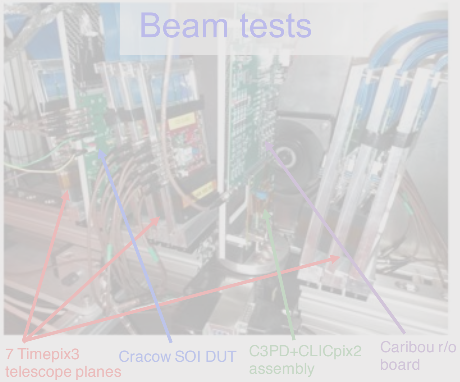
- Challenging requirements lead to extensive detector R&D program
- ~10 institutes active in vertex/tracker R&D
- Collaboration with ATLAS, STREAM, ALICE, LHCb, Mu3e, AIDA-2020

Focus on conceptual studies + technology demonstrators

CLIC pixel-detector R&D

Sensor + readout technologies

Sensor + readout technology	Currently studied for
Bump-bonded Hybrid planar sensors	Vertex
Capacitively coupled HV-CMOS sensors	Vertex
Monolithic HV-CMOS sensors	Tracker
Monolithic HR-CMOS sensor	Tracker
Monolithic SOI sensors	Vertex, Tracker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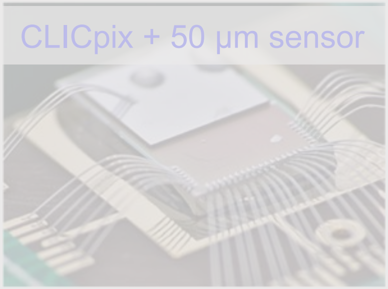
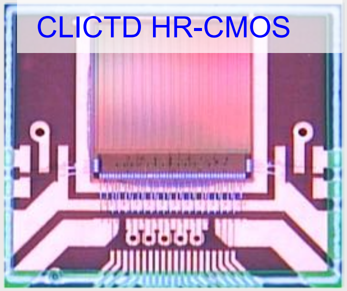

CLICpix + 50 μm sensor


C3PD+CLICpix2 glue ass.


ATLASPIX HV-CMOS

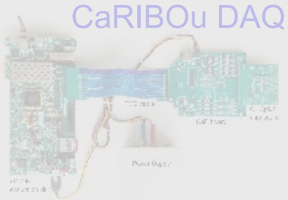
Focus of today's presentation →


CLICTD HR-CMOS


Cracow SOI

Simulation/Characterisation

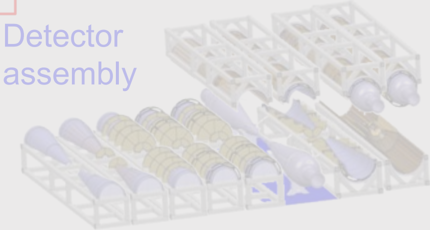

Allpix^2 sim.


CaRIBOu DAQ

Detector integration


Cooling


Light-weight supports


Detector assembly

- Challenging requirements lead to extensive detector R&D program
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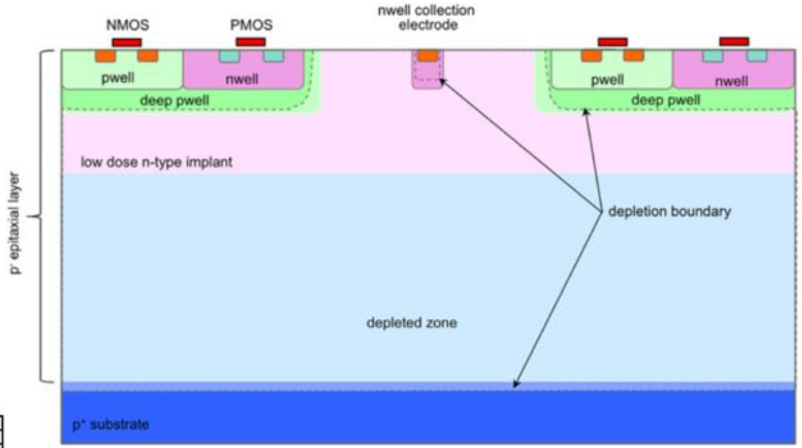
Focus on conceptual studies + technology demonstrators

Monolithic HR-CMOS sensors

- Integrated CMOS sensors on High-Resistivity (HR) substrate
- Small collection electrode separated from electronics
  → small capacitance, high signal/noise

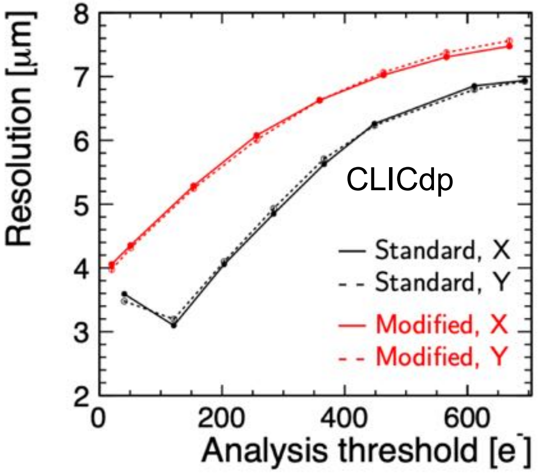
- Studied for CLIC tracker
- Tests with Investigator analog test chip (external r/o) in 180 nm modified HR-CMOS imaging process (ALICE development), various test matrices
- For 28x28 µm^2:
  99.3% efficiency (<400 e$^-$ thr.), σ_{SP}~4-5 µm, σ_t~6 ns

Modified HR-CMOS imaging process

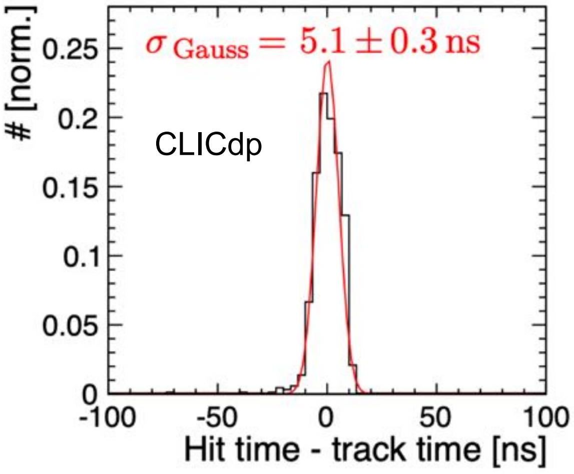


W. Snoeys et al. NIM A 871 (2017) 90–96

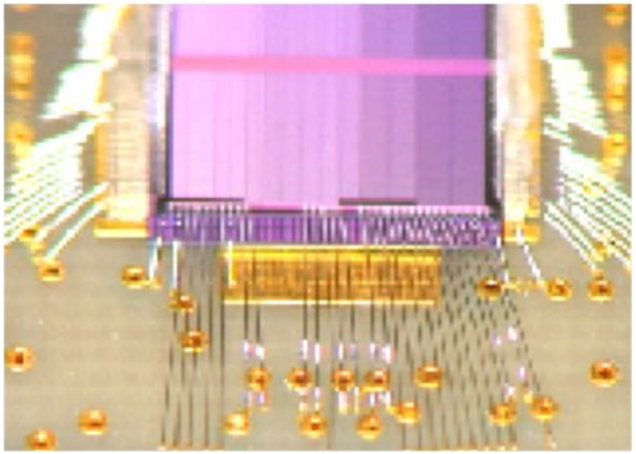
Spatial resolution vs. threshold:



Timing (modified process)



INVESTIGATOR HR-CMOS test chip

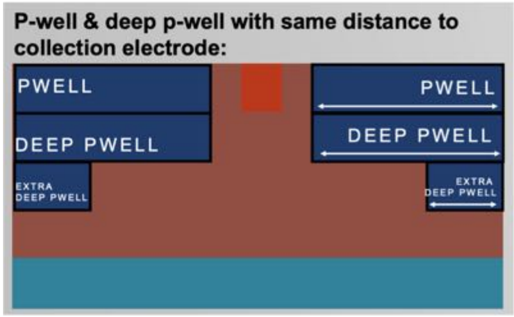


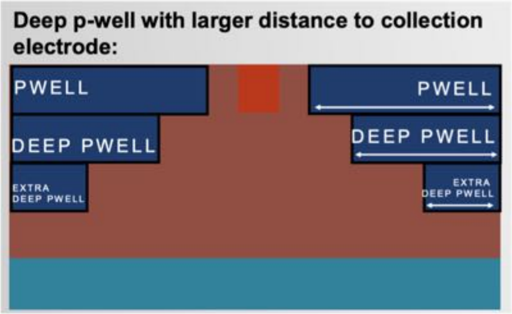
NIM A 927,187-193, 2019

Analog performance meets CLIC tracker requirements
→ Design of dedicated fully monolithic CLICTD test chip

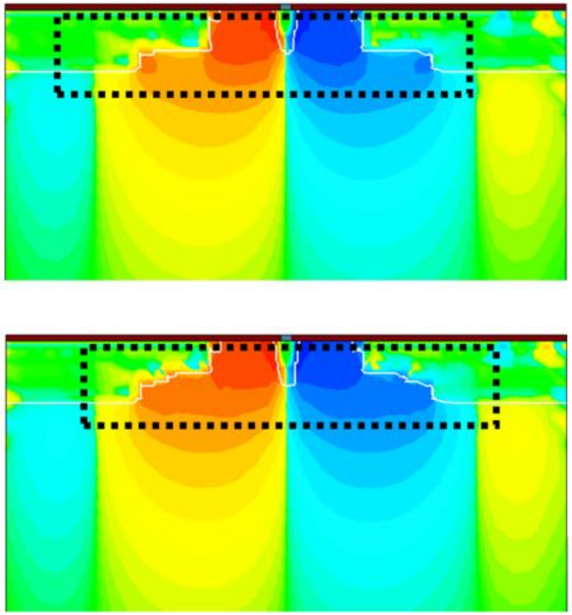
Sensor design optimisation example

p-well design



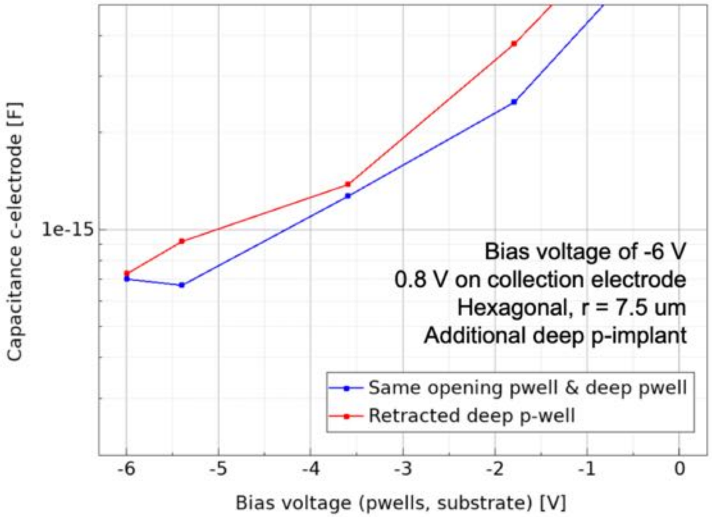


Lateral E-field



→ Retracted deep p-well increases E-field

Sensor capacitance

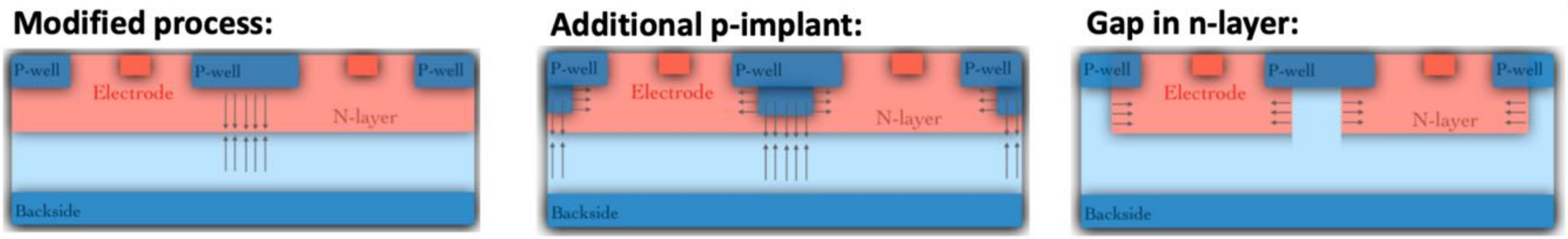


→ Retracted deep p-well helps to maintain low capacitance

- Complex depletion and E-field calls for systematic 3D-TCAD optimization of sensor layout, aiming for simultaneously achieving:
  - Full depletion (small capacitance for high S/N)
    → favours smaller p-well opening
  - Large field (fast charge collection)
    → favours larger p-well opening
- Solution:
  - Place p-wells close to electrode → full depletion around collection electrode
  - Retract deep p-well that shields circuitry → large field / fast charge collection

PhD thesis M. Munker, Bonn Univ., 2018

CMOS process optimisation

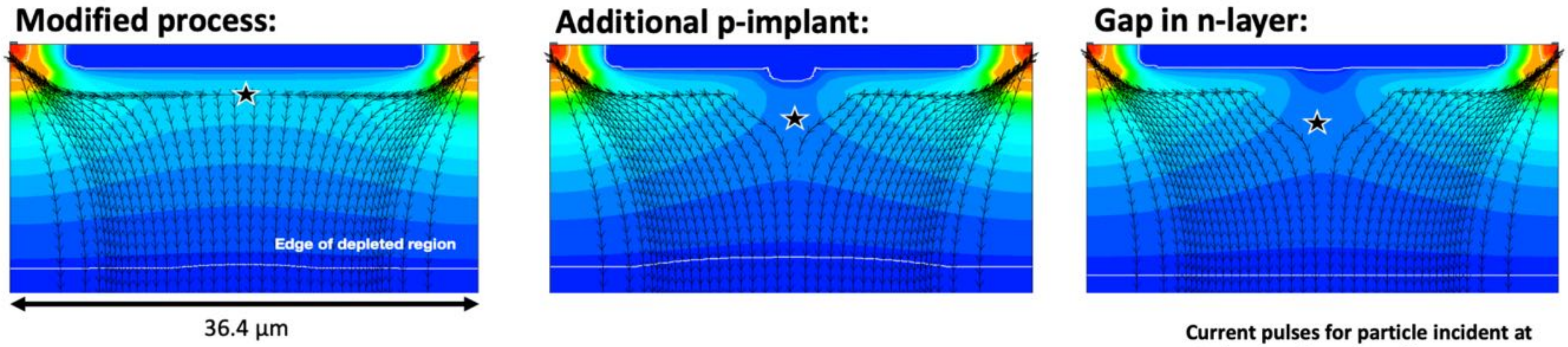


Modified process:

Additional p-implant:

Gap in n-layer:

Electrostatic potential, streamlines and electric field minimum (★):

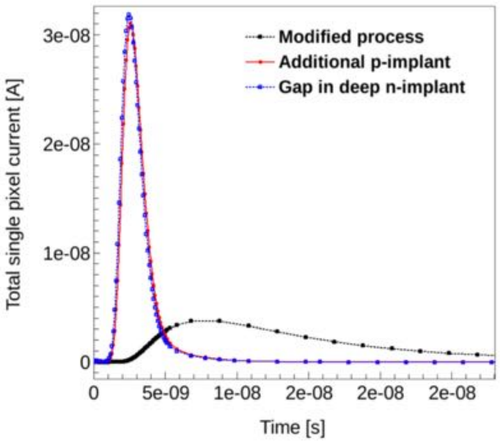


Modified process:

Additional p-implant:

Gap in n-layer:

Current pulses for particle incident at pixel corner (worst case), 3D TCAD:



- Further optimisation of modified CMOS imaging process, in collaboration with the foundry and with ATLAS/STREAM:
  - Avoid low-field regions at pixel borders by adding additional p-implants or gaps in the deep n-layer

  → Faster charge collection (CLIC requirement)

  → Improved radiation hardness (HL-LHC requirement)

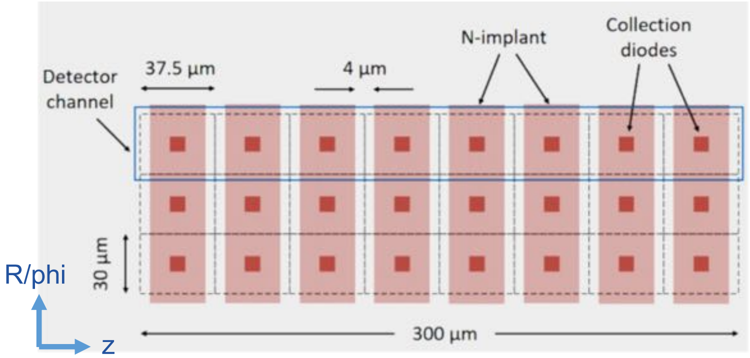
  → Reduced charge sharing (energy resolution, medical applications)
- Implemented in test chips (MALTA, CLICTD)

JINST 14 (2019) C05013

CLICTD sensor design

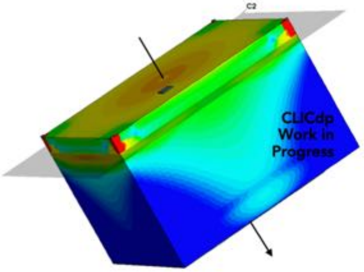
- New concept of channel segmentation for small collection-electrode sensor design, to maintain fast charge collection while reducing digital logic:
  30 x 300 μm^2 r/o channel size, 30 x 37.5 μm^2 pixel size
- TCAD geometry and process optimization
- Using process modification for faster charge collection and reduced in-channel charge sharing:
  n-layer segmentation only in long direction
  → maintain large charge sharing in short direction for better spatial resolution

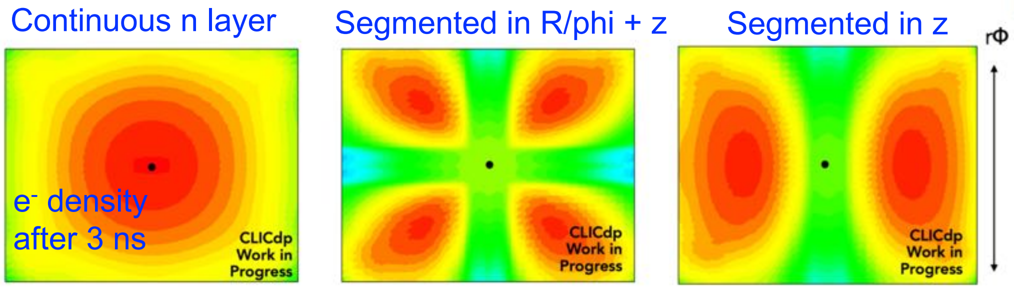
Pixel layout



TCAD optimisation:

Effect of sensor implant design on charge sharing



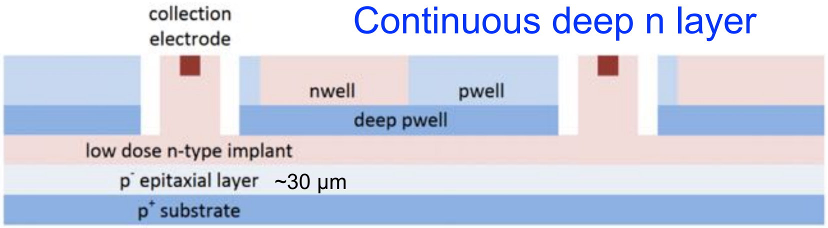


Continuous n layer

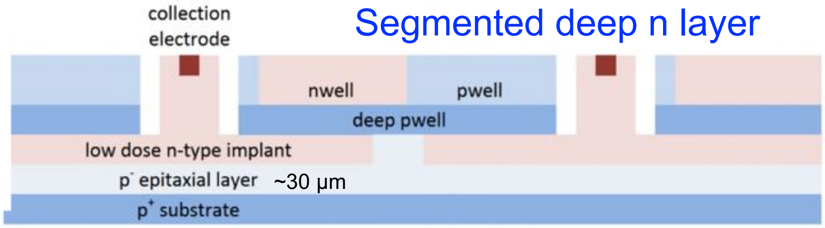
Segmented in R/phi + z

Segmented in z

Continuous deep n layer

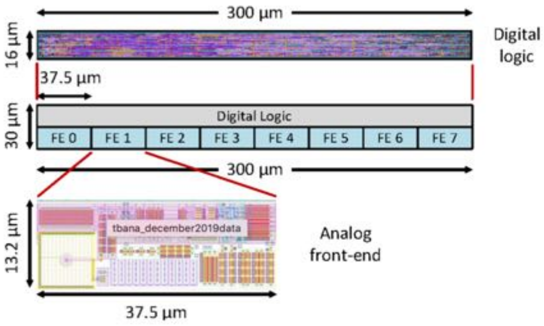


Segmented deep n layer



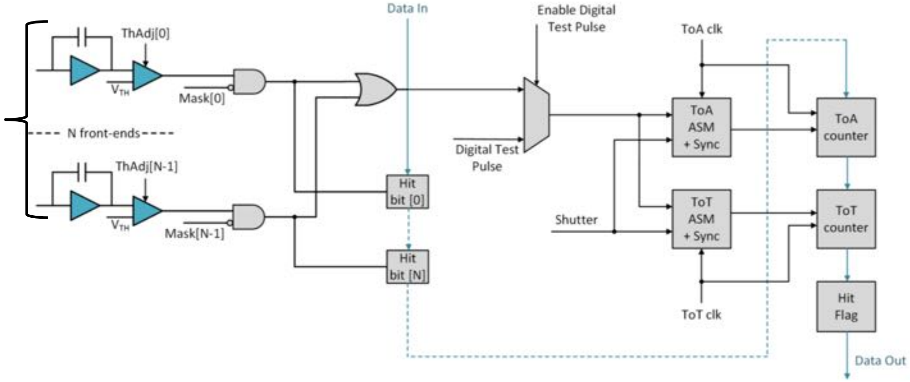
CLICTD chip design

CLICTD channel layout



8 collection diodes with individual CSA and discriminators, combined in logical OR

CLICTD channel readout

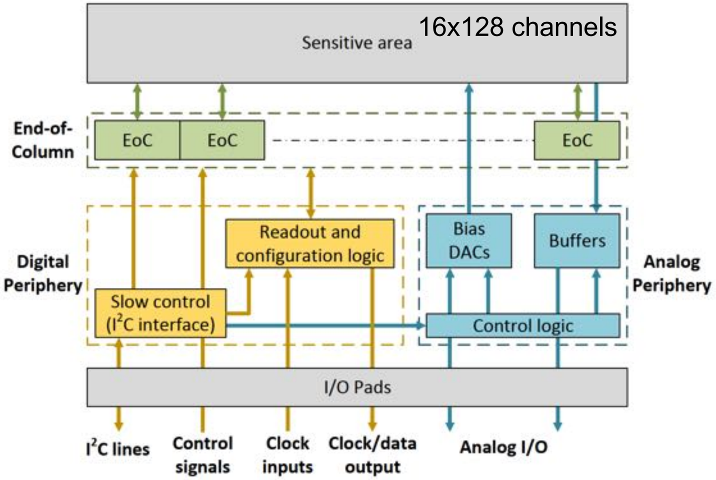


Output of logical OR passed to digital circuitry:

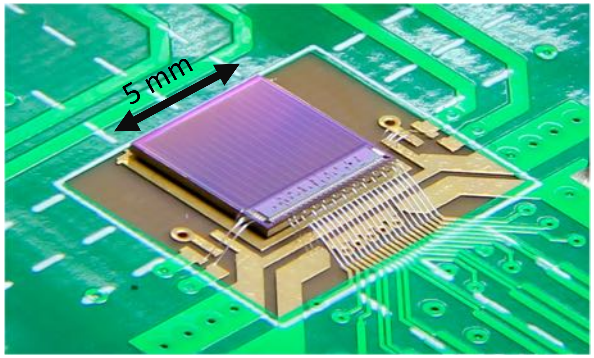
- Simultaneous 8-bit ToA and 5-bit ToT measurements
- Expect σ_{SP}~7 µm in short direction (charge sharing)
- Readout of hit pattern

  → maintain good resolution also in long direction
- 100 MHz clock to achieve 10 ns time binning

CLICTD periphery



CLICTD on test board



- Chip produced in MPW with process split: continuous n-layer / gap in n-layer in long-direction
- 30 µm epitaxial layer, 300 µm total thickness
- Thinned samples 40, 50 and 100 µm (not yet tested)

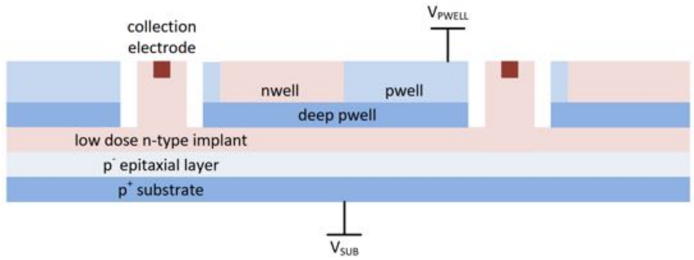
CLICdp-Conf-2018-008

CLICTD electrical characterisation

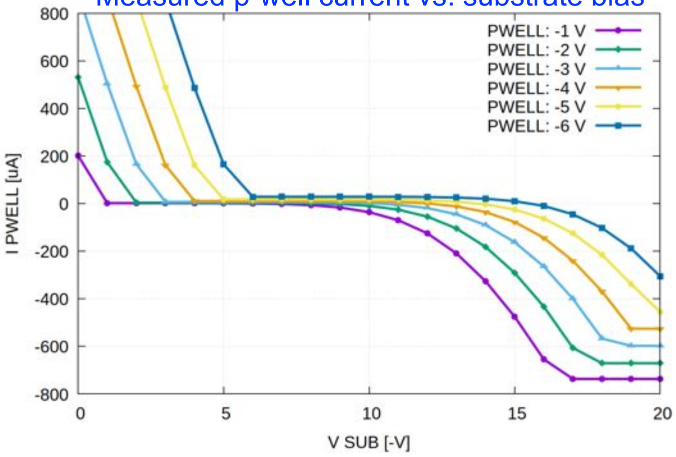
- Sensor leakage current characteristics measured for P-well and substrate bias
- Sensor can be safely operated with low leakage currents (few µA)
  at the maximum p-well bias of ~-6 V, for which the technology is rated

- Note: Optimal sensor performance (timing, charge sharing) does not require the highest possible bias voltage (*JINST 14 (2019) C05013*)

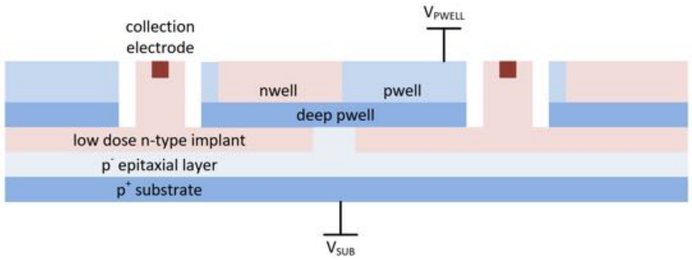
1st process variant: continuous n-layer



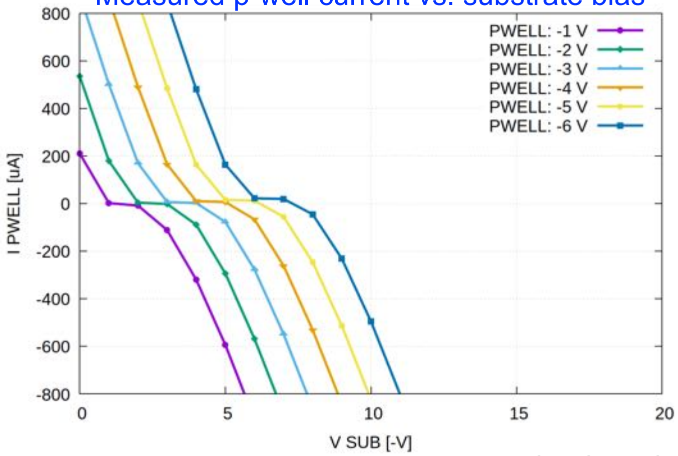
Measured p-well current vs. substrate bias



2nd process variant: gap in n-layer



Measured p-well current vs. substrate bias



CLICdp-Conf-2019-009

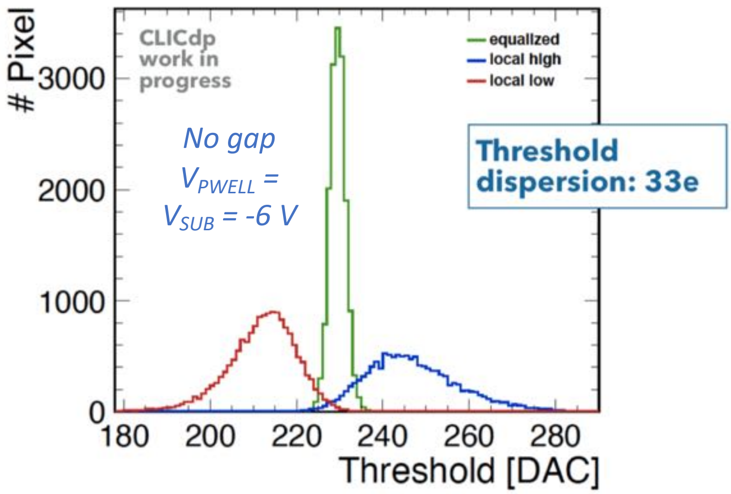
CLICTD equalization and calibration

- Laboratory measurements with test pulses and x-rays:
  - Find optimal operating parameters
    → local threshold adjustments
  - Calibrate device response
    → obtain noise and threshold in physical units
- Complication of monolithic imaging process technology:
  - Operation points of amplifier very sensitive to operation parameters (e.g. p-well bias)
  - Simulation models are only valid for 0V bias

→Iterative tuning of chip settings + calibrations
for all relevant bias settings

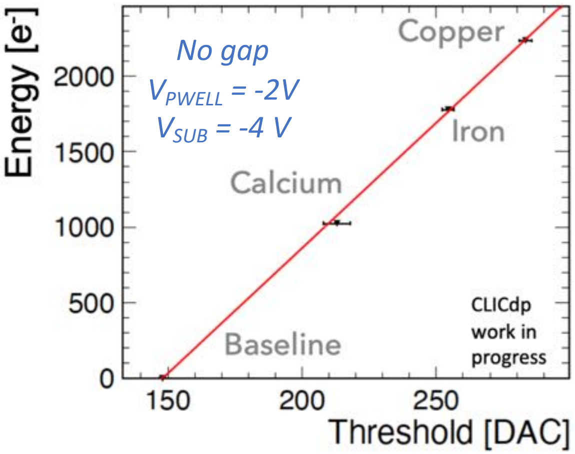
- Preliminary results for continuous n-layer, $V_{sub}=V_{pwell}=-6V$:
  Noise ~11 e^-, threshold dispersion ~33 e^-, min. threshold ~135±5 e^-

Example for threshold equalisation

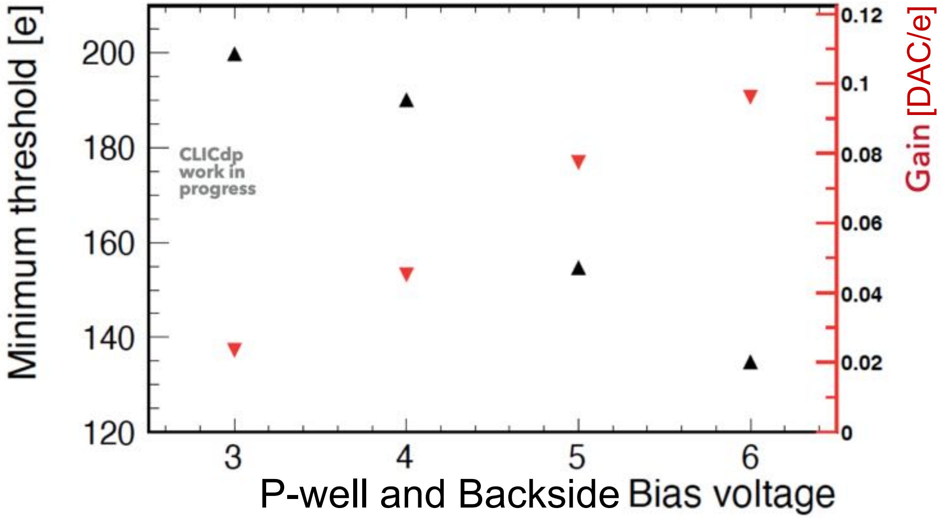


Threshold dispersion: 33e

Example for energy calibration with x-rays



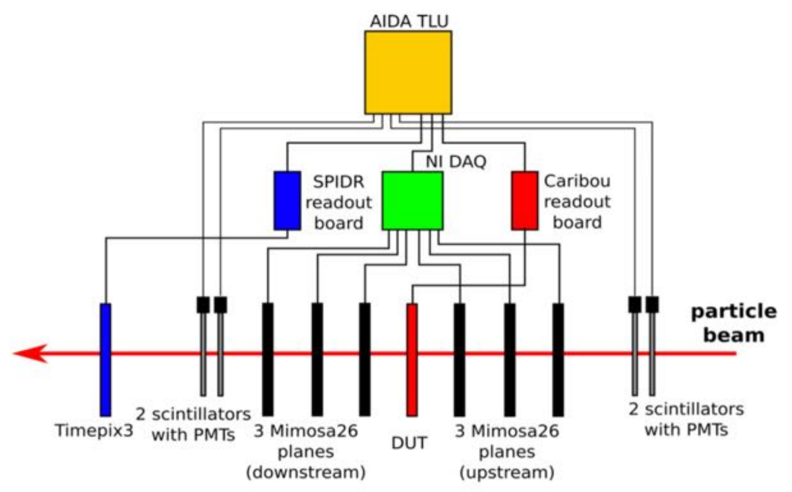
Minimum threshold and gain



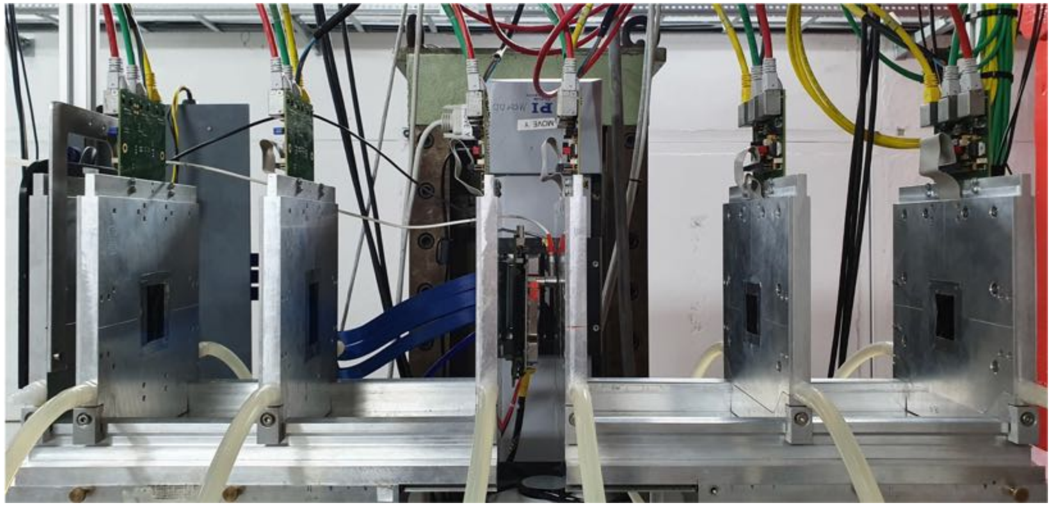
Test-beam measurements

- Beam tests at DESY II:
  - 5.4 GeV electron beam (few hundred Hz/cm^2)
  - 6 Mimosa26 telescope planes, General-Broken-Lines track fits → ~2.2-2.5 µm track resolution on DUT
  - Timepix3 timing plane → ~1.5 ns track-time resolution
  - Caribou readout for CLICTD, integrated in EUDAQ2 (triggered shutter operation)
  - Online monitoring, reconstruction and analysis with Corryvreckan

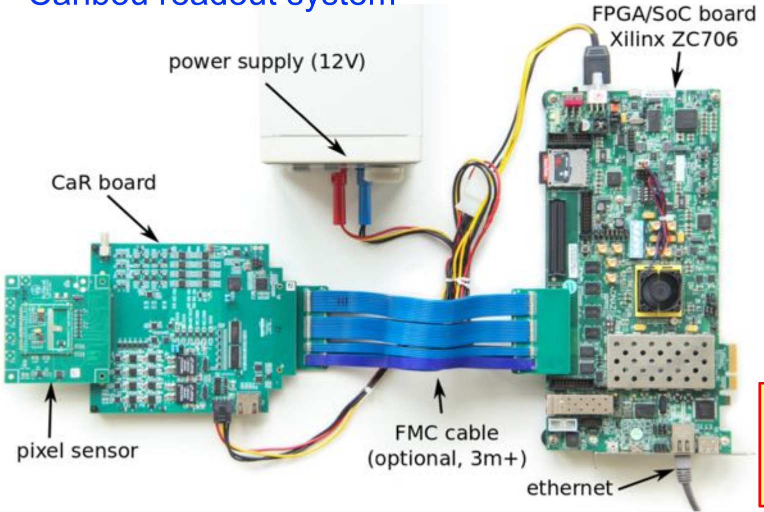
Schematic of CLICdp test-beam setup at DESY:



DESY TB21 setup in September 2019



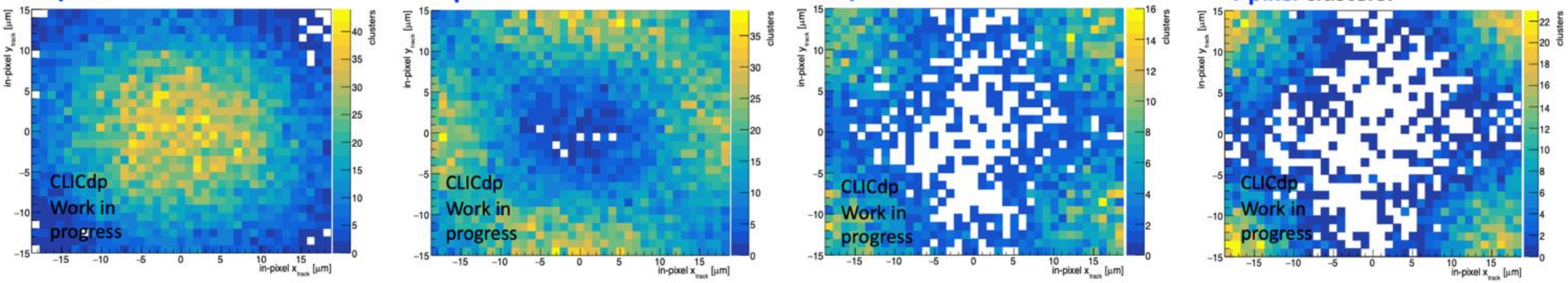
Caribou readout system



A big **thank you** to our friends from the DESY test-beam team for the sustained support and collaboration!

Charge sharing / clustering

In-pixel hit maps for different cluster sizes (-6V, no gap, THL=171 e$^-$)

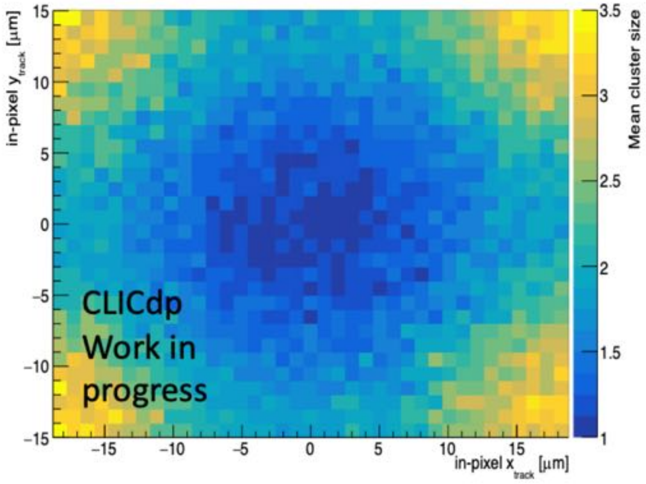

1-pixel clusters:

2-pixel clusters:

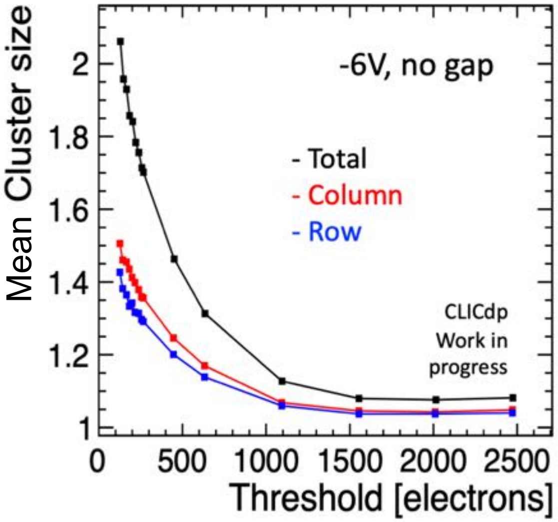
3-pixel clusters:

4-pixel clusters:

In-pixel mean cluster size (-6V, no gap)



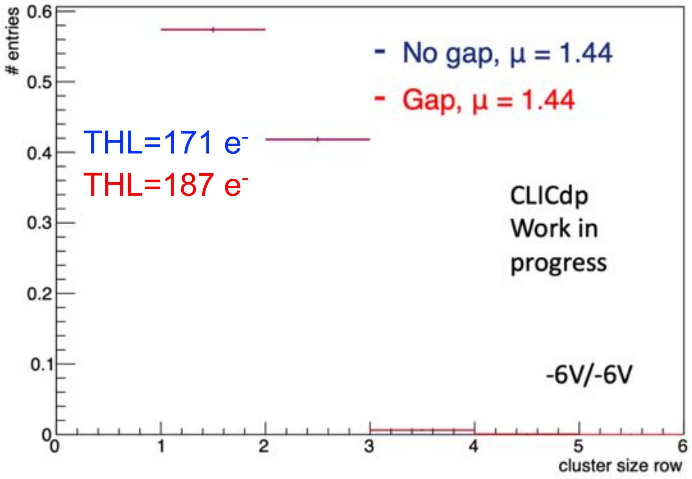
Mean cluster size vs. threshold



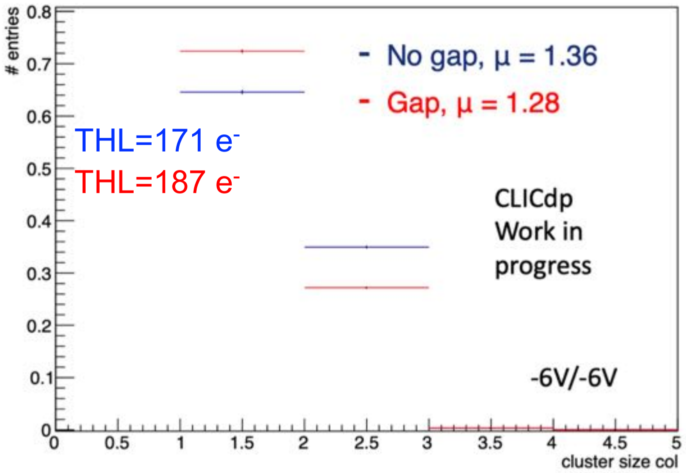
- Charge sharing / clustering as expected from pixel geometry and electric field

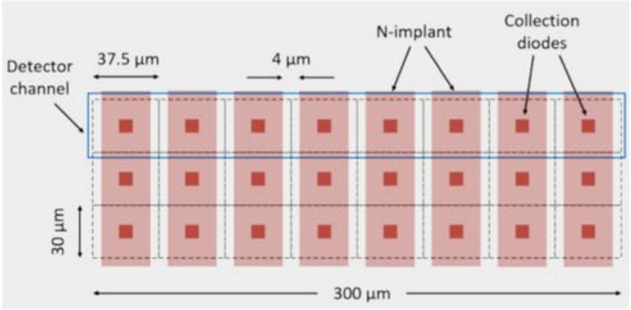
Clustering: comparison of process variants

Cluster size row, distributions **for both process variants**:

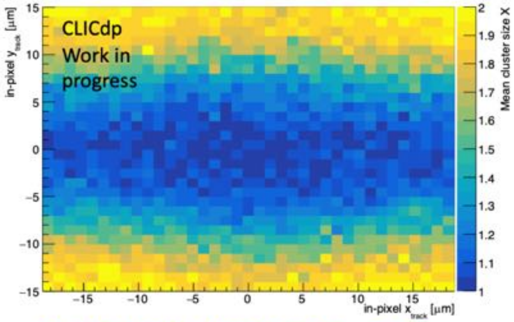


Cluster size column, distributions **for both process variants**:

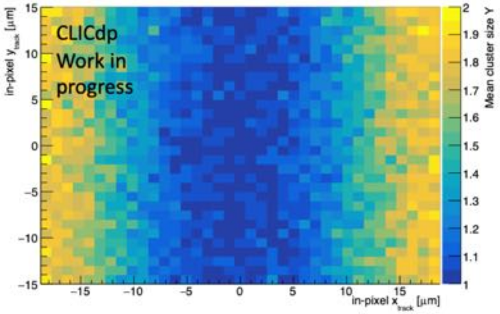




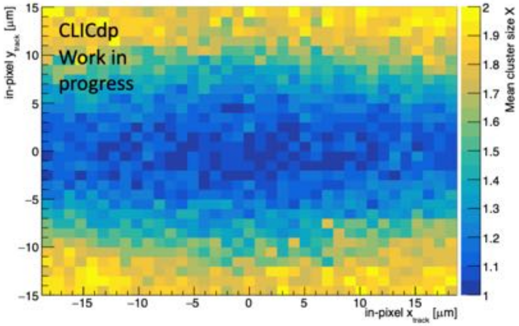
In-pixel row cluster size - **no gap**:



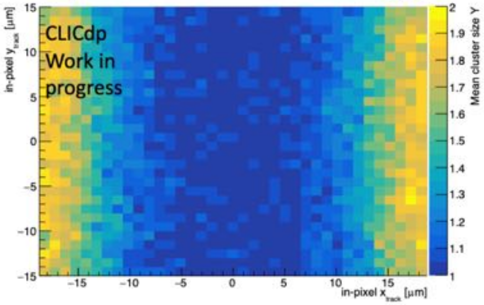
In-pixel column cluster size - **no gap**:



In-pixel row cluster size - **gap**:



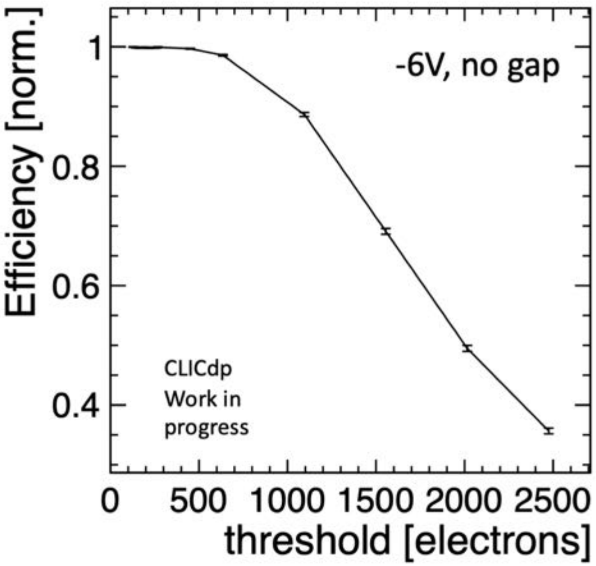
In-pixel column cluster size - **gap**:



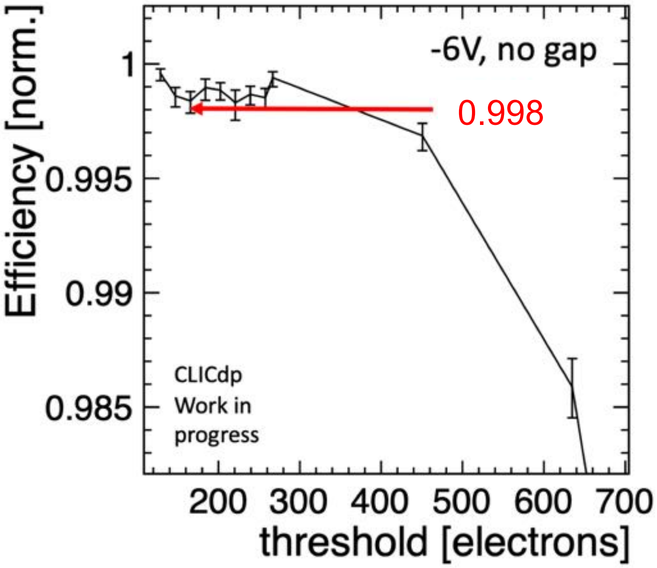
Gap in n-layer reduces cluster size in column direction, as expected

Efficiency

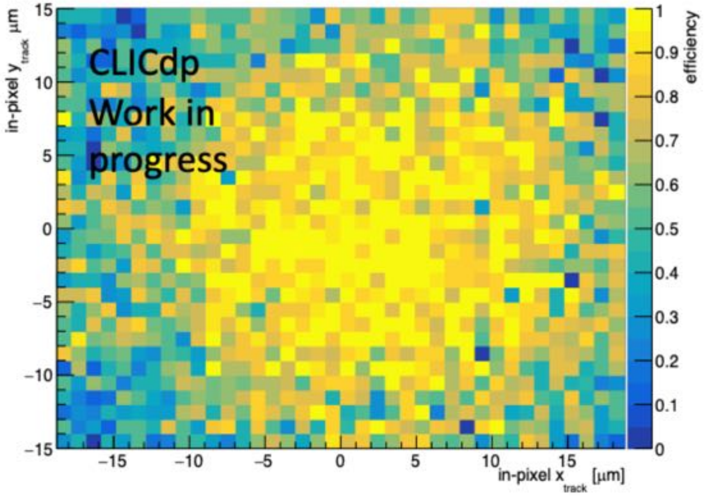
Single hit efficiency



Single hit efficiency (zoom)



In-pixel hit efficiency @ 1500 e^- threshold

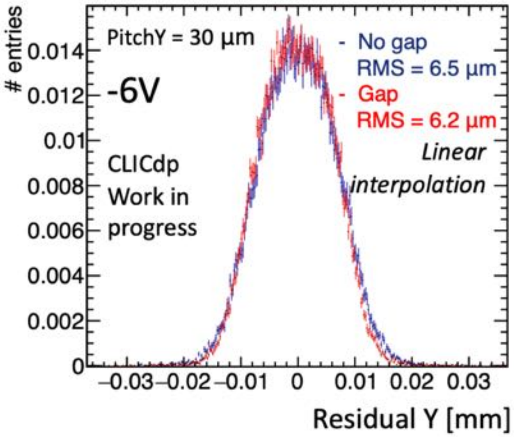


- For both process variants:
  Full hit efficiency (>99.8%) for threshold values below 400 e^-
- Expect signal MPV ~2.4ke^- for 30 µm epitaxial layer

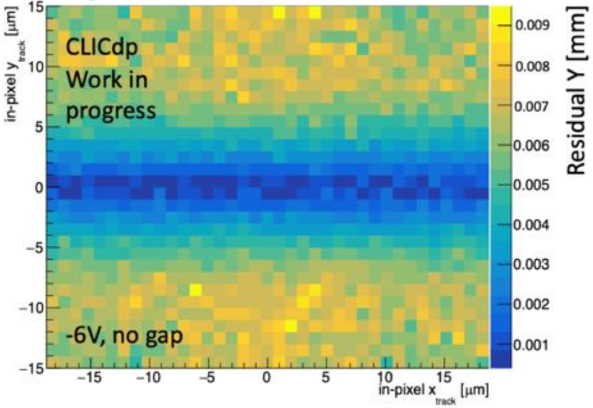
→ inefficiency at higher thresholds from cut into seed-pixel signal

Spatial resolution

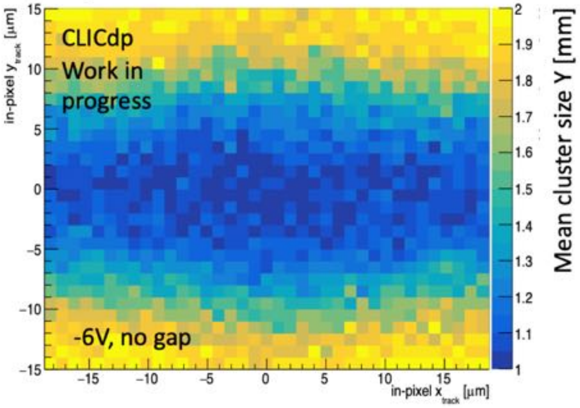
Row residual distribution:



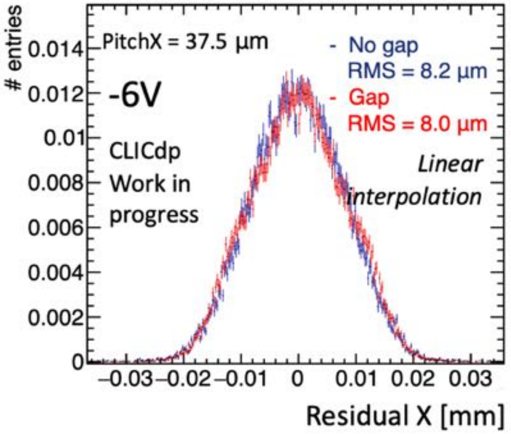
In pixel row residual:



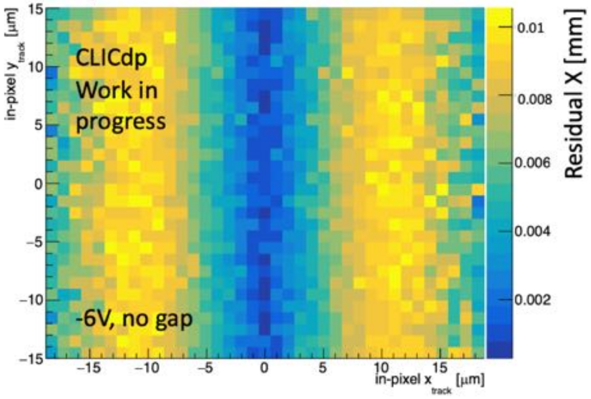
In pixel row cluster size:



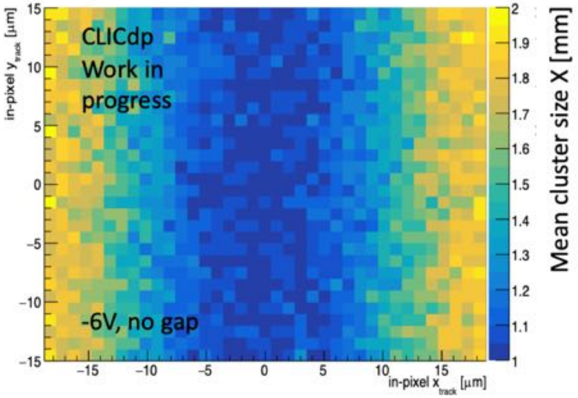
Column residual distribution:



In pixel column residual:



In pixel column cluster size:

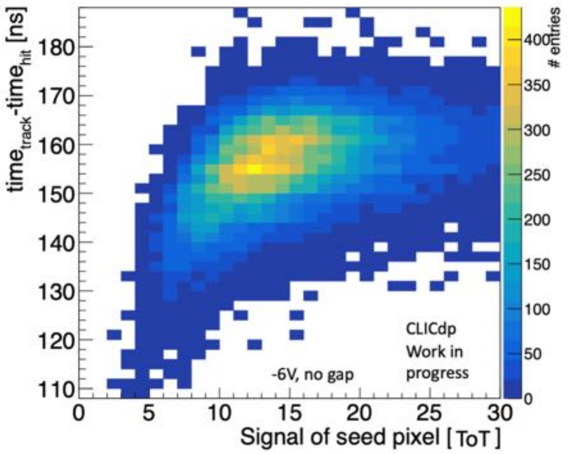


- Hit residuals in R/phi <7 µm (with linear interpolation and telescope resolution not unfolded)
- Strongly affected by non-linear field distribution over the pixel cell

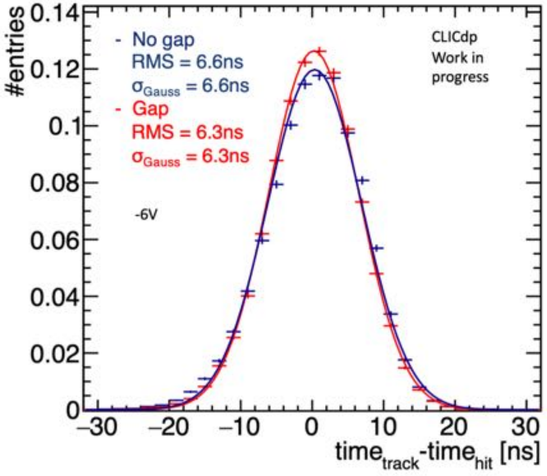
→ Will be improved with advanced hit-reconstruction methods (eta-correction for non-linear charge sharing, multi-variate position reconstruction)

Timing performance

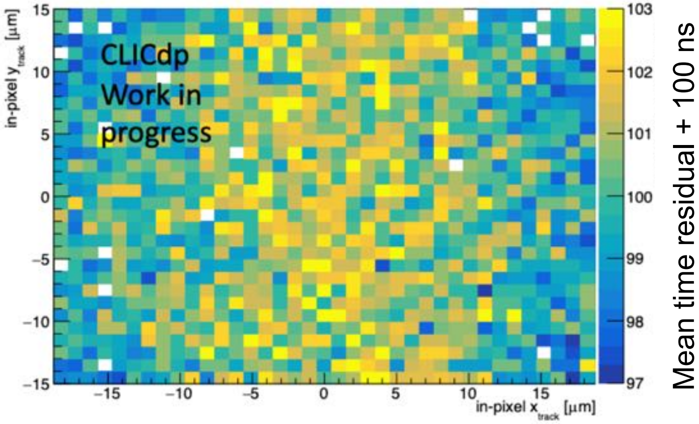
Time-walk for seed pixel:



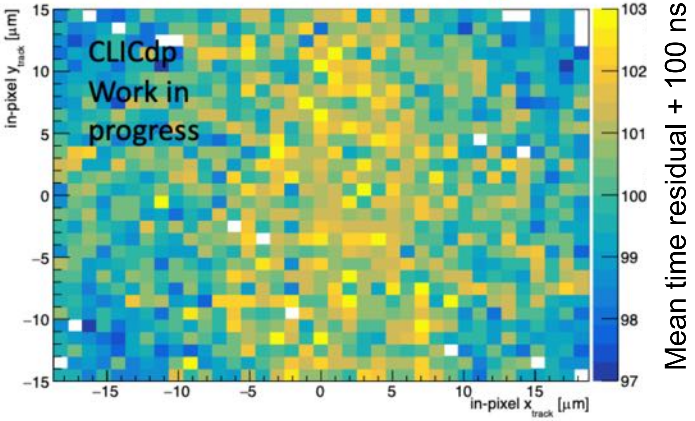
Hit-time residuals after time-walk correction



In-pixel time residual - **no gap:**



In-pixel time residual - **gap:**



- Hit-time residuals ~6 ns
  - Includes contribution of ~1.5 ns from Timepix3 track time stamps
  - Limited by 10 ns CLICTD ToA time bins

- Systematic offsets of in-pixel time residuals suggest further room for improvement

Conclusions / Outlook

- Stringent requirements for CLIC vertex and tracking detectors have inspired broad and integrated technology R&D program
- Optimisation of CMOS imaging process to meet requirements of CLIC (and HL-LHC)
- Developed CLICTD monolithic sensor for CLIC tracker requirements
- Encouraging preliminary performance results, meeting CLIC requirements:
  - Noise: ~11 e^-, minimum detection threshold: ~135 e^-
  - Efficiency: >99.8% (for <400 e^- threshold)
  - Spatial resolution: ~6 µm, temporal resolution: ~6 ns
- Process variants show the expected trends, detailed comparison in progress

- Next steps:
  - Study performance for inclined tracks / thinned samples
  - Re-submission of CLICTD with Czochralski wafers for increased depletion

- Future developments:
  - ATTRACT FASTPIX timing test chip → explore timing capabilities of technology
  - Qualification of 65 nm imaging process → smaller pixels / enhanced performance

Thanks to everyone who contributed to the results, and especially to Magdalena Munker, Katharina Dort and Iraklis Kremastiotis for providing material!

Part of the measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)

Additional Material

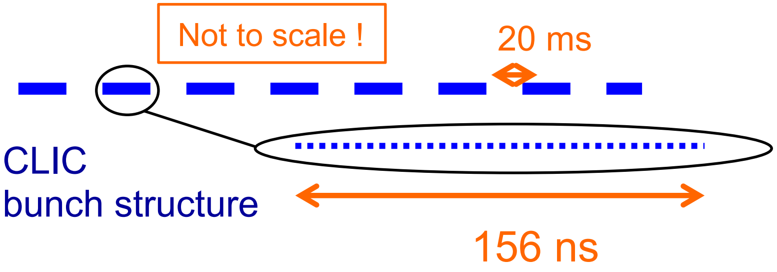
Experimental conditions at CLIC

- CLIC operates with bunch trains, 50 Hz repetition rate

→ Low duty cycle

→ Trigger-less readout between trains

→ Allows for power-pulsed operation of detector, to reduce average power consumption


Not to scale !

20 ms

CLIC bunch structure

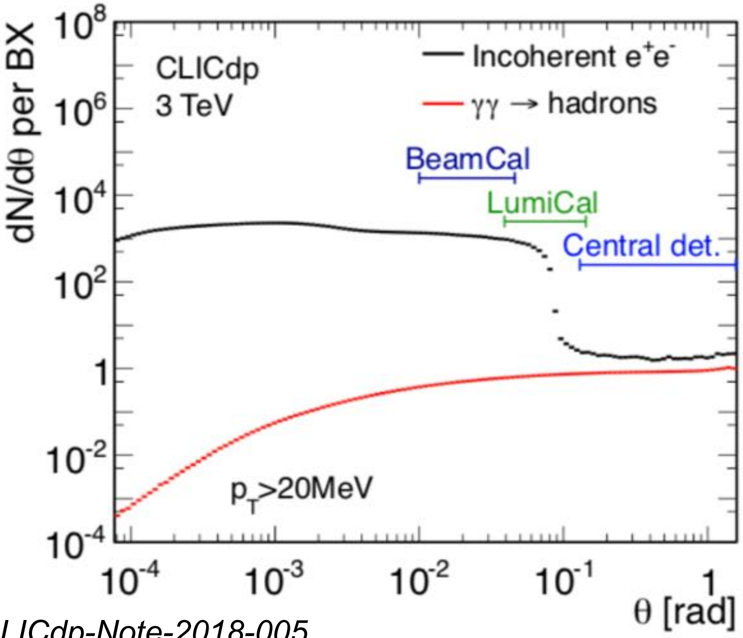
156 ns

- Collisions within 156 ns bunch trains
- High E-fields lead to Beamstrahlung

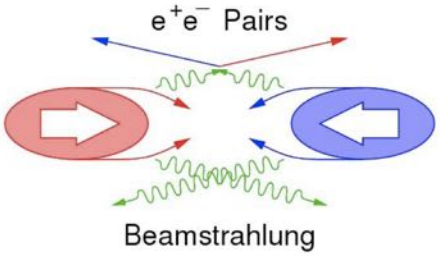
→ High rates of beam-induced background particles

→ Drives detector design (layout, granularity, timing)

Very small bunches:
40 nm (x) x 1 nm (y) x 44 µm (z)
(at 3 TeV)



CLICdp-Note-2018-005



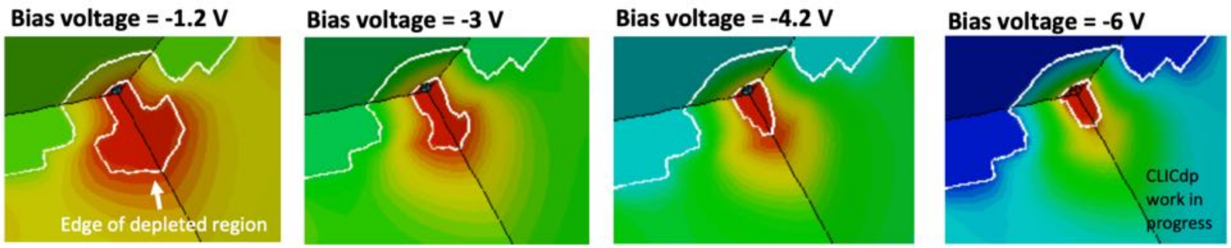
Main backgrounds in detector

- **Incoherent e+e- pairs**
  - 19k particles / bunch train at 3 TeV
  - Constrains beam pipe radius, granularity
- $\gamma\ \gamma$ →hadrons events
  - 17k particles / bunch train at 3 TeV
  - Constrains granularity, layout, impacts physics

High instantaneous hit rates (up to 6 GHz/cm^2), however: very low readout rate (50 Hz)

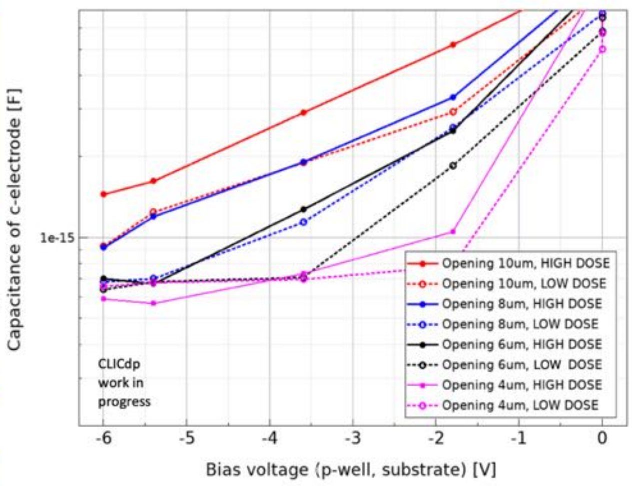
Sensor design optimisation

Impact of different voltages on depletion around collection electrode & potential:



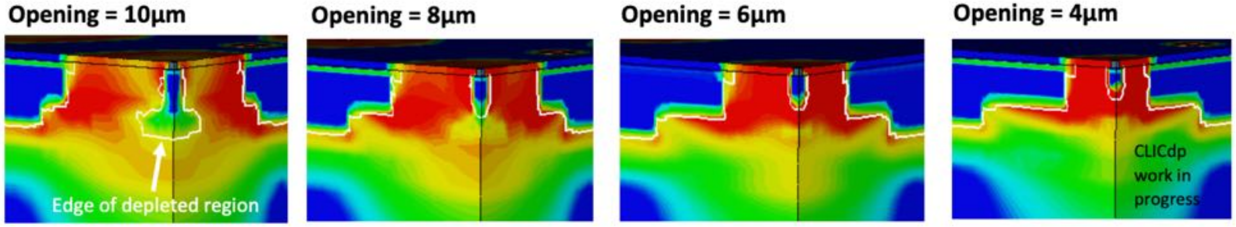
Bias voltage = -1.2 V **Bias voltage = -3 V** **Bias voltage = -4.2 V** **Bias voltage = -6 V**

Capacitance vs. bias voltage for different openings:



CLICdp-Pub-2018-004

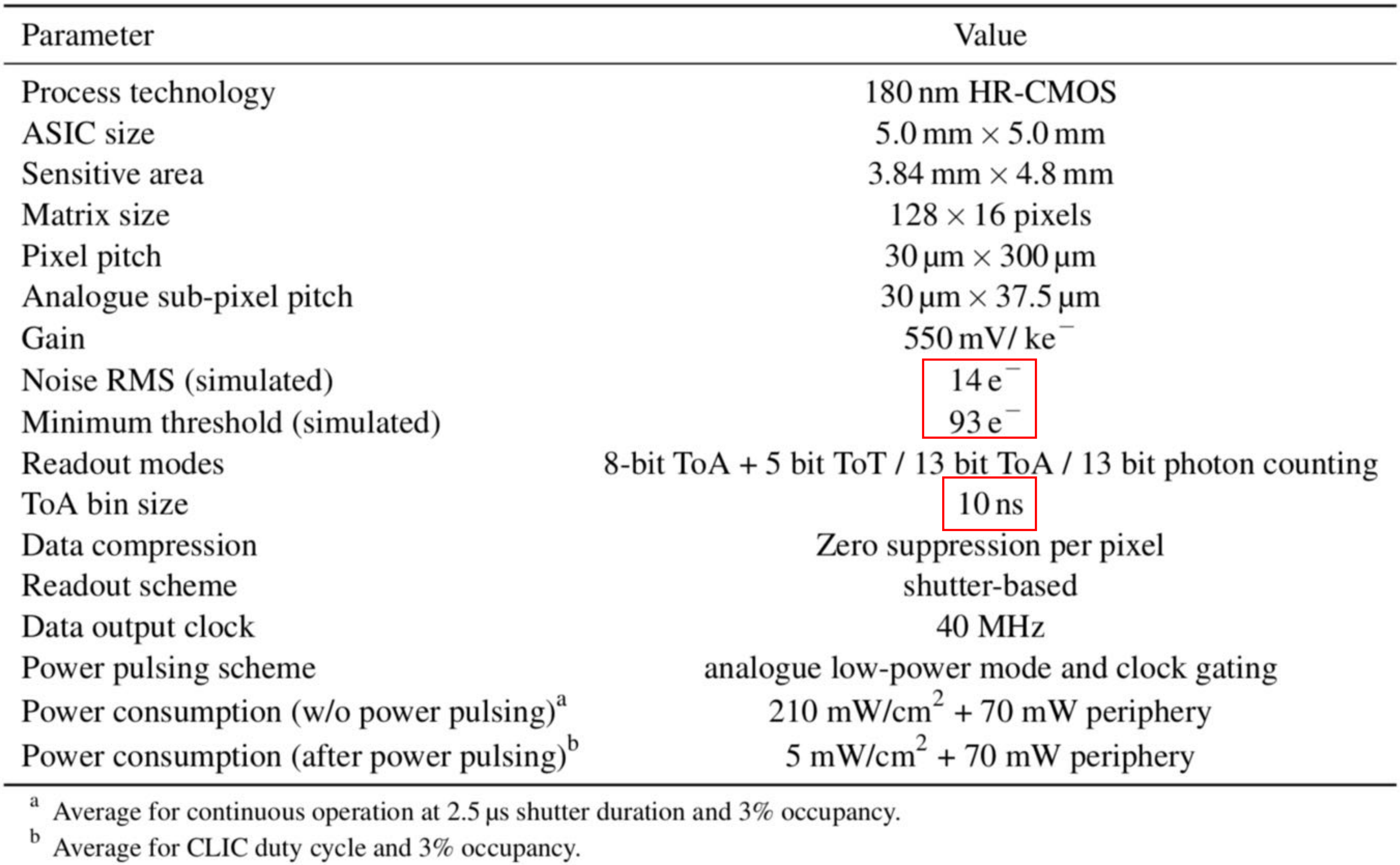
Impact of different p-well openings on depletion around collection electrode & field (-6V):



Opening = 10μm **Opening = 8μm** **Opening = 6μm** **Opening = 4μm**

- Complex depletion and E-field calls for systematic 3D-TCAD optimization of sensor layout, aiming for simultaneously achieving:
  - Full depletion (small capacitance for high S/N)
    → smaller p-well opening
  - Large field (fast charge collection)
    → larger p-well opening
- Solution:
  - Place p-wells as close as necessary to deplete around collection electrode
  - Place deep p-well that shields circuitry as far away from collection electrode as circuitry allows

CLICTD design parameters



Parameter	Value
Process technology	180 nm HR-CMOS
ASIC size	5.0 mm × 5.0 mm
Sensitive area	3.84 mm × 4.8 mm
Matrix size	128 × 16 pixels
Pixel pitch	30 µm × 300 µm
Analogue sub-pixel pitch	30 µm × 37.5 µm
Gain	550 mV/ ke$^-$
Noise RMS (simulated)	14 e$^-$
Minimum threshold (simulated)	93 e$^-$
Readout modes	8-bit ToA + 5 bit ToT / 13 bit ToA / 13 bit photon counting
ToA bin size	10 ns
Data compression	Zero suppression per pixel
Readout scheme	shutter-based
Data output clock	40 MHz
Power pulsing scheme	analogue low-power mode and clock gating
Power consumption (w/o power pulsing)[a]	210 mW/cm^2 + 70 mW periphery
Power consumption (after power pulsing)[b]	5 mW/cm^2 + 70 mW periphery

[a] Average for continuous operation at 2.5 µs shutter duration and 3% occupancy.

[b] Average for CLIC duty cycle and 3% occupancy.