
CERN

# AC-Dipole Limitations and Options for its Upgrade

147th HiLumi WP2 Meeting - 14.05.2019

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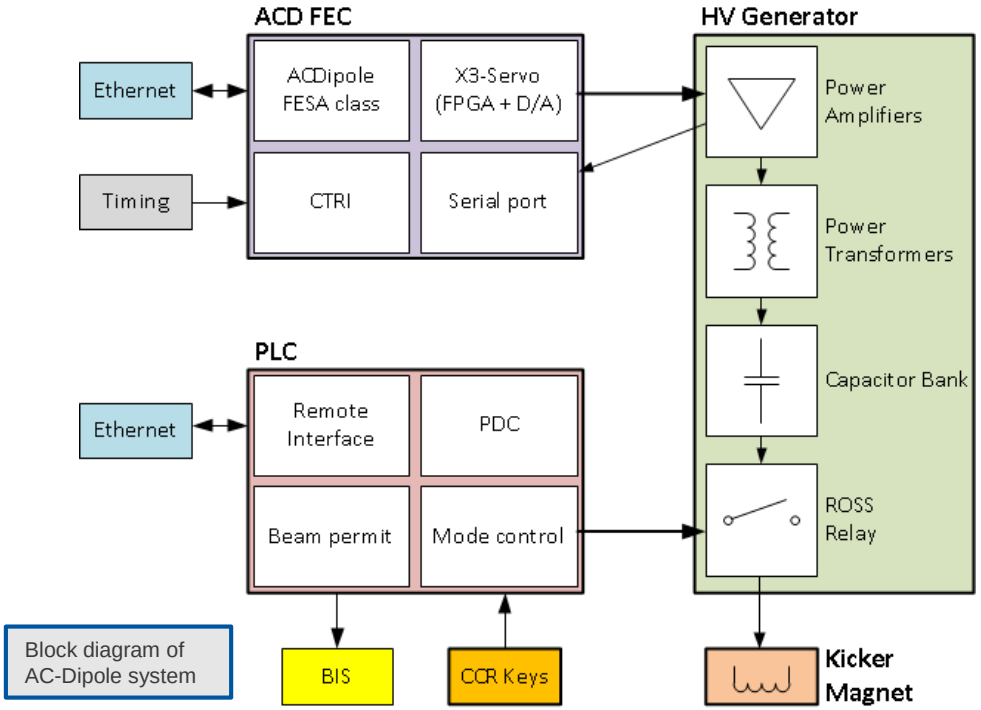
# AC-Dipole Overview




Block diagram of AC-Dipole system

ACD FEC :
- ACDipole FESA class for settings/state control
- Timing event for trigger
- X3-Servo card to generate the waveforms
- Serial port to check power amplifiers configuration

PLC :
- Mode control (CCR keys)
- Beam permit control (BIS)
- ROSS relay control (Closed in AC-Dipole mode only)
- Power distribution control

HV Generator :
- 2x Power Amplifier / Power transformers
- Capa Bank
- Safety ROSS relay

Resonant System: Capa bank / Magnet

# AC-Dipole Overview



Front of Generator:
- 1 FEC (Moved outside generator during LS1)
- 2 Power Amplifiers

Some pictures… (before LS1)

Each MKQAc generator is a combination of 3 generators in 1:
- Tune
- Aperture
- AC-Dipole

Integration could be improved…

# Present Main Parameters

| Parameter | Value | Limitation Element |
|---|---|---|
| Max pulse repetition [s] | 60 | - Power dissipation in transformers |
| Max flat-top length [ms] | 600 | - FPGA card gateware (1s waveform max) |
| Max current [A] | ~1700 | - Power dissipation in transformers / Amplifiers |
| Bandwidth H [Hz] at max I<br>(Software limits, at lower I) | ~3000 – 3300<br>(2700 – 3600) | - Fixed Capa-Bank value: Resonant system centred at ~3150 Hz<br>- Output voltage limit on Amplifiers |
| Bandwidth V [Hz] at max I<br>(Software limits, at lower I) | ~3400 – 3750<br>(3000 – 4000) | - Fixed Capa-Bank value: Resonant system centred at ~3500 Hz<br>- Output voltage limit on Amplifiers |

# Pulse Length Limitation

FPGA Card X3-Servo:

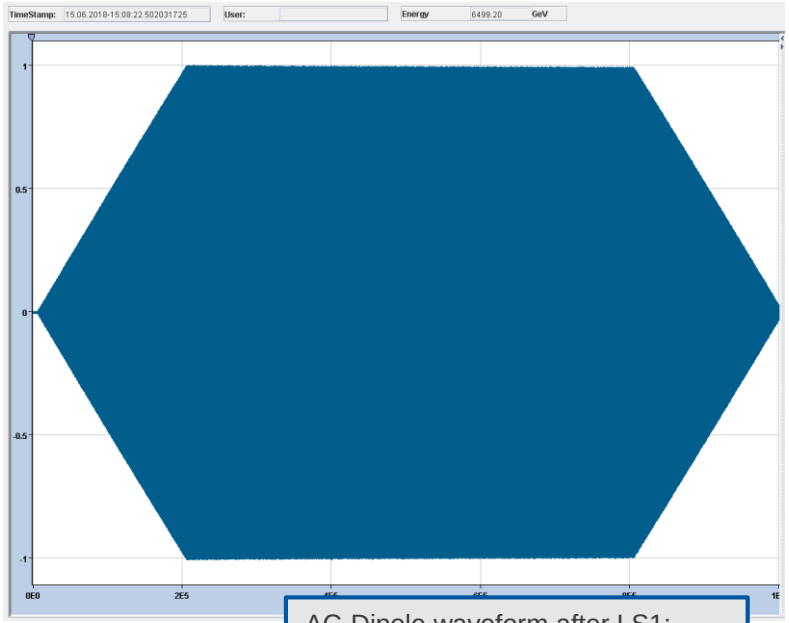
- Max memory = 1Msamples, at 1MS/s

⇒ Max pulse length = 1s

Before LS1, the pulse length was limited in software to 200 ms.

600 ms flat-top is the max pulse length that we can provide now.

X3-Servo XMC card




AC-Dipole waveform after LS1:

- Fixed 200 ms ramp up/down
- Max 600 ms flat-top

# Power Limitation

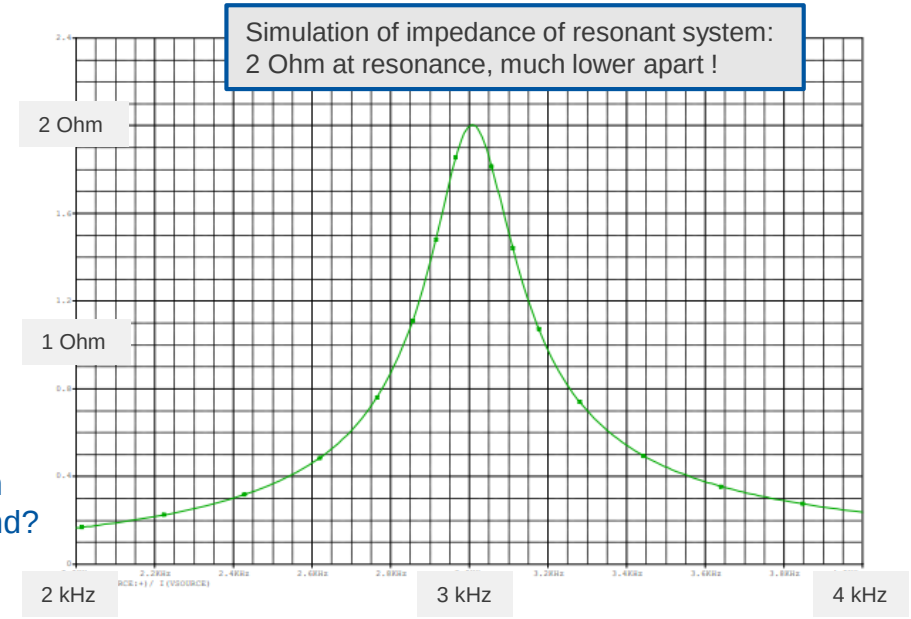
Main limiting elements:

Power amplifiers:
- 2x PowerSoft Digam K20: (Each 18 kW on 4 Ohm)

Power transformers:
- 2x CME transformers: custom design (Each 18 kVA)

Pulse peak current limited by amplifiers:
- Lower performance apart resonance, impedance < 2 Ohm
- Impedance not optimal for amplifier over all frequency band?

Pulse rate limited by transformer:
- 1 pulse every 60s



# Band-Pass Limitation

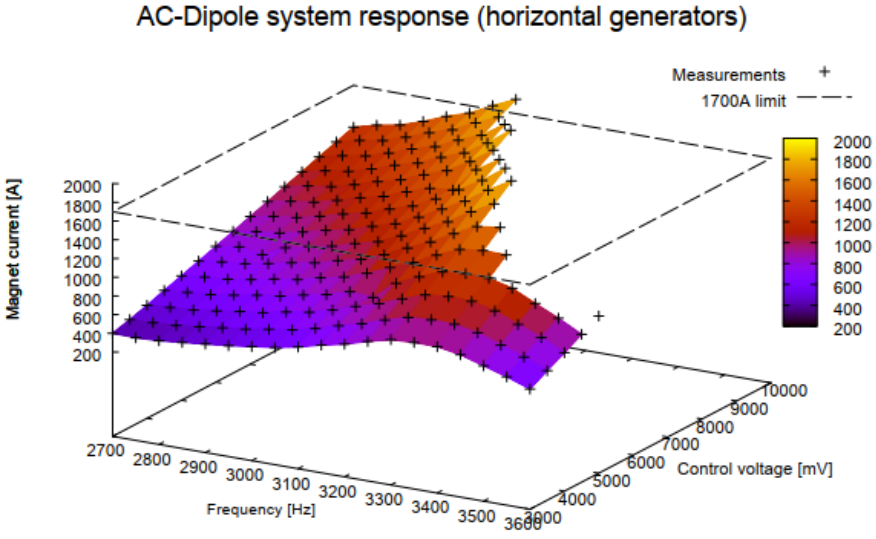
Resonant system:

- Fixed Capa Bank Values

⇒ Fixed center frequencies for H / V

Initial design was to have a variable capa bank,
it was never implemented.

| Kicker Type | Capa Bank [uF] | Center Freq [Hz] |
|---|---|---|
| Horizontal | 722 | 3148 |
| Vertical | 582 | 3485 |




Max current: Voltage / Frequency limit

=> OP max voltage is limited in FESA software using a reference table Vmax(f).

# Many problems seen during operation

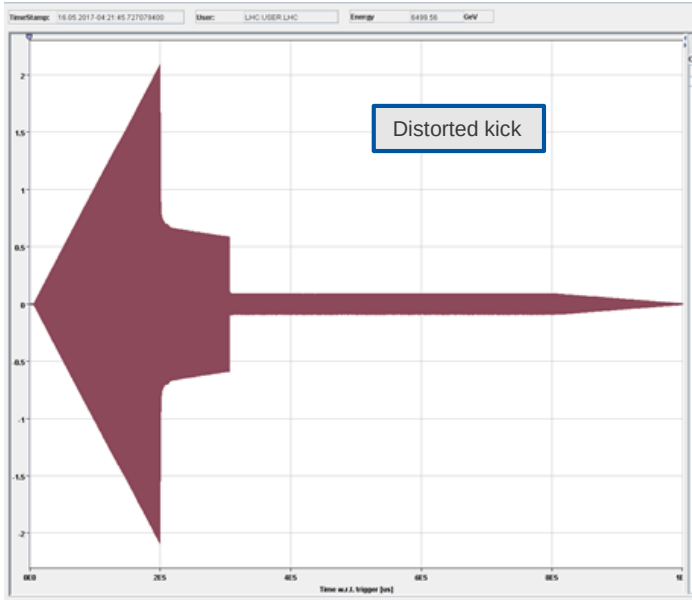
Waveform distorted sometimes:

- Power amplifier thermal protection/compression?
- Many power amplifiers broken!

  *“For large kicks, AC dipole reaches limit of strength before 100%”*

⇒ Is the system pushed at the limit since FT increase from 200 to 600ms ?

⇒ We are blind, difficult to understand problems as we miss diagnosis




PLC / FESA software problems:

- System not turning ON properly, have to send the ON request many times
- Large kick for 0V strength
- System pulsing with previous voltage for 1 kick sometimes (Aperture mode)

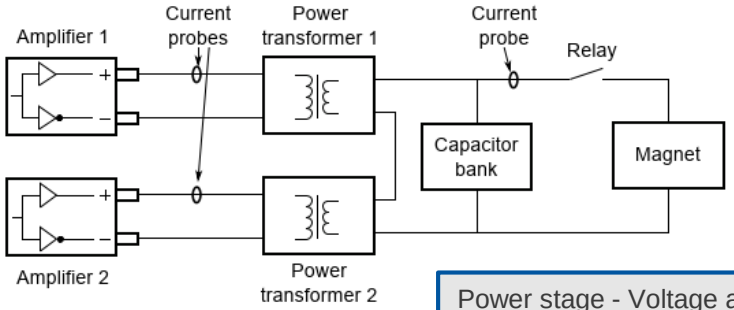
See OMC meeting presentation:
Felix Carlier – 28.08.2018
https://indico.cern.ch/event/750148/

# Missing Diagnosis Tools

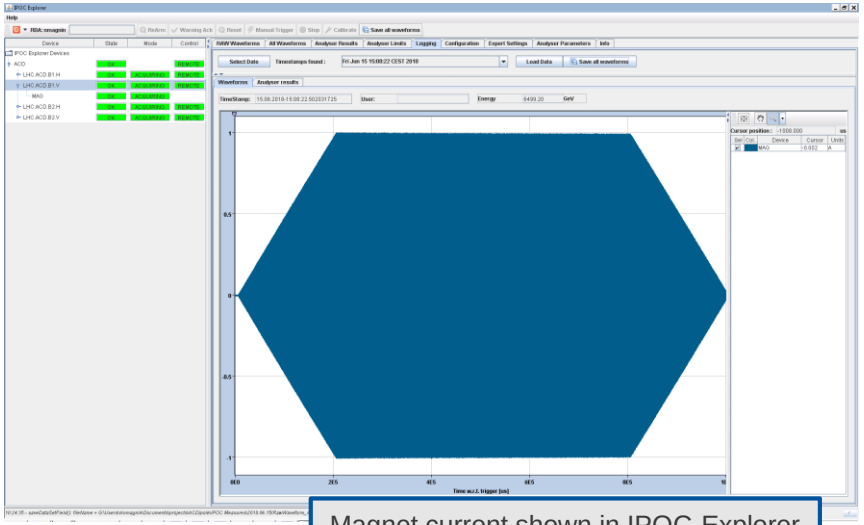
More software diagnosis needed since long time (No hardware development/procurement needed):

- Provide diagnosis for amplifier configuration/faults

- Acquisition of all amplifier voltage/current waveforms for Internal Post Operation Check (IPOC)
  (check current sharing between amplifiers, etc…
  Now IPOC only acquires magnet current)




Power stage - Voltage and Current probes:
Signal acquired by FPGA, but not used by software…



Magnet current shown in IPOC-Explorer

# New Requirements from BE/ABP

| Parameter | Present Value | Requested New Value |
|---|---|---|
| Max pulse repetition [s] | 60 | 10 (30) |
| Max flat-top length [ms] | 600 | 3600 (40’000 turns) (20’000) |
| Max current [A] | 1700 | ~1900 (Increased kick for 7.5TeV operation ?) |
| Bandwidth H [Hz] at max I<br>(Software limits, at lower I) | ~3000 – 3300<br>(2700 – 3600) | Tune: 0.26 - 0.34 (0.5 for MD)<br>=> ~2900 – 5700 |
| Bandwidth V [Hz] at max I<br>(Software limits, at lower I) | ~3450 – 3750<br>(3000 – 4000) | Tune: 0.28 - 0.34 (0.5 for MD)<br>=> ~3100 - 5700 |

~40x more average power dissipated in closed generator without cooling !

- **=> Completely new generator design needed ! (New concept?)**

After discussion with Rogelio, relaxed requirements proposed in red:

- Max length not needed at max power, limit the voltage depending on the length (max power limit)
- Frequency change can be done between MDs, not from pulse to pulse
  (= Access to change capa bank value ? Already possible today, needs procedures)

# Maintenance during LS2

- Migration of all software to new BE/CO version (FESA3 v7/8, Silecs, etc…)
- Generation of a new Linux 64bit driver for X3-Servo FPGA card
- Adaptation of FESA software to new driver

- Correction of bugs seen in operation:
  - State Control problems (ON / OFF / STANDBY commands)
  - Setting Control (Pulse Amplitude/Frequency)
  - Etc…

- Problems with compressed waveforms / Amplifiers broken:
  Revise Max Voltage vs Frequency limits
  - Perform measurements on Test Bench and 4 LHC AC-Dipoles at various frequencies/amplitudes
  - Redefine limit reference tables, more conservative to increase availability

# Upgrade: Suggested Work Package 1

Software upgrade:

- Software development for diagnosis improvement
  - Provides diagnosis for amplifier configuration/faults
  - Acquisition of all amplifier output voltage/current waveforms for IPOC (check current sharing between amplifiers, etc…)
- Validation on test bench
- Installation & Commissioning

| | |
|---|---|
| Manpower | 0.5 FTE (missing) |
| Budget | - |

# Upgrade: Suggested Work Package 2

Software & Gateware & Hardware upgrade:

- New FPGA gateware development:
  - Pulse length / rate limits increased, power is the limit.
  - Improve fault detection based on amplifier output voltage/current measure
- New FPGA hardware (X3-Servo probably obsolete)
- New Linux 64bit drivers, adaptation of FESA Software
- Validation on test bench
- Installation & Commissioning

| | |
|---|---|
| Manpower | 0.5 FTE (missing) |
| Budget | 50 kCHF |

# Upgrade: Suggested Work Package 3

New AC-Dipole power generator design:

- New power circuit, variable capa bank(?), cooling(?), etc… tbd
  - Max pulse length + max pulse rate + max current
- Production of prototype and validation on test bench
- Production of 4 generators & spare
- Installation & Commissioning

| | |
|---|---|
| Manpower | 2 FTE (missing) |
| Budget | 350 kCHF (1 prototype + 5 production) |

We would need a pre-study for more accurate estimate, based on final new functional specification

# Summary

- Problems seen in operation during LHC run 2 should be fixed after LS2
- OP limits probably lowered after LS2 to increase availability
- AC-Dipole performances are limited, BE/ABP has new requests for HL-LHC
- We need a new AC-Dipole specification from ABP.
- This upgrade can be split into small work units and staged
- Missing resources (P+M) to work on this system

# Spare slides

# Variable Capa Bank