Class 0 Power Converters
Update on ADC development and testing

Nikolai Beev

High Precision Measurements Section
Electrical Power Converters Group
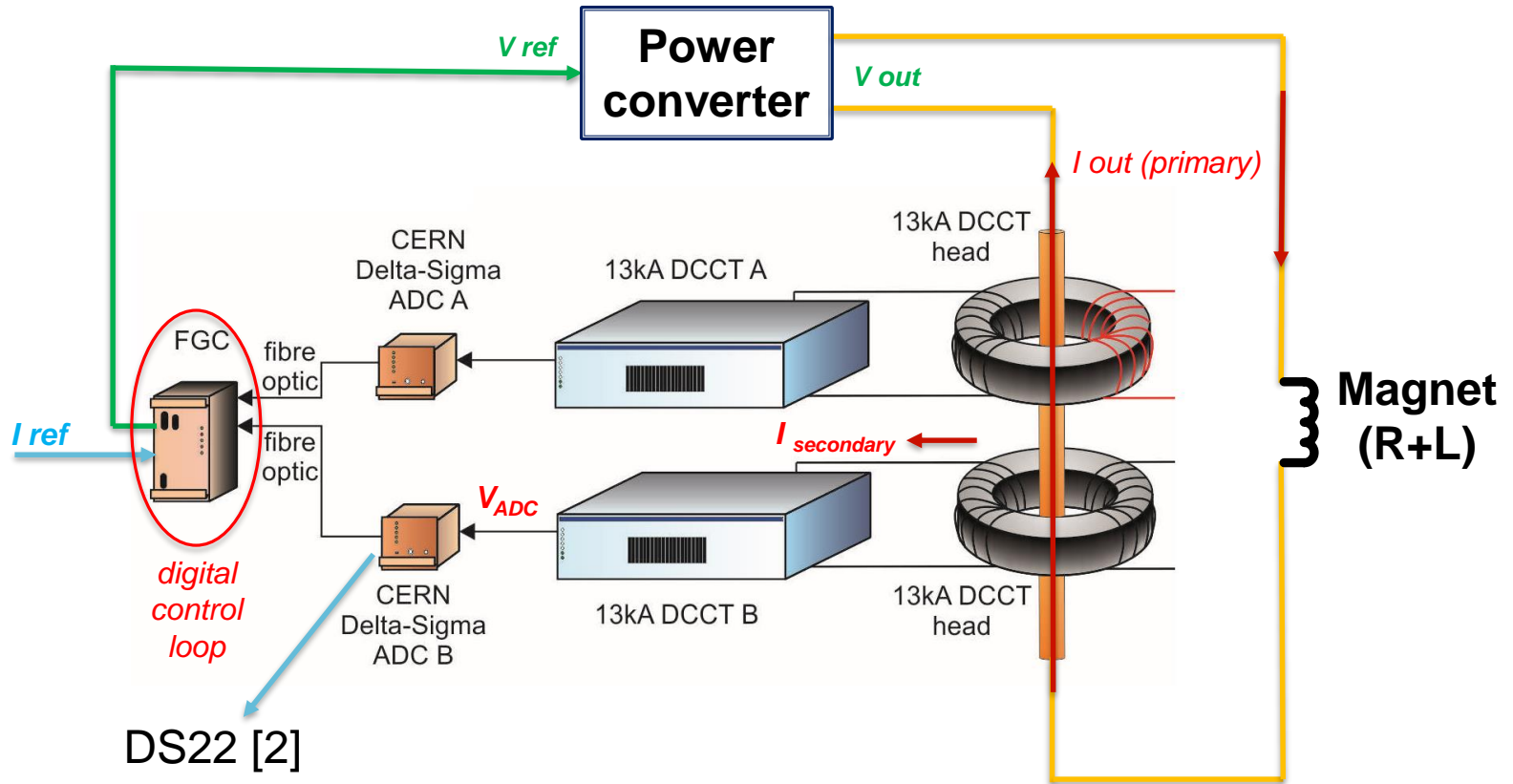Technology Department

HL-LHC TCC meeting

18.04.2019

Presentation Outline

- **Significance of the ADC**

- **HL-LHC Class 0 Requirements**

- **ADC strategy: DS24 and HPM7177**

- **Preliminary test results**

- **Conclusions**

# LHC High Precision Measurement System

[1] M. C. Bastos *et al.* "High accuracy current measurement in the main power converters of the large hadron collider: tutorial 53," in *IEEE Instrumentation & Measurement Magazine*, vol. 17, no. 1, pp. 66-73 (2014)

[2] J. Pett. A high accuracy 22 bit sigma-delta converter for digital regulation of super-conducting magnet currents. *Third International Conference on Advanced A/D and D/A Conversion Techniques and their Applications*, pp. 46 – 49 (1999)
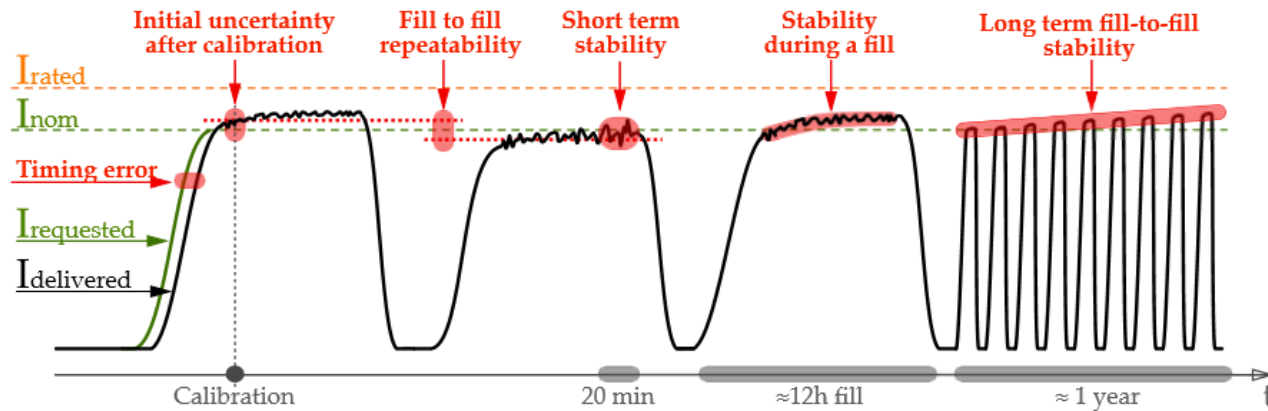
Current Regulation: Closed loop performance
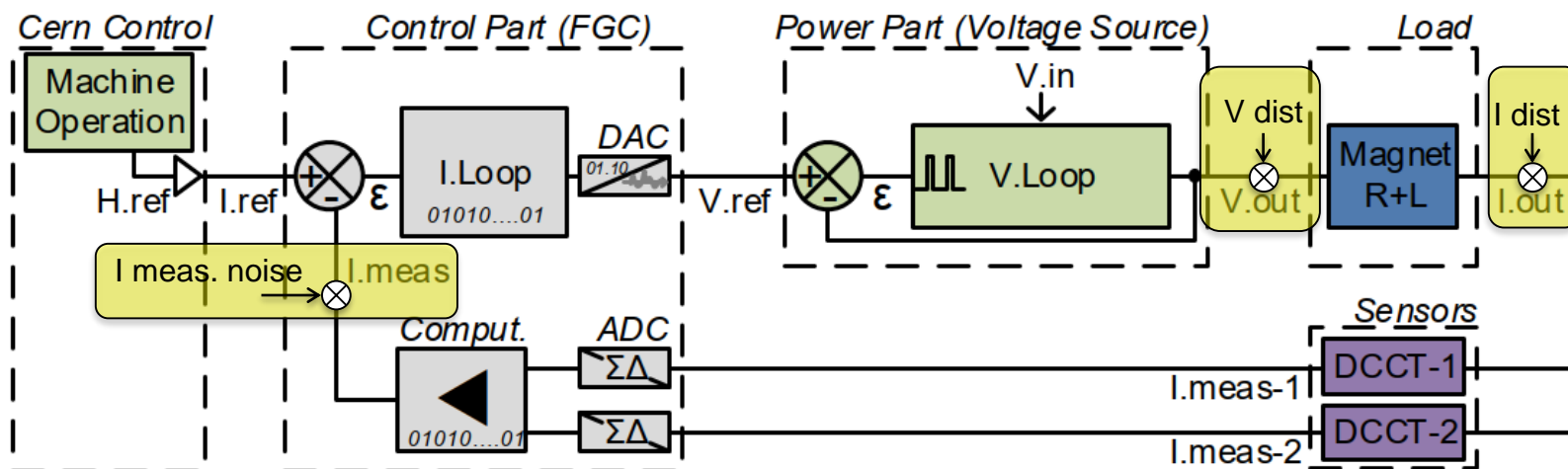
RPTE.UA83.RB.A78 – LHC 13 kA
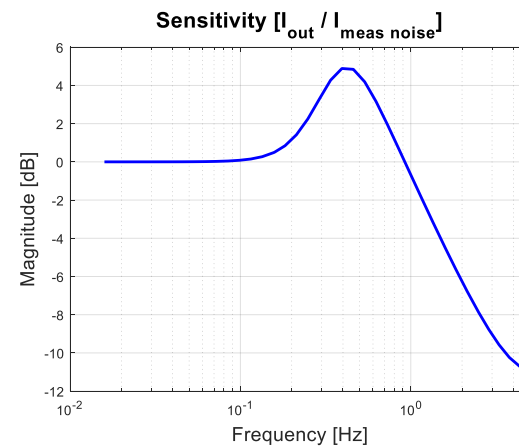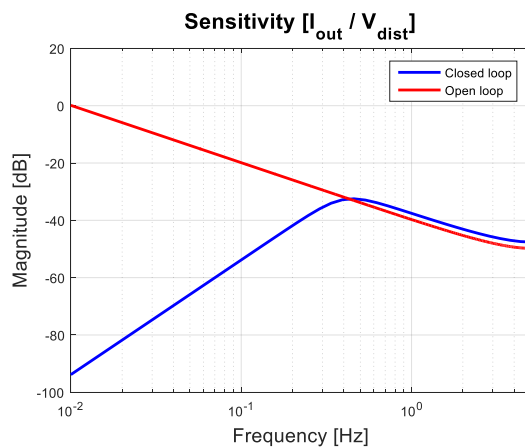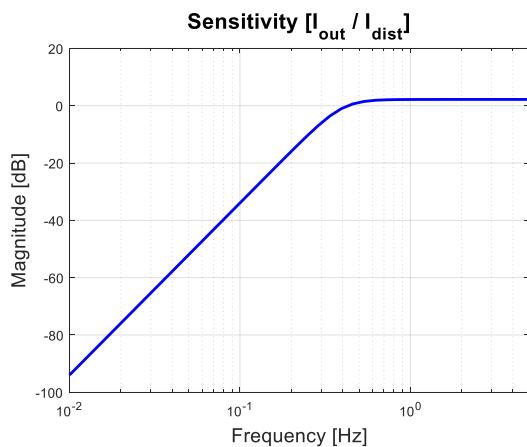
HL-LHC Class 0 Requirements

	Class 0	
	total PC	**adc**
Resolution [ppm]	0.5	0.2
Initial uncertainty after cal [2xrms ppm]	2.0	1.0
Linearity [ppm] [max abs ppm]	2.0	1.0
Stability during a fill (12h) [max abs ppm]	**0.7**	**0.3**
Short term stability (20min) [2xrms ppm]	**0.2**	**0.1**
Noise (<500Hz) [2xrms ppm]	**3.0**	**1.0**
Fill to fill repeatability [2xrms ppm]	**0.4**	**0.1**
Long term fill to fill stability [max abs ppm]	8.0	4.0
Temperature coefficient [max abs ppm/C]	**1.0**	**0.2**

T = const.

$\Delta T = 0.5\ ^\circ C$

[3] M. C. Bastos. HL-LHC Power Converter Requirements. EDMS 2048827 v.2

DS22

- Designed at CERN in the 1990s [2]
- 3rd order Sigma-Delta ADC built of discrete components
- Temperature-stabilized with a Peltier element
- Improved gradually over the years
- Version 10.1 (2006) installed in LHC: Class 1 – main bends, main quads, inner triplets
- Excellent reliability record so far

- Not compliant with HL-LHC Class 0 requirements for noise (LF and broadband) and fill stability
- Contains obsolete components
- Has known and recurring problems (e.g. idle tones)

ADC strategy for HL-LHC Class 0

- **DS24** – an improved version of DS22
  - replacement of obsolete components
  - improvements in LF and broadband noise
  - mitigation of the idle tones with a different dithering scheme
  - improvements in the digital low-pass filter
  - new documentation - schematics and layouts in Altium Designer; new 3D models and mechanical drawings

- **HPM7177** - a brand new digitizer based on a commercial ADC chip

DS24

- DS22 was studied in detail in the past 2 years to identify possible improvements

- **EDMS 2054292 V1** [4] summarizes all changes from DS22 V10.1 to DS24

- Expected performance improvements:
  - significant decrease of LF noise
  - slight decrease of broadband noise
  - significant reduction or elimination of idle tones

- Design documentation:
  - EDA-03978 – ADC module
  - EDA-03979 – Modulator
  - EDA-03980 – Power supply
  - EDA-03981 – Shielding PCB
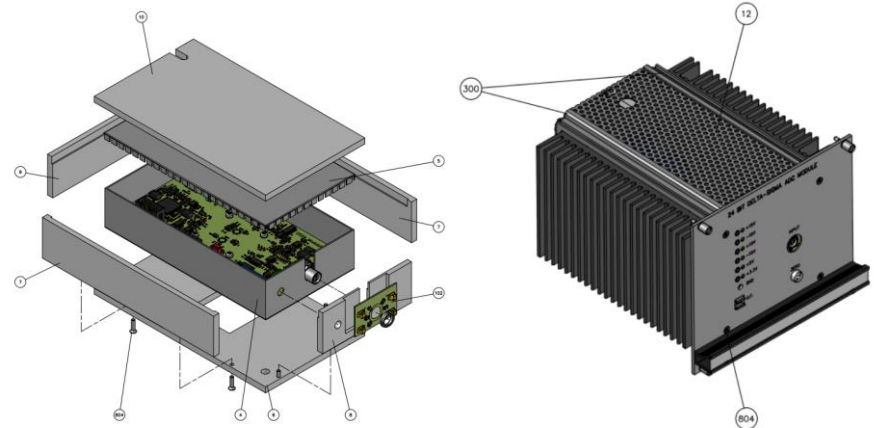
DS24 Low-frequency Noise
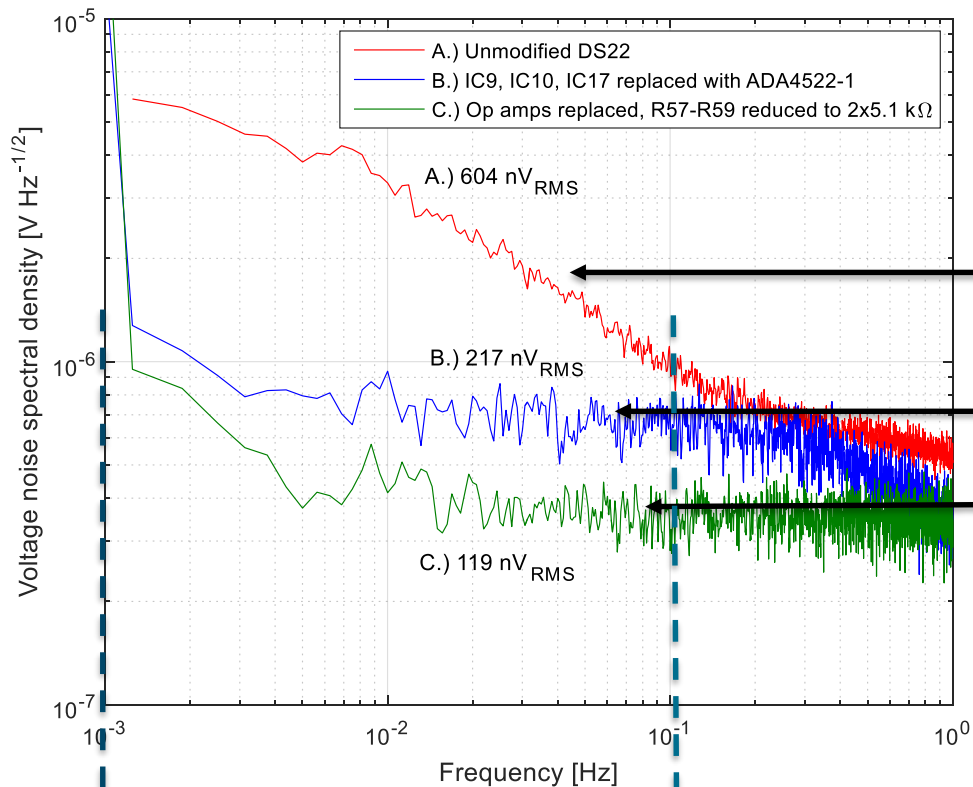
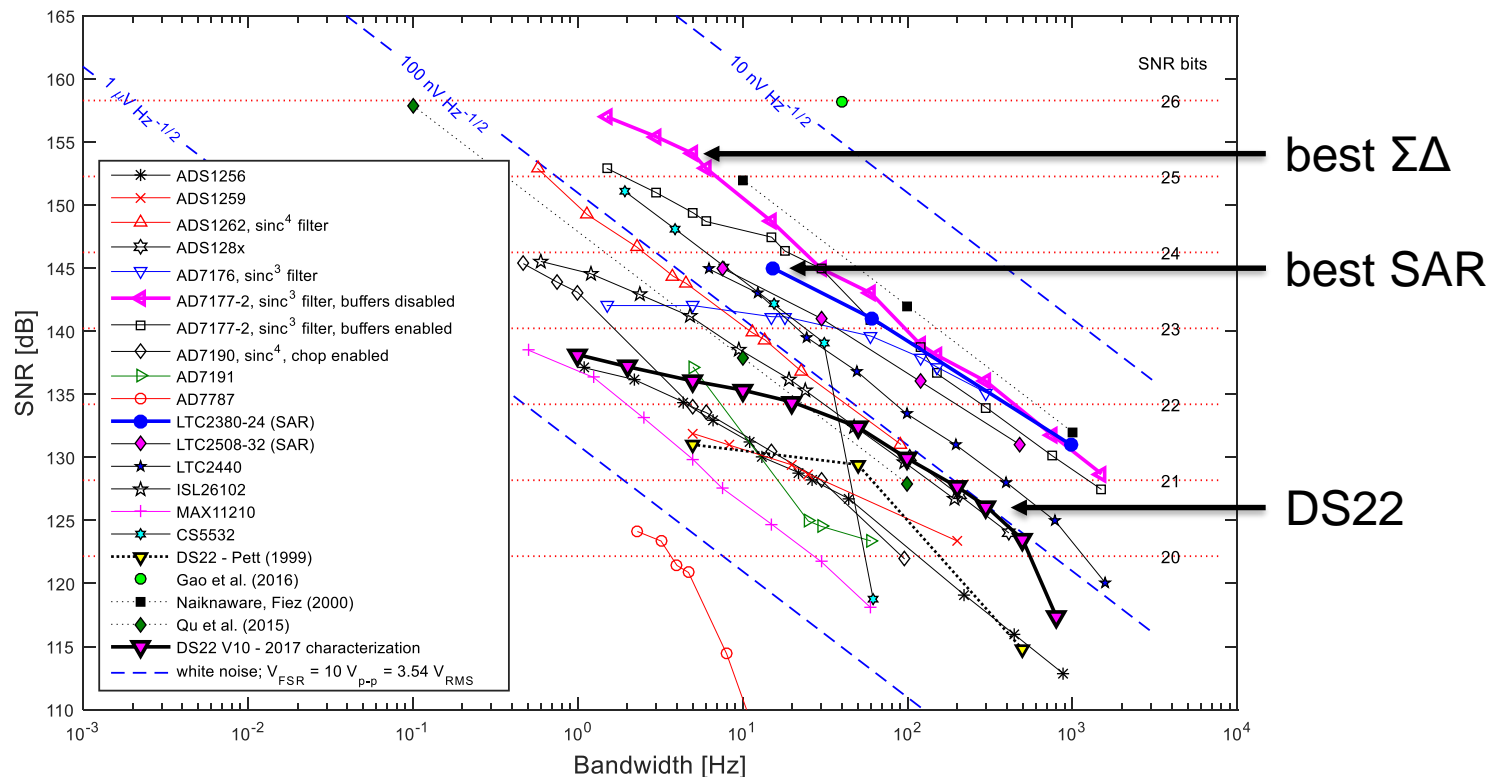# Commercial ADC Survey and Pre-selection

- Commercial ADCs with nominal resolution ≥24 bits were considered
- Datasheet information (noise, SNR, effective resolution) was carefully studied and scaled for a fair comparison. Results were reported in [5]


[5] N. Beev. Analog-to-digital conversion beyond 20 bits. Proceedings of I2MTC-2018, Houston, TX (2018)

Commercial ADC testing - LF noise

- A test bench based on a NI PXIe FPGA system was developed
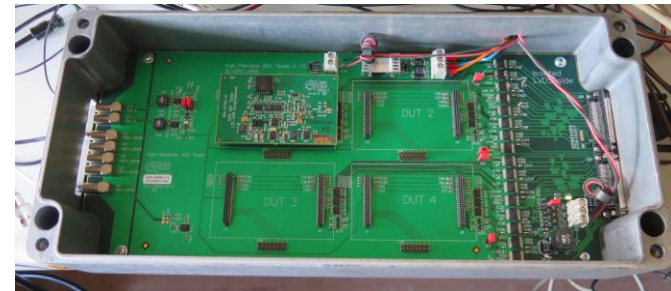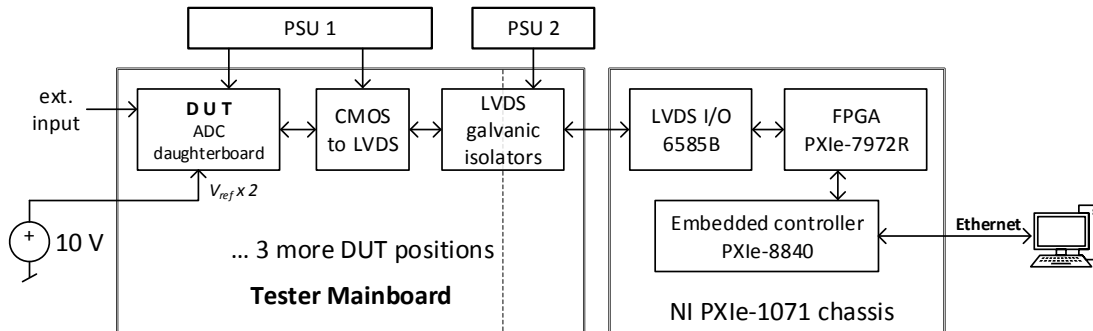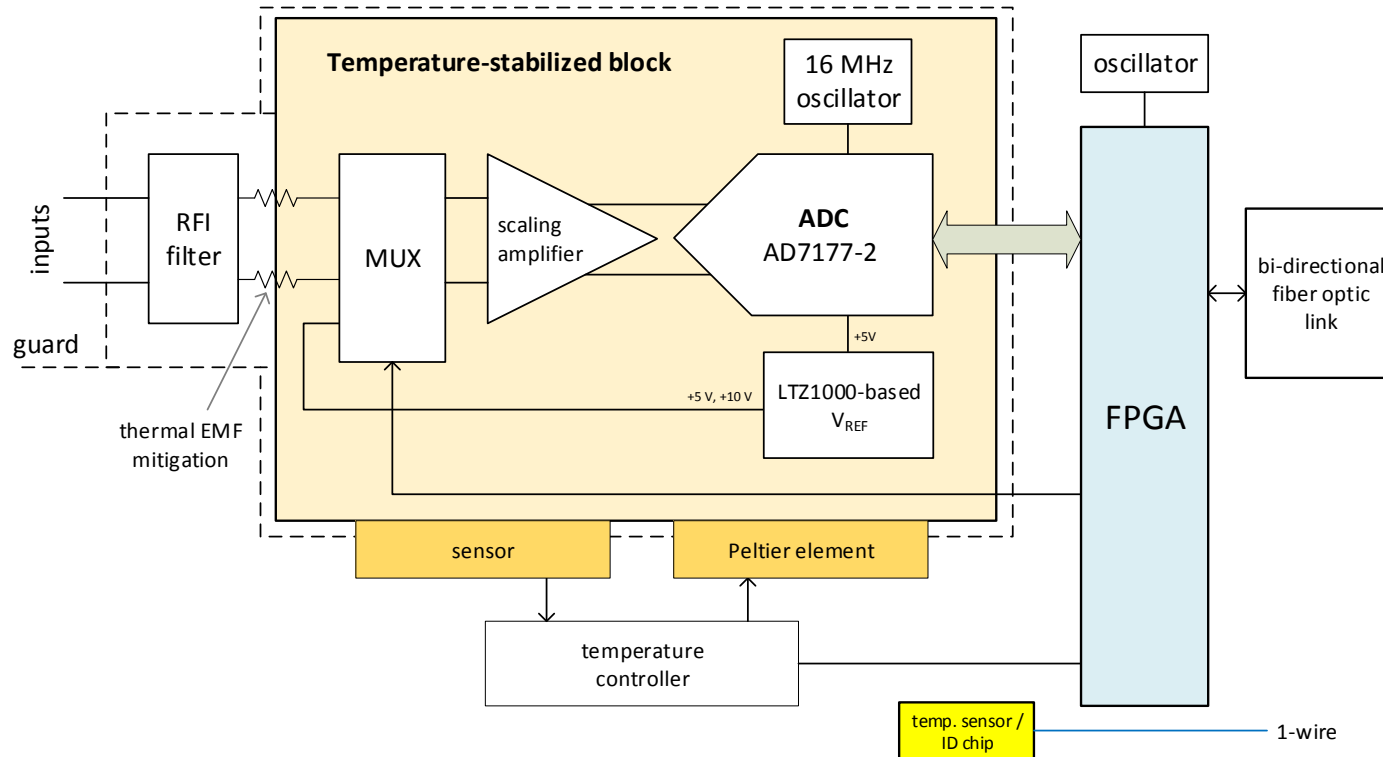

- Tested devices: **LTC2380-24**, **AD7177-2,** LTC2378-20, AD7176-2
- Identical measurement conditions: shorted inputs, 20-minute acquisition buffer, FFT averaging (Welch method with Hanning window, no overlap)
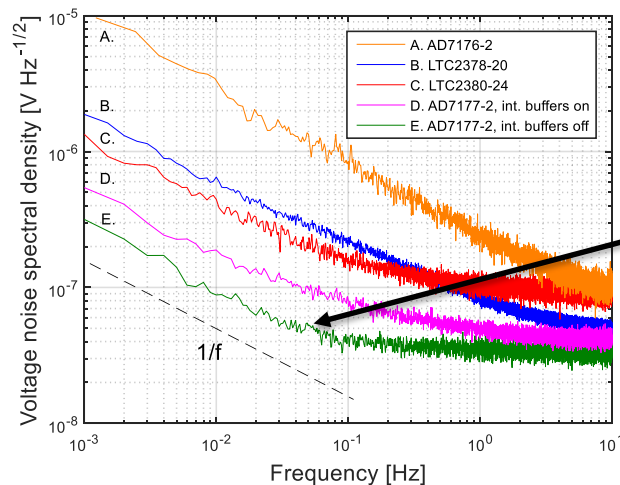
AD7177-2 is the clear winner

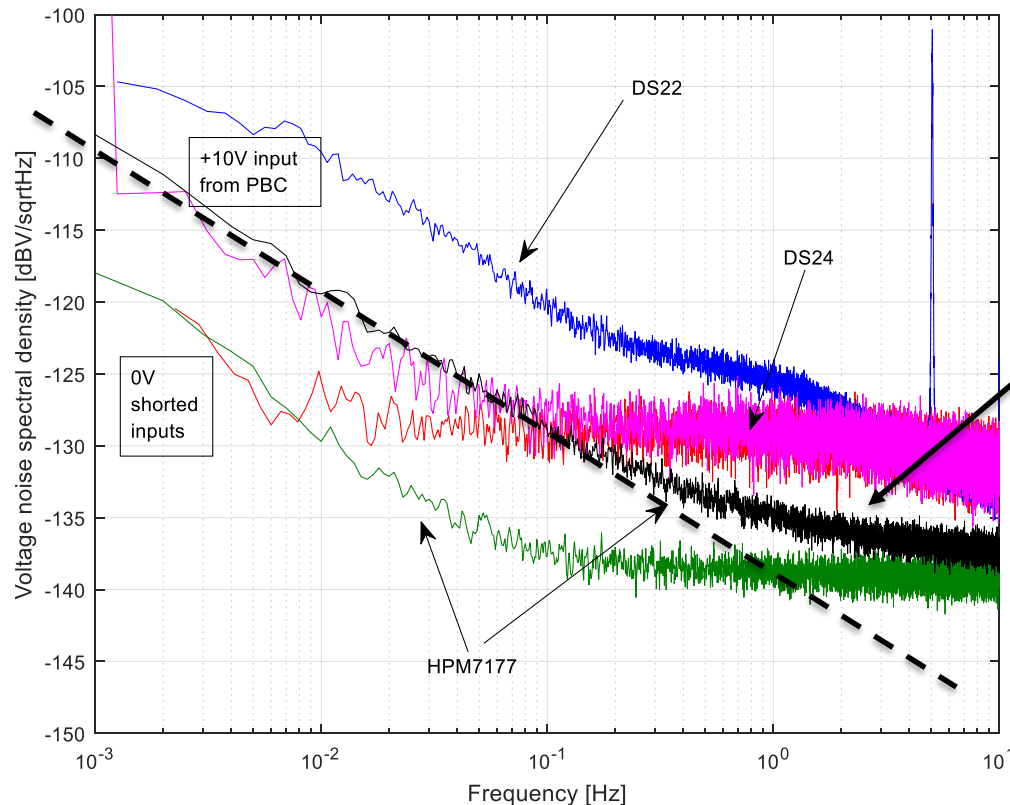- 32 nV Hz$^{-1/2}$ white noise
- 15 nV$_{RMS}$/decade 1/f noise
- $f_{corner} \approx 0.05$ Hz

- reproducible between devices

HPM7177 digitizer architecture

[6]   HPM7177 Open Hardware project
https://www.ohwr.org/project/opt-adc-10k-32b-1cha/wikis/wiki

DS24 and HPM7177 – Low-frequency noise

HPM7177 has advantage over DS24 above 0.1 Hz, particularly up to 10-20 Hz

At +10 V (full scale) both ADCs are limited by the voltage reference (LTZ1000) 1/f noise below 0.1 Hz

Safely within the HL-LHC specs

DS24 and HPM7177 – Broadband noise

- DS24 is expected to be slightly better than DS22 (≈20%)
- HPM7177 has yet lower broadband noise than DS24 up to 500 Hz (≈25% lower)
- A new digital filter for DS24 will make a big difference for reducing the aliased noise after decimation
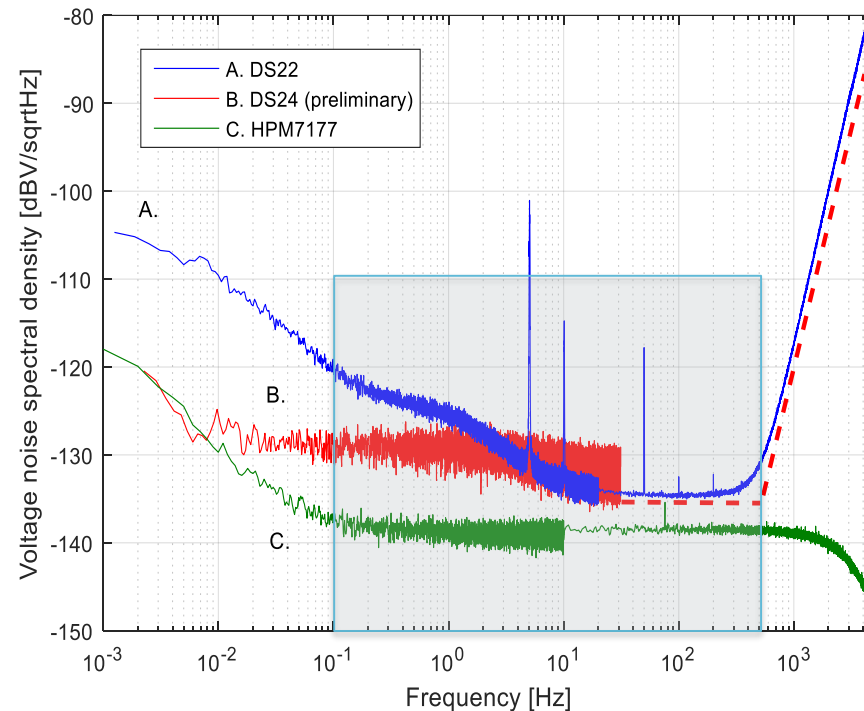
DS22 and HPM7177 - Linearity

- DS24 is expected to be the same as DS22
- LUT-based linearization could be implemented in HPM7177 to improve the figure
- In both ADCs, linearity is safely within the specs

DS22
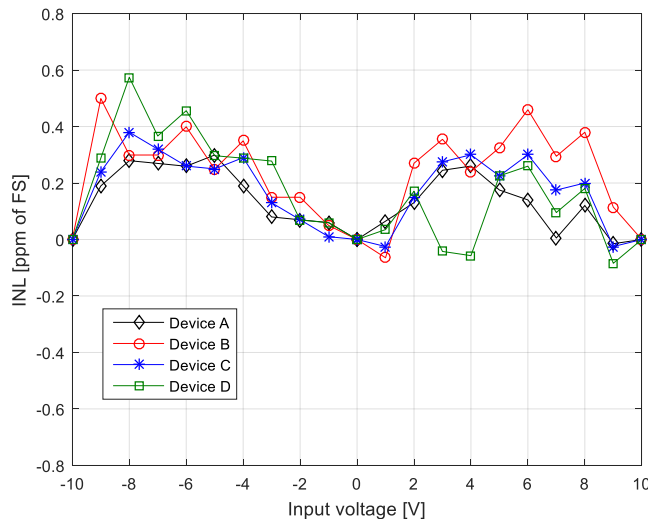
HPM7177 (prototype)

DS24 vs HPM7177 - Summary

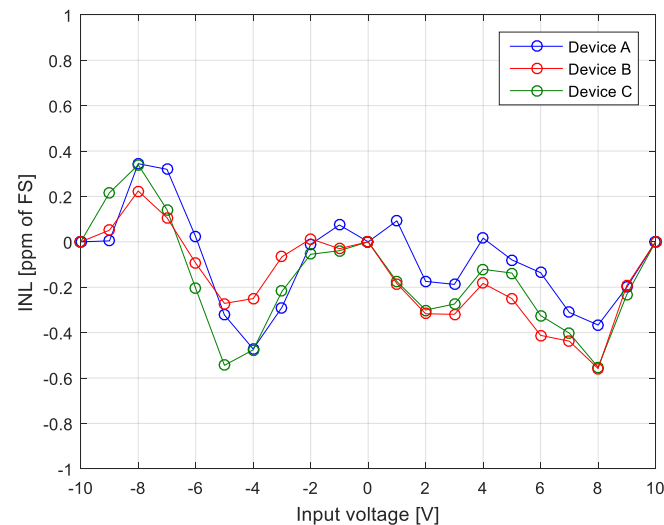| Specification	Conditions	Unit	HL-LHC Class 0 requirement	DS24	HPM7177
Noise	0.1 – 500 Hz	ppm (rms)	0.5	> 0.4	0.3
Short-term stability	1 – 100 mHz	ppm (rms)	0.05	< 0.025	< 0.025
Fill stability	23 µHz to 10 mHz	ppm (p-p)	0.3	≈ 0.2	≈ 0.2
Linearity	3-point method -FS to 0; 0 to +FS	ppm	1	0.5	0.6 (<0.3 with digital correction)
Temperature coefficient	T_{amb} = 20°C to 40°C	ppm/°C	0.2	< 0.2	< 0.05

LTZ1000 -limited

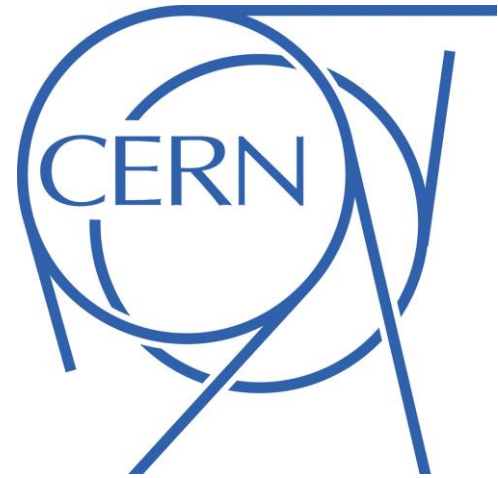|	DS24	HPM7177
Optical interface	Unidirectional out: bitstream	Bi-directional in: synchronization out: serial data
Built-in calibration capabilities	No	Yes
Inputs	Fully differential with floating GND	Single-ended with floating GND
Compatibility	FGC 2, FGC 3.2	FGC 3.2

Status and planning

- DS24 is currently in production
  - ➢ 3 prototypes will be available in mid-2019
  - ➢ performance testing will finish by the end of 2019

- HPM7177 is currently in the final design stages
  - ➢ documentation is under preparation at the CERN Design Bureau, will be ready in mid-2019
  - ➢ 3 prototypes will be produced by the end of 2019
  - ➢ performance testing in early 2020

- HPM7177 characterization against a Josephson Junction array – external collaboration with PTB - Braunschweig planned for 2020

- Decision on which ADC to use – mid 2020
- Pre-series production of 22 units for IT String – January 2021
- Series production of 89 units for HL-LHC – January 2024

Conclusions

- The ADC plays an important role in the measurement chain and ultimately in the quality of the current delivered to the magnets

- Higher performance in the ADC is desirable, as it relaxes the requirements for the DCCT

- We have two feasible ADC candidates for HL-LHC Class 0

- Commercial integrated high-resolution ADCs have improved significantly over the years, but the discrete-component solution is still competitive

- At very low frequencies (<0.1 Hz), both DS24 and HPM7177 will be limited by the LTZ1000 voltage reference

References

[1] M. C. Bastos *et al.*, "High accuracy current measurement in the main power converters of the large hadron collider: tutorial 53," in *IEEE Instrumentation & Measurement Magazine*, vol. 17, no. 1, pp. 66-73 (2014)

[2] J. Pett. A high accuracy 22 bit sigma-delta converter for digital regulation of super-conducting magnet currents. Third International Conference on Advanced A/D and D/A Conversion Techniques and their Applications, pp. 46 – 49 (1999)

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[4] N. Beev. DS24 Design Proposal. EDMS 2054292 V1

[5] N. Beev. Analog-to-digital conversion beyond 20 bits. Proceedings of I2MTC-2018. Houston, TX (2018)

[6] HPM7177 Open Hardware project
https://www.ohwr.org/project/opt-adc-10k-32b-1cha/wikis/wiki

Thank you!