SAMPA & SRS integration

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Tips to be Covered

- Introduction
- Objective Top view
- Related Works
- Challenges
- Partial results
- Next steps

Introduction

SAMPA chip

- A 32 input channels ASIC, made in CMOS 130nm technology.
- Digital signal processor - pedestal removal, baseline ship corrections, zero-suppression, …
- Data transmission: up to 11 activable e-link at 320 Mbps
- Specific data communication protocol

SRS system

- A complete Scalable Readout System
- The DATE Online system
- The Scalable Readout Unit (SRU)
- Programmable Front End Cards (FECs)

Introduction

- The SRS organization for new developments

Common to all projects

Specific development to each “new compatible chip”

A.) **Common system components of SRS**:

- The DATE Online system of the ALICE LHC experiment, stable and user friendly: its use by RD51 is based on a MoU with the ALICE DATE team
- 10 Gigabit Ethernet as commercial, very high performance standard for readout links, based on copper or fibre.
- The Scalable Readout Unit (SRU) as a 40-fold DTC link concentrator between the frontend system and the 10Gigabit port of DATE (not needed for small systems)
- Programmable Front End Cards (FECs) that fit in a cheap, mechanical framework (6U x 220 Euro-card) with PCIe connectors to interface adapter cards
- DTC link cables (CAT6) for transferring Data Trigger and Control between the FECs and the SRU
- A user-programmable trigger and clock interface based on LVDS and NIM logic on both SRU and FEC cards .
- TTC fibre interface on the SRU for trigger and timing distribution in LHC experiments

B.) **Shareable components for classes of chips (analogue , digital, etc):**

- SRS adapter cards to interface different types of chips (analogue, digital, mixed) to the FEC card.
- Chip readout links (cables, fibres) for distances of tens of meters between the FEC crate and the hybrids on the detector

C.) **Detector specific components:**

- Chip hybrids with standard connectors (example: HDMI) on the detector and on the readout side, allowing the user to choose the most suited readout chip
- Application-specific adapter cards in A, B or C format for user-defined purposes like diode bias control etc.

Our targets here !

Introduction

- Compatible external chips matrix

Linear Chips

New ▾ Actions ▾ Settings ▾

Chip Name	Experiment	Detectors	#channels
APV25	CMS	silicon microstrip detectors CMS	128
AFTER	T2K TPC	TPC	72
MSGCROC	DETNI	Position Sensitive Microstrip Gas Chambers for Thermal Neutrons (DETNI)	32
Beetle	LHCb	Si strip, MAPMT	128
VFAT	TOTEM		128
NINO	ALICE	TOF	8
CARIOCA	LHCb	muon MWPC	8
MiMac		MIcro-tpc Matrix of Chambers (GEMs, Micromegas)	16
PASA+ALTRO	ALICE	TPC	16

For assistance with Access Web Datasheet, see Help.

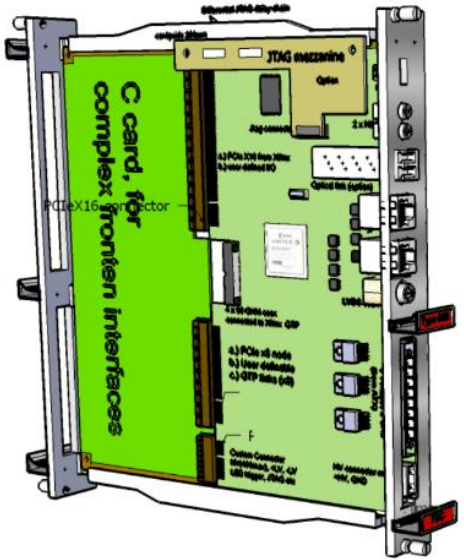
Pixel Chips

New ▾ Actions ▾ Settings ▾

Chip Name	#ch	Pixel Area (um x um)	Noise	Modes
MEDIPIX-2	256x256	55x55	100e-	ph-counting
MEDIPIX-3	256x256	55x55	72e-	ph-counting/tim

SRS system

- The FEC board: Used as first step to interface external chips



- One FPGA Virtex 6
- A optional C card
- Cables to interfacing
- Direct connection to a PC or SRU unit

Introduction

- Compatible external chips

Example: The Pixel chip

Linear Chips

New Actions Settings

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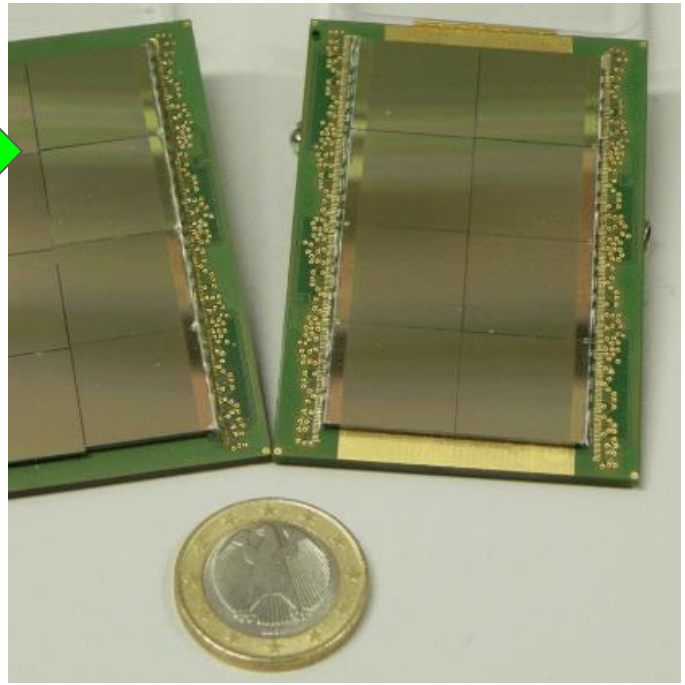
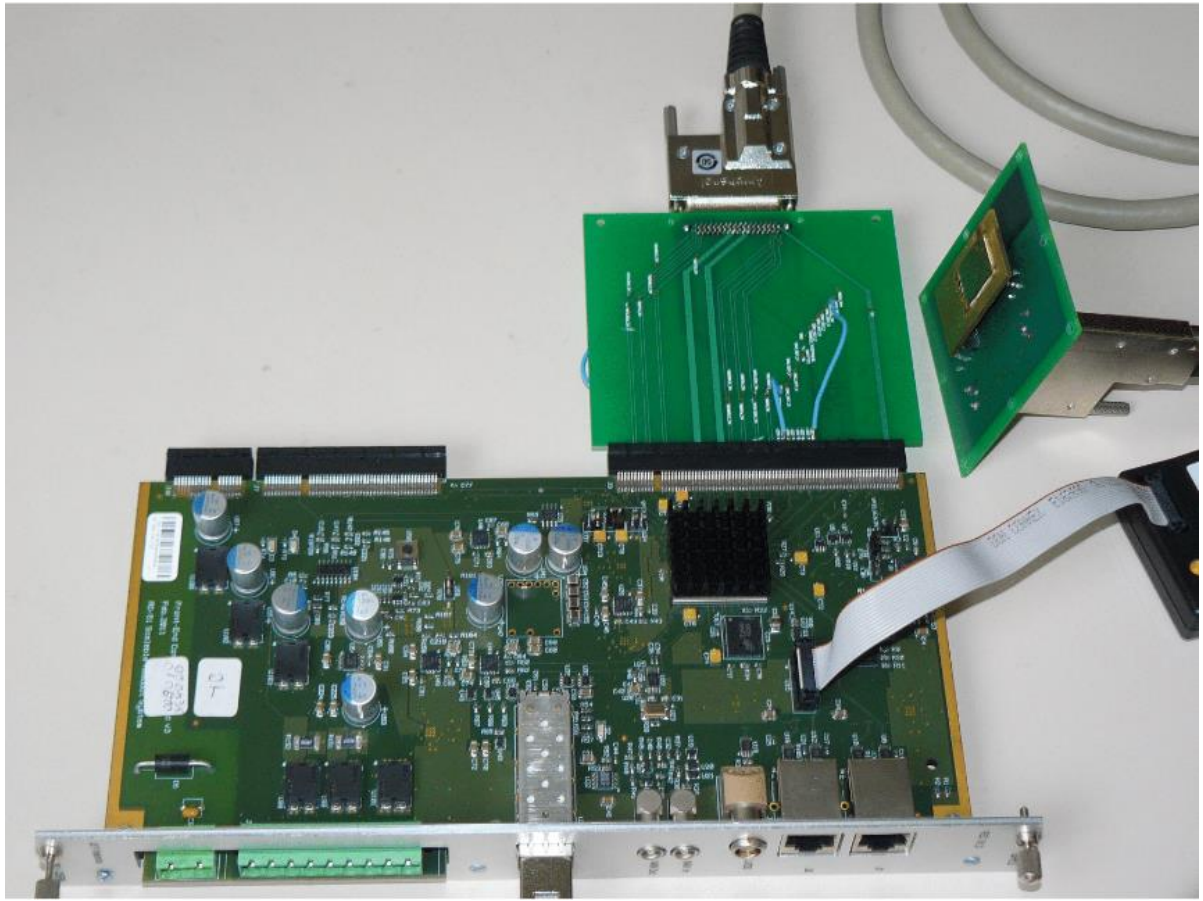


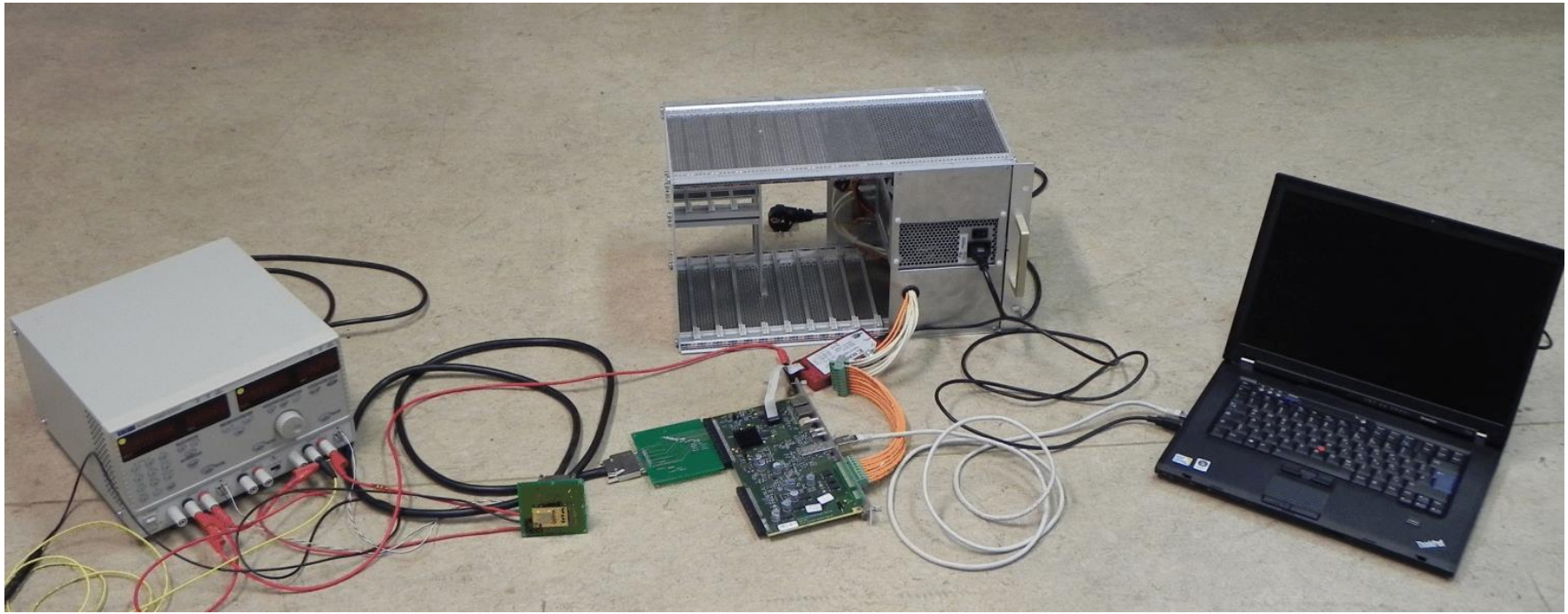
Introduction

- **Example:** The Pixel chip and SRS integration
- One FEC card
- One Adapter card
- One Pixel chip
- Cables



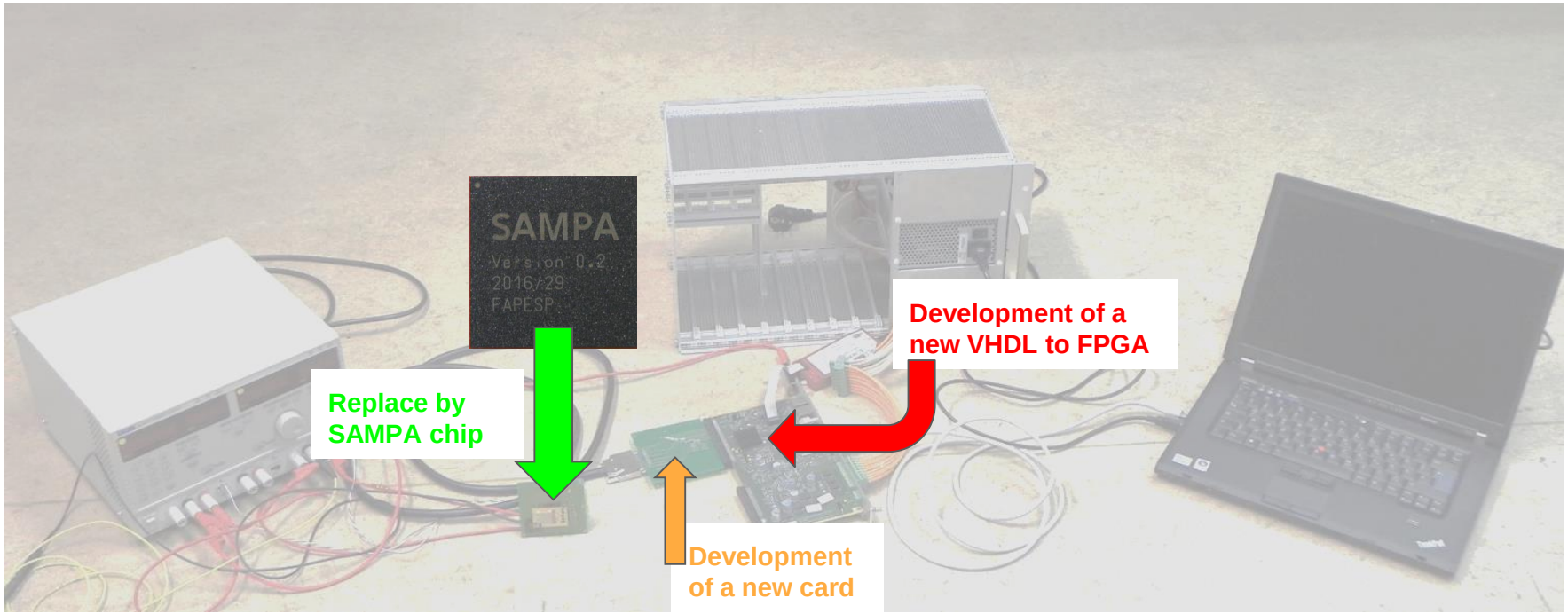
Introduction

- **Example:** The Pixel chip and SRS integration - complete system



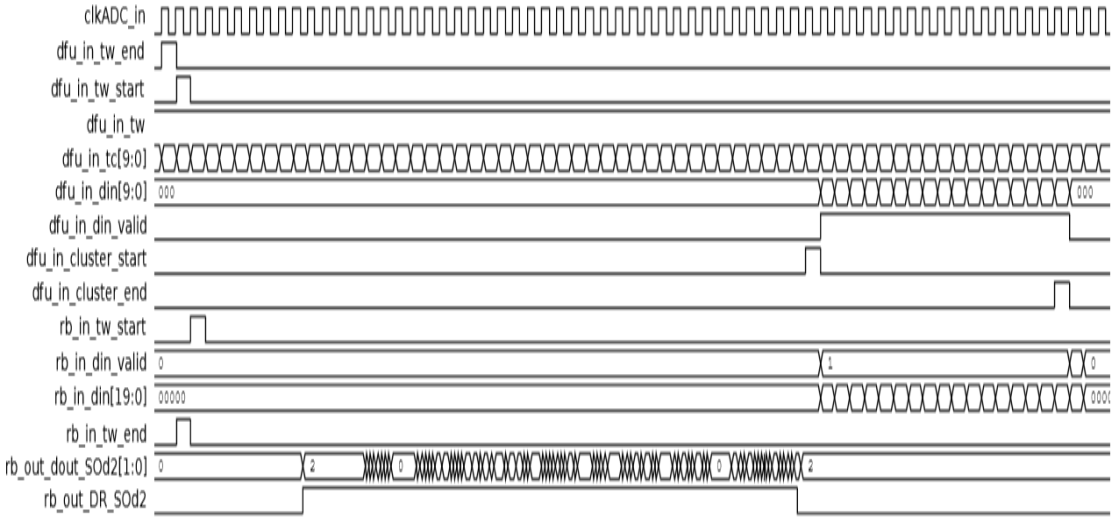
Objective (Top view)

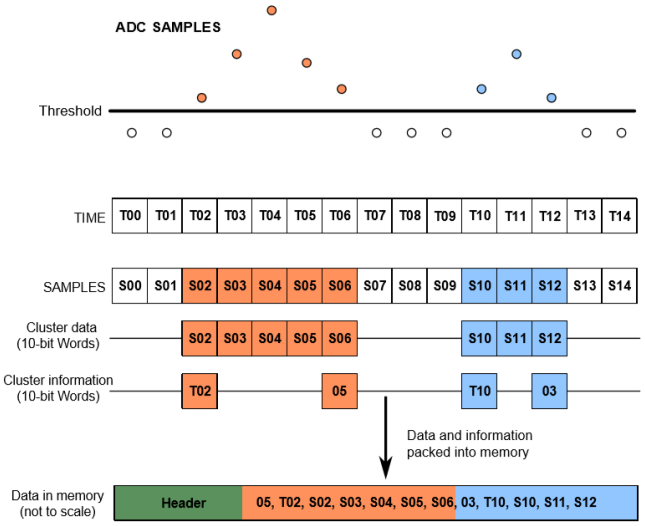
- **A similar system, composed by one or more SAMPA(s) chip(s)**



Challenges

- Understand the SAMPA’s protocol behaviour and;
- Creates a “receiver” to SAMPA serial out signals





Correlated works

- To aid our development of SAMPA and SRS integration, we uses 3 existing projects:

- **SAMPA testboard**: A FPGA project used to develops the SAMPA chip - It contains a complete (and bigger) receiver of all SAMPA serial out

- **Muon Chamber SAMPA integrated**: A FPGA project used to uses a SAMPA chip in a CERN experiment - It contains a very easy-to-use (but poor) receiver of just one SAMPA serial out

- **VMM and SRS integration system**: VMM is another chip, but it already integrated in to SRS - Here, the VHDL inside the FPGA Virtex 6 will be useful.

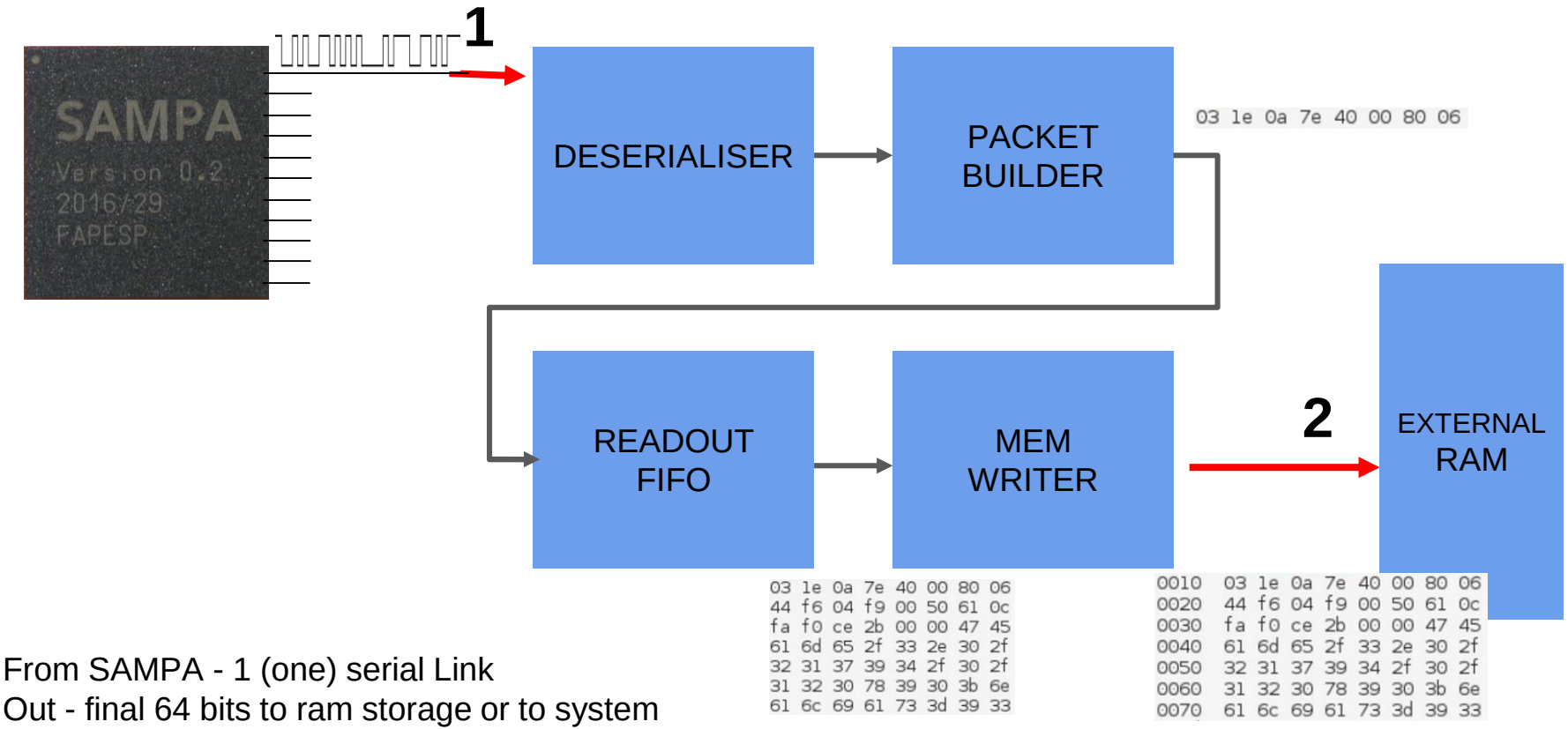
Challenges

- Understand the existing projects and; Reuses part of VHDL codes

- Two options:
- Uses the receiver structure of Tesboard design - A very complex design to understands and uses. May be impossible to uses this structure in Virtex 6 (too large design - study in course…)

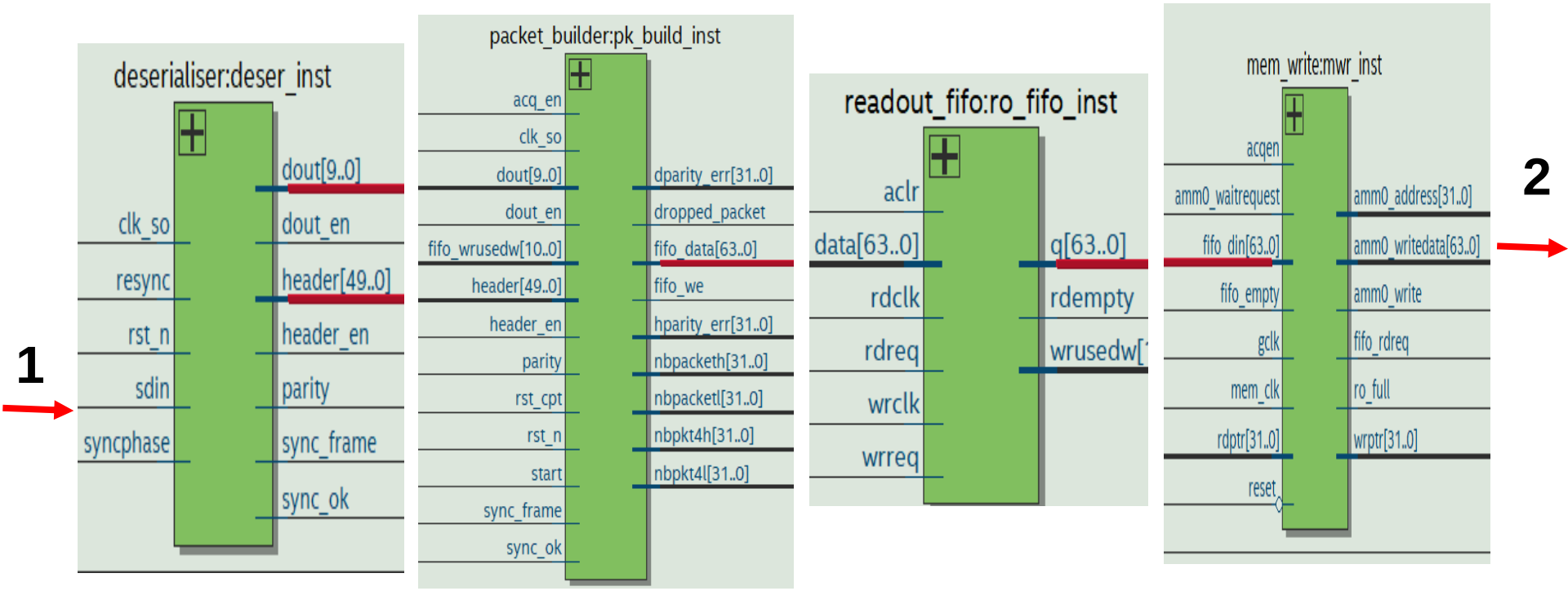
- Uses the receiver structure of Muon Chamber - A simple structure to learn and uses, but it is very poor: It decodes just a one SAMPA link. May be possible to replicates this structure 2 or more times (each structure decodes one SAMPA link)

SAMPA “Muon Chamber” Receiver (VHDL blocks)



1 From SAMPA - 1 (one) serial Link
2 Out - final 64 bits to ram storage or to system

SAMPA “Muon Chamber” Receiver



1 From SAMPA - 1 (one) serial Link
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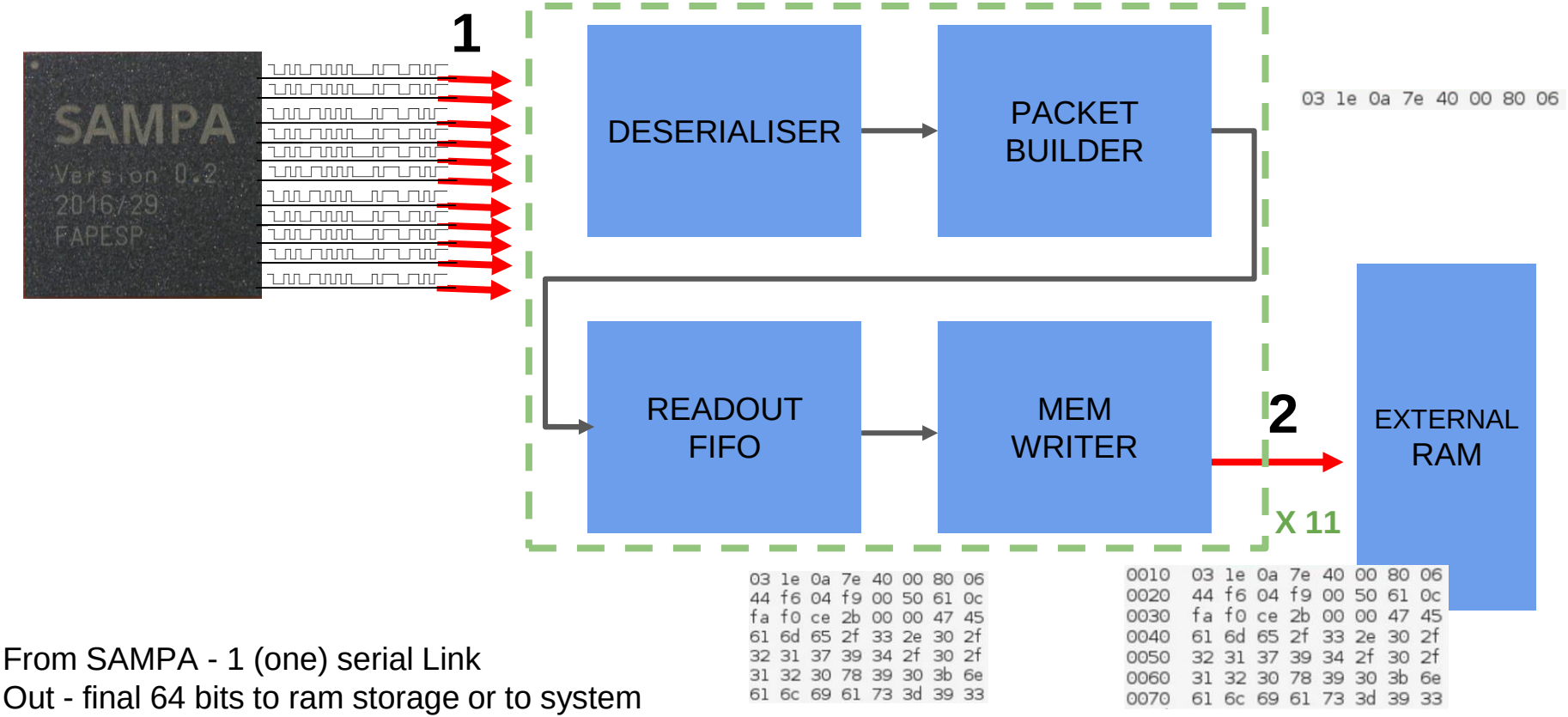
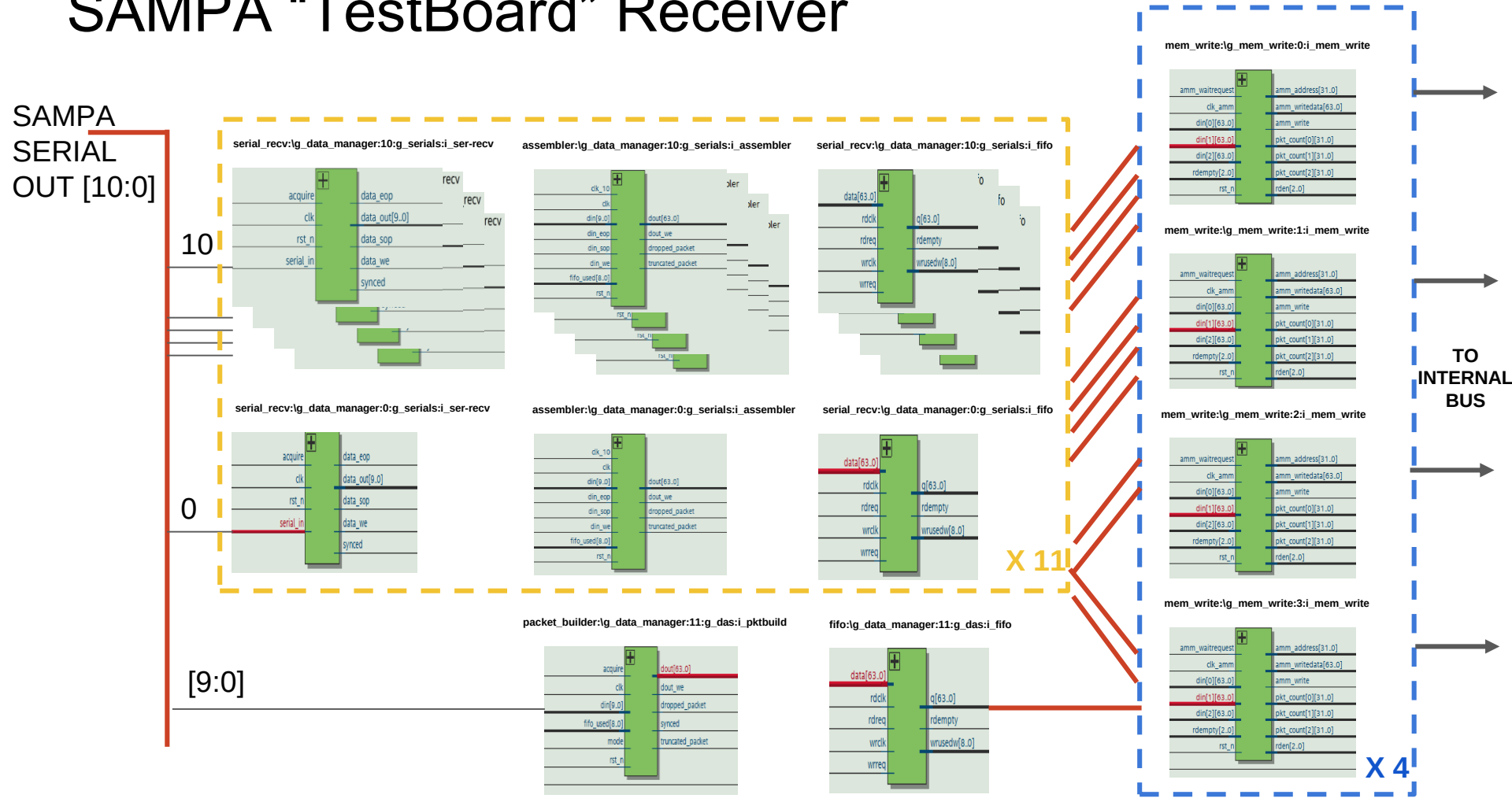
SAMPA “TestBoard” Receiver (VHDL blocks)



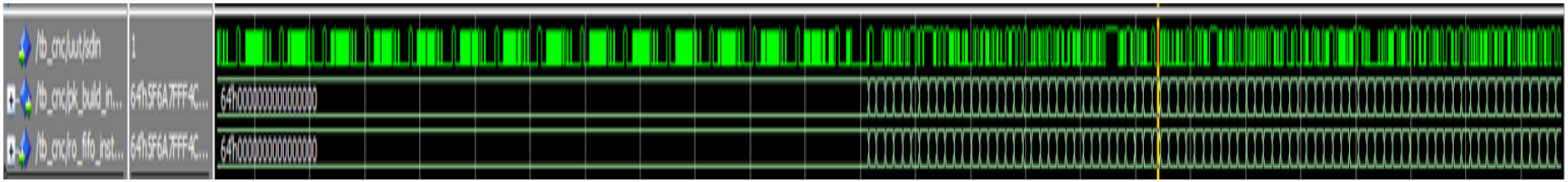
1 From SAMPA - 1 (one) serial Link
2 Out - final 64 bits to ram storage or to system

SAMPA “TestBoard” Receiver

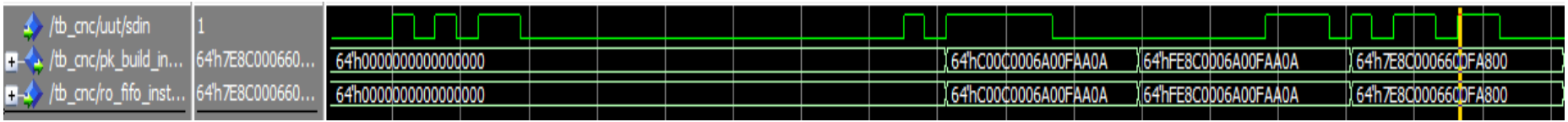


Partial results (simulation only)

The Muon Chamber is being tested with good partial results...

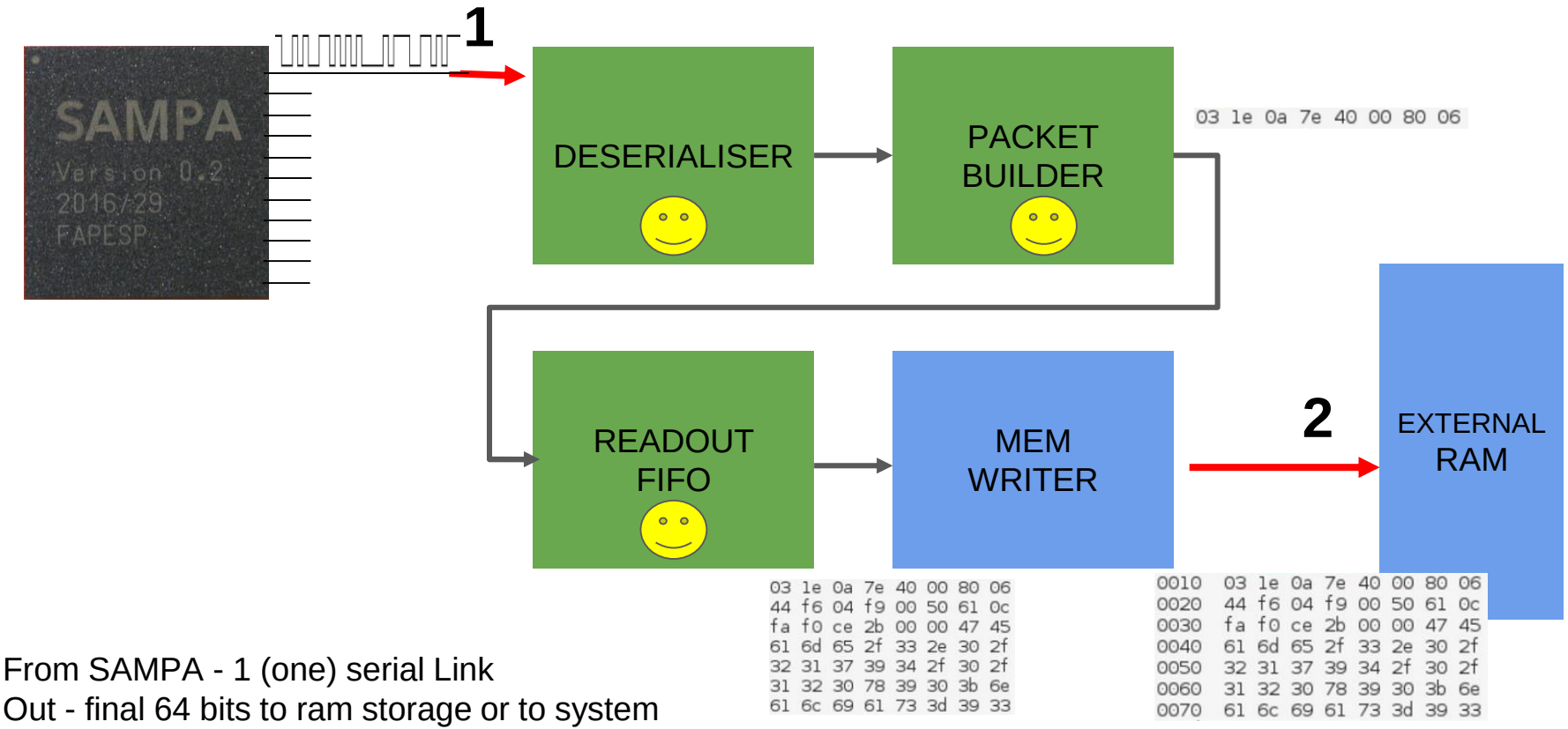


One serial link of SAMPA was decoded in a several payload of 64bits



And the data is being storage in a local FIFO buffer

Partial results (simulation only)



1 From SAMPA - 1 (one) serial Link
2 Out - final 64 bits to ram storage or to system

Partial results (simulation only)

To obtain these “simple” partial results:

1. Deep study and learn of how the SAMPA was developed and simulated
2. So many conflicts of ModelSim simulations was solved
3. So many different VHDL non-standard libraries was compiled
4. Install Quartus II and problems resolution to runs both “Testboard” project and “Muon Chamber” project
5. Install Xilinx ISE 14.7 (in a windows XP) and problems resolution to compile the “VMM_SRS” in the Virtex 6 (just to know the SRS VHDL side)
6. Cut the VMM “VHDL side” and SRS “VHDL side” in two distinct Virtex 6 projetcs - to obtain a clear SRS VHDL project

Next steps

1. Simulates the complete Muon Chamber receive structure
2. Rewrites some VHDL parts of its structure to runs in a Xilinx device (both Correlated Works was developed to uses in Altera device)
3. Try to integrates the modified VHDL Muon Chamber receive structure to SRS VHDL side in the Virtex 6 - here, if we can read one SAMPA serial out… sucess !
4. Verify the possibility of replicates this receiver structure to receives more serial links - a structure similar to Testboard...

References

1. The SAMPA chip
   https://indico.cern.ch/event/647995/contributions/2652469/attachments/1507265/2349076/SAMPARENAFAE_2017.pdf
2. What is SRS https://indico.cern.ch/event/77597/contributions/2088463/attachments/1056845/1506857/RD51-SRS-Description.pdf#page=1&zoom=auto,-274,604
3. SRS + Timepix - Michael Lupberger
4. SAMPA V3 Specification Revision 0.2 Arild Velure, Bruno Sanches

Thank you !!!

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