

RISC-V in 5 minutes

J. Devine

10/5/19



**A fully open
computer:
Open CPU source.
Open toolchain.**

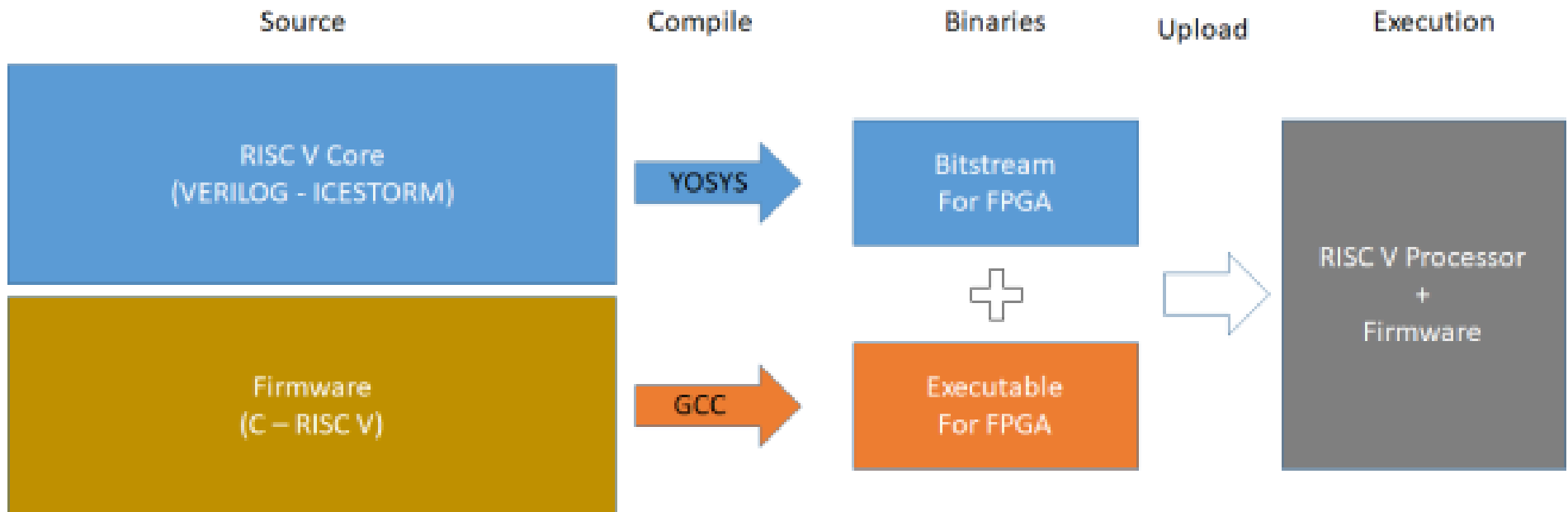
**Build your own,
from source,
deploy to an FPGA,
very quickly!**

For all the details, check out my blog post on this topic:
<https://pingu98.wordpress.com/2019/04/08/how-to-build-your-own-cpu-from-scratch-inside-an-fpga/>



Minute 1: What are we talking about?

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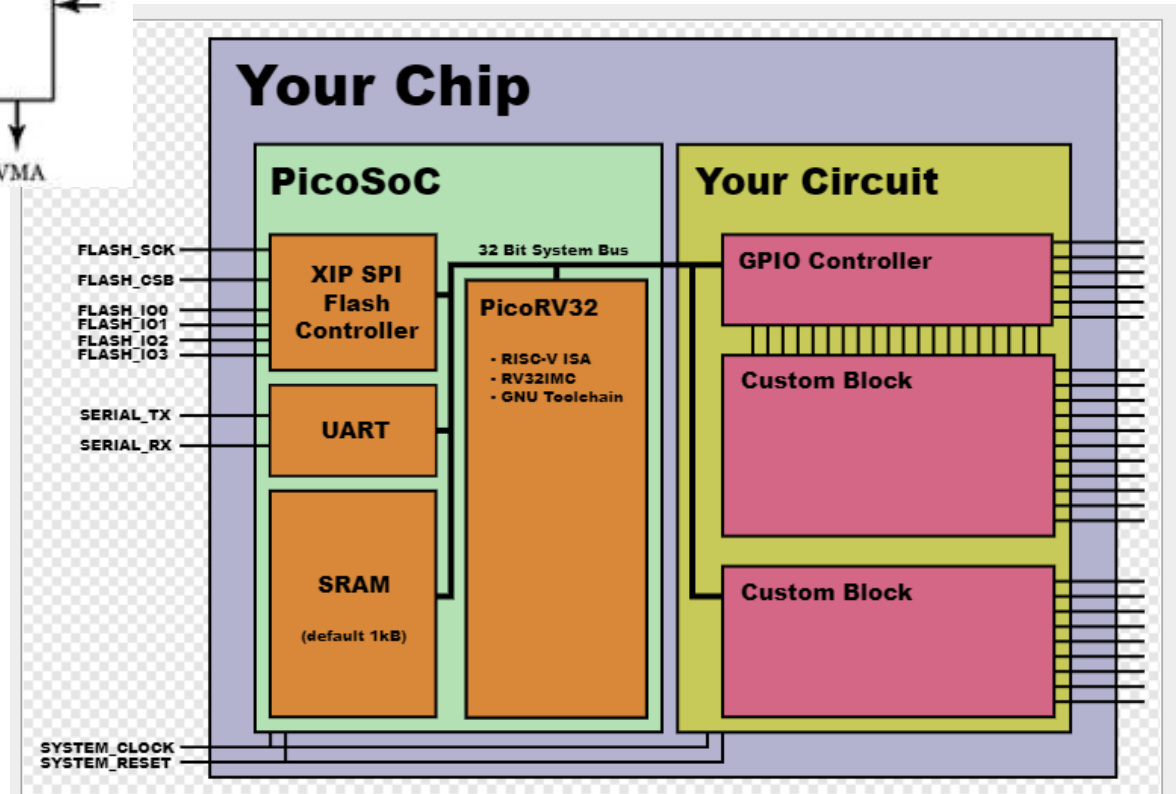
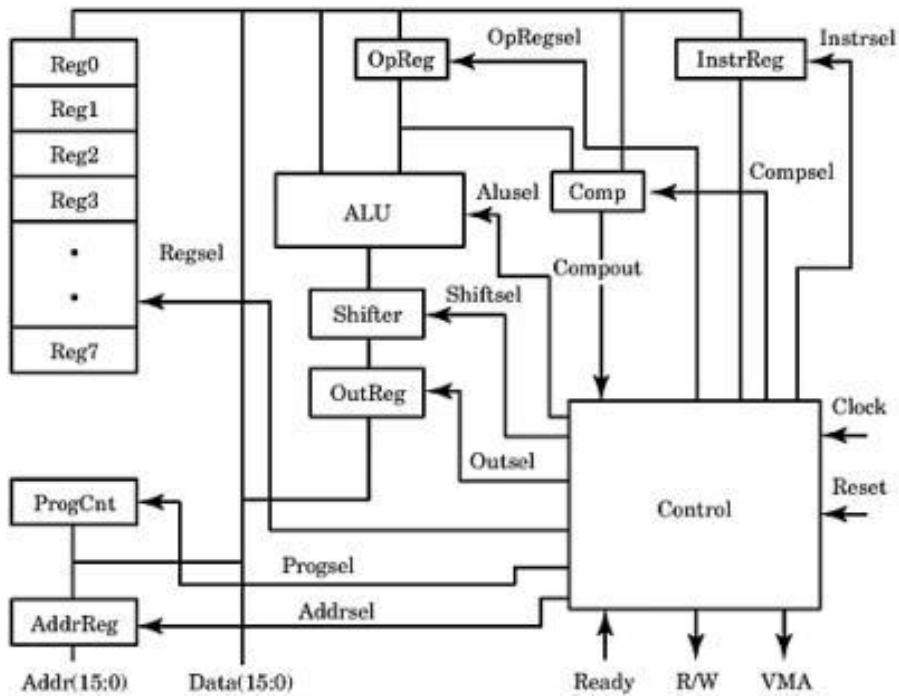


We need two toolchains, one for the processor and one for the code to be executed on the processor.

(actually we'll cheat a little and use one I synthesized earlier since the bitstream generation takes 6-7 minutes on my laptop!)

Minute 2: The toolchains

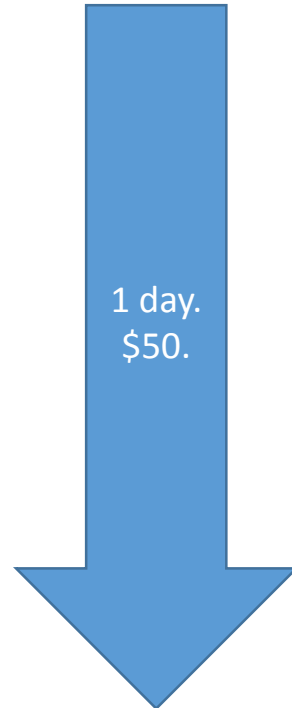
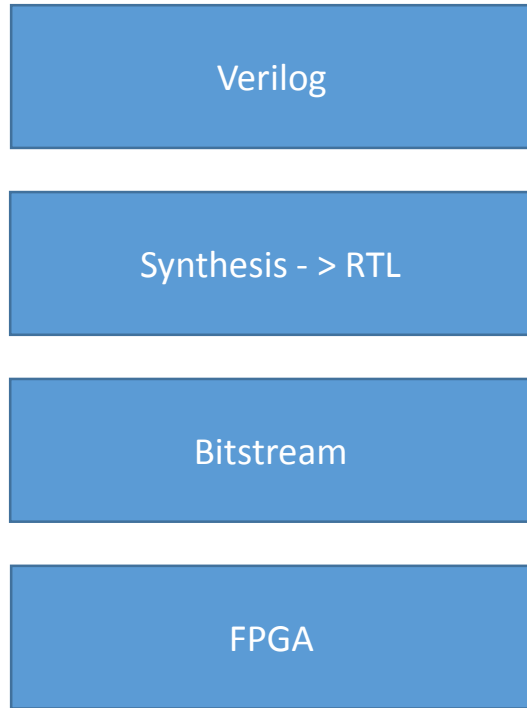
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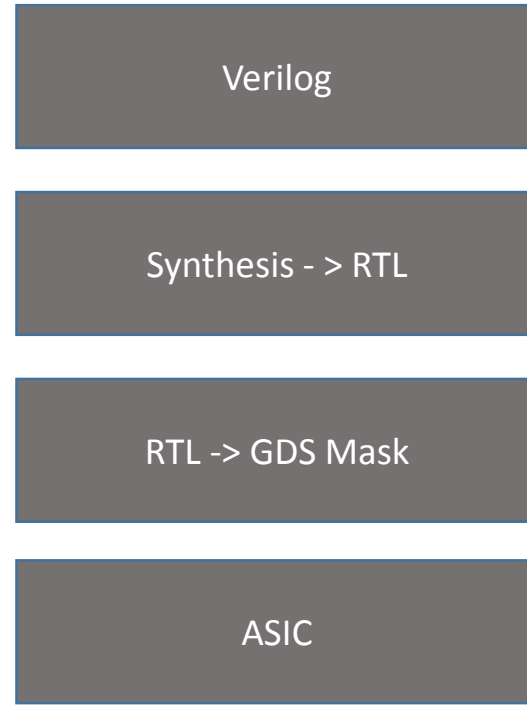
Minute 3: While we wait.

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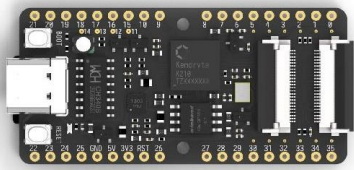
FPGA Route



ASIC Route

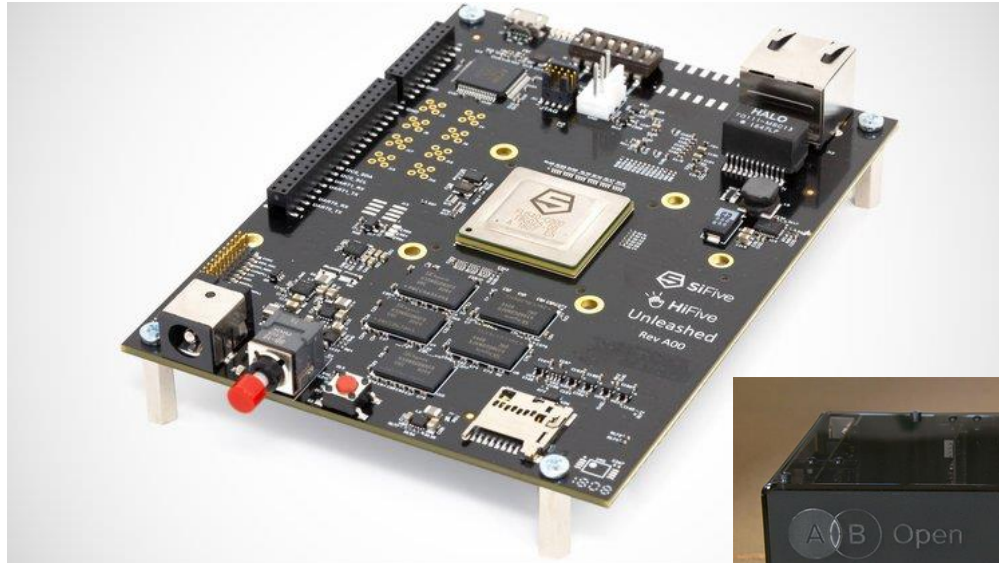


Minute 4: Advantages of this architecture



Maix BiT
Kendryte K210
\$12.90 from Seeed

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SiFive Unleashed -
RISC-V in silicon.
\$999



A RISC-V desktop, as built by Andrew Back \$4000
<https://hackaday.com/2019/02/11/building-a-risc-v-desktop/>

Minute 5: Limits to RISC-V at the moment & demo!