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The electronics of the upgraded LHCb calorimeter system

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The LHCb detector foresees a major upgrade for the next data taking period of the LHC, in 2021. The main characteristics of this upgrade is a full software trigger running at 40MHz. The calorimeter system of LHCb is part of this upgrade and the major evolution consists in replacing the electronics of the electromagnetic and hadronic calorimeters in order to send the full data flow to the counting room at 40MHz by means of four optical links per front-end board (FEB). The former earliest-level trigger calculations performed on the FEB during the runs 1 and 2, will be kept for the upgrade and will be sent to the PC farm in order to optimize the software trigger. The gain of the photomultipliers will also be reduced by a factor 5. This will be partially compensated by an increase of the gain of the electronics by a factor 2.5. The remaining factor 2 will be used to extend the dynamics of the calorimeter and to extend the physics case to some new topics.
The development of this electronics is well-advanced. The analog part has been designed, produced and the production has been tested last year. Several prototypes of the FEB have been realized during the last years. The last one is the pre-production sample and the almost three hundred boards needed should be fabricated in the next months. The firmware of the nine BGAs that equip the boards is mostly written and tested and only limited evolutions are foreseen in the future. The software for the configuration, the control and the tests of the FEB during data-taking has been conceived in parallel to the design of the electronics.
The new FEB of the calorimeters of LHCb will be presented in the context of the upgraded detector. The analog part relies on two integrators running alternatively at 20MHz and is fully differential so that it provides an accurate energy measurement in a 25ns window with a very limited spill-over and leading to a low-noise system, estimated to ˜1.3 ADC (˜7 MeV) per channel, in spite of the increased gain. The performances of the board in term of noise, linearity, diaphony, etc... will be given. The digital treatments and calculations performed in the FPGA to remove the low noise contributions and to determine the quantity needed for the software trigger will be described and illustrated by the test beams performed as well as the tolerance to radiations.

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