Time synchronization and DAQ electronics for ECAL of NICA MPD

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NICA

Nuclotron based Ion Collider Facility
in Dubna, Russia

Heavy ions – 4.5 GeV/n
Protons – 12.6 GeV
NICA Multi Purpose Detector

- Au+Au interactions at 6 kHz (min bias)
- Multiplicity: 1000 charged particles for central collisions at $\sqrt{s_{NN}} = 11$ GeV.
- 5 ~ 30 GB/s raw data rate

General layout of MPD (central part)

1$^{st}$ stage
- SC Coil – superconducting solenoid
- IT – inner tracker
- TPC – time-projection chamber
- TOF – time-of-flight system
- ECal – electromagnetic calorimeter
- FD – fast forward detectors
- FHCal – forward hadron calorimeter

2$^{nd}$ stage
- ECT – endcap tracker
- CPC – cathode pad chambers
General ideas put in DAQ design

- Pipeline operation, data push, flow control
- Diagnostics in hardware and software. Monitoring, logging
- Data integrity: CRC, sequence numbers
- Fault tolerance, SEU events mitigation
- Based on open and industry standards

Timing requirements

1) Time resolution of **10 ns** allows to background and Pile-Up cancellation practically to zero.

2) Significantly higher resolution is required for suppression of secondary photons from the interaction with the material of the MPD detector. These photons arrive with significant delay and simulation studies has shown time resolution of the order of **1 ns** is sufficient to suppress background events down to negligible level.

3) **Sub-ns** time measurement in ECAL allows to use this detector as a time-of-flight device to support main TOF detector. The estimated calorimeter time resolution is approximated by:

\[ \sigma \approx \frac{100 \text{ ps}}{\sqrt{E \text{[GeV]}}} \]

- 38,400 readout channels
- 14 bit, 62.5 MS/s digitizers
- 600 digitizer boards inside MPD magnet
- 38 data merger boards in electronics racks
- 10 kW dissipated power

* drawing shown for illustrative purposes only
MPD DAQ Architecture

Trigger signals

Trigger Processor

Time Server

RDATU

New work

New work (Hardware)

Calorimeter readout

Barrel zone

MPD platform

DRE — Detector Readout Electronics
CRU — Common Readout Unit
FLP — First Level Processor

Ilia Slepnev, JINR

CHEF 2019, Fukuoka, November 28
Timing and Control Electronics
About White Rabbit

- A protocol to synchronize clocks in thousands of nodes with sub-ns accuracy and ps precision
- Developed at CERN in collaboration with organizations worldwide
- Open Hardware, Open Software, commercial production and support by companies

- Precision Time Protocol (PTP) synchronization. Device local clock is synchronized to master clock: link delay is evaluated by measuring and exchanging frames with tx/rx timestamps
- Synchronous Ethernet (SyncE) Layer 1 syntonization: all nodes use same physical layer clock frequency. Clock is encoded in the Ethernet carrier and recovered by the receiver chip.
- Digital Dual Mixer Time Difference (DDMTD) phase detection for sub-ns delay measurement

New revision of IEEE1588 with High Accuracy Option/Profile is expected in 2020.
White Rabbit Network Components

White Rabbit Switch

- Reference clock inputs / outputs
- 18 Gigabit Ethernet ports
- Fiber-optical transceivers up to 10 km
- Management and monitoring
- Web GUI, ssh, SNMP, ...

White Rabbit Node: Protocol IP Core

- Implementation of WR protocol
- Synthesizable FPGA logic
- Integrates with user design
- Includes embedded CPU
CRU-16 board

Timing, Control and Data Merge and Buffer

- 16:1 digitizer board “hub”. Provides clock and trigger information for downstream boards, receives raw data stream, perform by-event merging, buffers data and streams it to computer farm
- 4 GB onboard DDR3 memory for data buffering, decouples real-time hardware data flow from software data receivers
- 4 QSFP downlink ports to connect 16 Detector Readout boards with “hydra” trunk fiber cables, one 40Gb/s QSFP data sink port
- 3 SFP ports for Trigger Distribution, Clock & Timing
- 10/100 Ethernet Slow Control
- White Rabbit for time synchronization with uplink

Status

- FE-Link designed and tested on prototype
- 4 boards assembled and basic functions tested
- Firmware and software under development
CRU-16 and FE-Link

Front-End (FE) link
- Similar to *Synchronous Gigabit Ethernet*. Fixed packet length and latency, 8b/10b encoding and framing
- Maximum data rate: 2.5 Gb/s VXS backplane (TTVXS), 8 Gb/s (CRU-16) with commercial fiber-optical transceivers.
- DRE clock synchronized to CRU with digital PLL. Short fixed cables – one time delay calibration.
- Timestamps, trigger, data readout, control over same link
- No TCP-IP stack complexity in DRE. Simple FPGA code with fail-safe FSM and data pipelines to mitigate SEU events.

Aggregation “switch” (CRU-16 core)
- Data packet switch. Connects to DAQ network with 10 GbE (40GbE option), hardware UDP-IP.
- On-board FPGA running White Rabbit and service CPUs
- Raw data diagnostics: hardware histograms, RAM-based multichannel counters
- On-board DRAM buffer to mitigate software latency
- Hardware event data merging (future option)

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TTVXS — VXS Switch Board

TTVXS is a Time, Trigger and Management module for VXS crate

- Clock, timestamp and trigger distribution to VXS payload boards over VXS serial backplane
- 4 SFP+ sockets for Detector Readout, Trigger Distribution and Clock & Timing connections
- Reference frequency and timestamp provided by White Rabbit Network or FE-Link (with CRU-16)
- Additional clock and trigger interface by FMC (VITA-57) card slot – integration with other systems

Status
- Second PCB revision, 4 boards ready, more in production
- Basic functions implemented
- Put in operation for MPD TOF test stands

IPMI mezzanine board

- IPMI (Intelligent Platform Management) function for automatic topology discovery, module status monitoring and control, firmware update. Also used in CRU-16.
- SNMP, Web, console. Runs FreeRTOS on STM32F7 CPU.
Digitizer Electronics
Signal arrival time estimation methods

Typical MPD ECAL SiPM signal digitized with 14 bit, 62 MS/s ADC. Proper shaping and anti-alias filter assumed. What time resolution can we get with which algorithm?

- Fixed threshold, with baseline recovery, or
- Digital constant-fraction discriminator, zero crossing
- Leading edge or CFD with linear interpolation
  FPGA possible, high DSP block usage
- Digital, shape parametrization (curve fitting)
  CPU/GPU implementation preferred
  new signals may require new curve equation
- Digital, deconvolution and gaussian curve fitting
  Works with arbitrary curve. Automated deconvolution filter construction.

\[
\frac{\sigma t}{T} \sim k \frac{1}{\text{SNR}}
\]

Precision limited to digitizer time step
\(16\text{ ns}\)

Fractions of digitizer time step
\(~ 1\text{ ns}\)

\(~ 100\text{ ps}\)

Depends on pulse shape and signal to noise ratio
Signal recovery: “deconvolution”

Acquisition channel as discrete Linear Time Invariant (LTI) system. Note: Non-linear effects have to be corrected before or after linear transforms.

\[
f \ast g + \varepsilon = h
\]

\(f\) – input signal, detector current
\(g\) – acquisition channel transfer function
\(\varepsilon\) – electronics and quantization noise, distortions
\(h\) – actual value recorded

**Acquisition channel transform**

**Time domain convolution**

\(f \ast g \approx h\)

**Frequency domain multiplication**

\(F \cdot G \approx H\)

**Signal recovery**

**Time domain “deconvolution”**

**Frequency domain division**

\(G^{-1} = F / H\)

Reverse transform \(G^{-1}\) is approximate: random noise and distortions are irreversible. Optimization of gaussian signal phase (position) and width allows to minimize reverse transform artifacts.

**Actual registered ADC waveform**

**“deconvolution” FIR filter impulse response**

**“deconvolved” and gaussian fit**

Why gaussian shape

- Computational simplicity for Least Squares Fit methods
- Tail cancellation – for free
- Fixed shape – same algorithm code for all data, allows GPU implementation or CPU optimization.
- Fast! LSq fit Levenberg–Marquardt on CPU: 70,000 waveforms per sec per core
ECAL digitizer board structure

- 64 channels, 14 bit 62.5 MS/s
- White Rabbit compatible hardware
- Clock frequency synchronized to master
- Constant phase (time offset)
- FE-Link: Time, Trigger, Control and Data streaming on single fiber link
- Magnetic field tolerant
- FPGA SEU mitigation: fail-safe FSMs, data pipeline architecture, configuration scrubbing
- Cooling: liquid, leak-less system

SiPM \(\rightarrow\) shaper \(\rightarrow\) ADC \(\rightarrow\) FIR \(\rightarrow\) BLR, Z/S \(\rightarrow\) ring buffers

- Sampling clock
- Digital phase detector
- Recovered bit clock
- Control, data format, FIFO
- TCP-IP
- RX/TX PHY
- SFP+ optics 10GBASE-X
- FE-Link

DAC \(\rightarrow\) PLL servo

- 8 blocks x 8 channels
- Shared DSP at 500 MHz
- ~100 us uncompressed

- RC A/A filters
- 4 x ADS52J90
- FEASTMP, DC/DC
- FPGA
- JTAG
- Dual SFP to CRU-16

ADC64ECAL board v1.0 (without liquid cooling system)
Results

- digitizer and timing electronics designed, assembled and tested
- pre-production samples put in operation on test stands, ready to mass production
- Basic functions of FPGA firmware and DAQ software works on test stands. Development continues: hunting bugs, replacing legacy code, optimizations, etc.

photo: Clock distribution test setup

VXS crate with 72-channel 24ps TOF TDC modules and TTVXS in the middle
BMN-2018 Time Synchronization Test

Calibration pulse timestamp difference across detectors, BMN Run 5143
TDC resolution: 20 ps RMS each channel

GPS time server

10 MHz
1 PPS
NTP date

WRS-3/18

Crate-level clock distributor

Multichannel TDCs

T0 “start” detector

8 m twinaxial

TOF detectors

10 m coaxial

Multichannel TDCs

calibration pulser
500 kHz, TTL

Online monitoring per-event ΔT histogram

ΔT Measurement precision was limited by TDC used
Long-term drift observed: next slide...

σ = 29 ps
BMN-2018 Time Synchronization Test

Long-term drift is caused by 25 ps/°C temperature coefficient of AD9548 PLL used in measurement board.

Time difference averaged by spill
BMN Kr run
14 hours data taking

run 4976
run 5015

Time drift < 20 ps
MPD time distribution board – Lab tests

Two TTVXS v1.1 boards synchronized to White Rabbit switch WRS-3/18

Histogram of relative time difference, $\sigma = 10.439$

- $\sigma(\Delta T)$ 10.5 ps
- $\pm 42$ ps max no dropouts

Clock phase difference measured with 14-bit 125 MS/s ADC board (8 ps $\Delta T$ intrinsic resolution)
Clock edge time reconstruction performed by software
Measurement time: approx. 5 minutes
Long term stability: TBD

- Temperature compensated precision VCXO: Connor-Winfield DOT050V 20 MHz
- PCB trace, clock multiplexer and fan-out components delay variations are compensated by PLL feedback loop
Thank you!
Backup slides
References

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3. MPD Data Acquisition System Technical Design Report, 2019
4. T.Włostowski, Precise time and frequency transfer in a White Rabbit network, 2011.
5. https://www.ohwr.org/project/white-rabbit