Report on the 2019's SiW-ECAL beam test @DESY and the COB performance

A. Irles, LAL-CNRS/IN2P3 on behalf of the **SiW-ECAL**

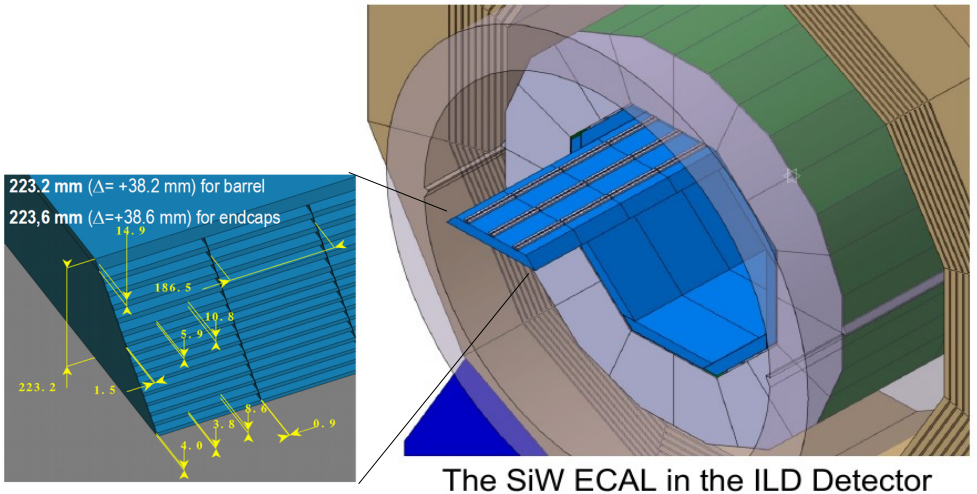
CHEF2019 29/11/2019

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 654168

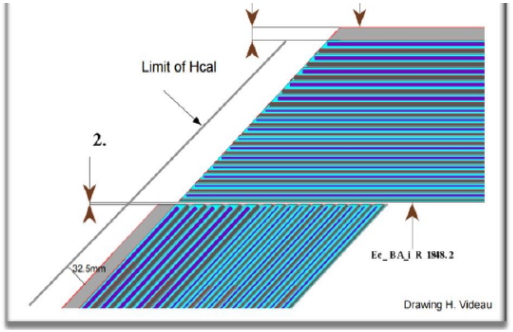
Introduction

Towards a real detector: (some) challenges

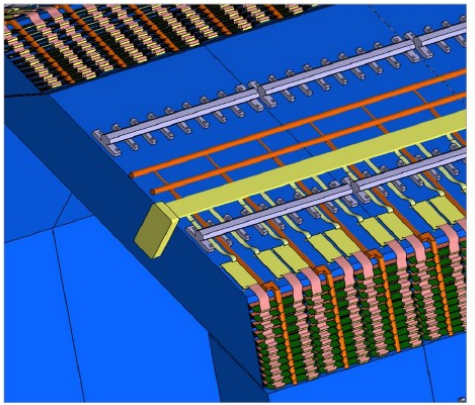
- **Long slabs** : up to ~15 ASU (~3m)
  - Complex object: mechanics and electronics.
  - Electrical prototype built and tested (see J. Kunath's talk)
- **Spatial constraints: front-end** (see R. Poeschl's + this talk):
  - limited space between layers and between ECAL and AHCAL
  - Control & Readout electronics at the extremity of the slab.
  - One electronic card for controlling and reading~10^4 channels
- **Spatial constraints: ultra thin PCB** (this talk):
  - Very compact design: 20 cm for 20-30 active layers + 24X0 tungsten → very limited space for inactive material (PCB, electronic components)



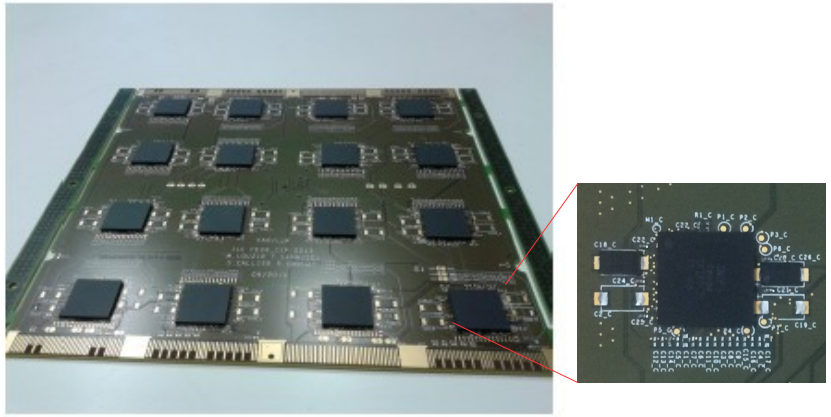
The SiW ECAL in the ILD Detector



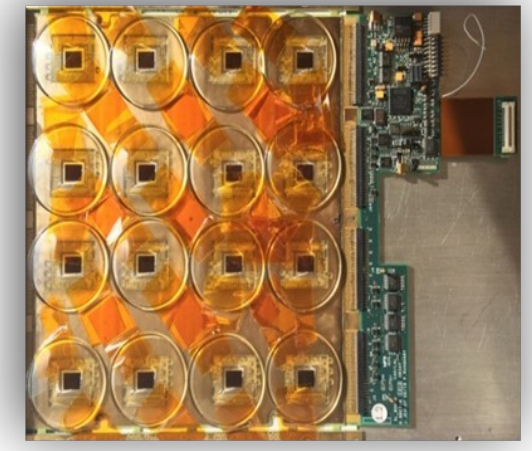
E-CAL Services



Reminder: R&D on PCB for SiW-ECAL



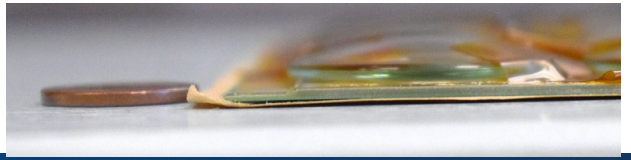
- BGA packaged chips
  - Space for external decoupling capacitors
  - Symmetric stacking will improve flatness,
  - good for wafer gluing
  - Optimal shielding of signal traces

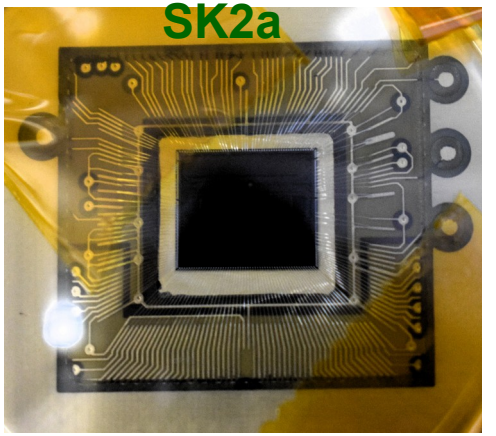


- PCB with naked die
  - Thin board (~1.2mm)
  - Planarity is an issue
  - Challenging for PCB producers
  - Little space for extra components
- See later.

Ultra thin PCB: Chip On Board

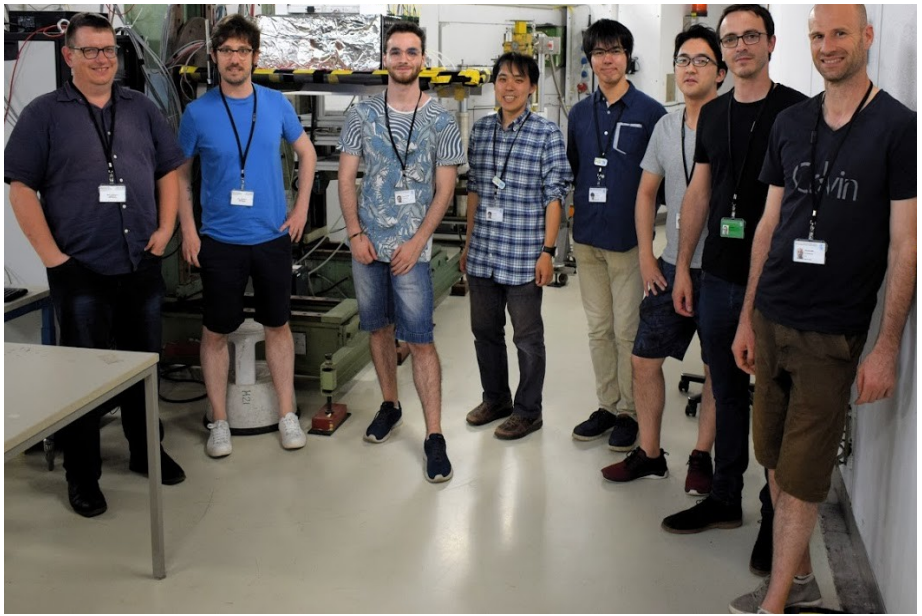
- **ILD tight spatial constrains:** Total space for ASICs and PCB 1.8mm (was 1.2mm since ~2007)
- **Chip-On-Board proposal:**
  - Naked ASICs wirebonded.
  - Cavities (~250um) for the ASICs
- **LAL & OMEGA** collaboration with **ITAEC/SKKU** (Sungkyunkwan University, Suwon – Korea) and **EOS company** for the PCB production.
- 10 FEV11_COB produced.
  - **1.2mm thickness** → 9 layers PCB !
  - **Good Planarity** (metrology made in LAL) and electrical response.
  - **No extra components** (i.e. decoupling capacitances, etc)
- **4 boards wirebonded** at **CERN** bonding lab. Also In contact with CAPTINNOV Platform.
  - Extensively tested at LAL before gluing a full size sensor to them

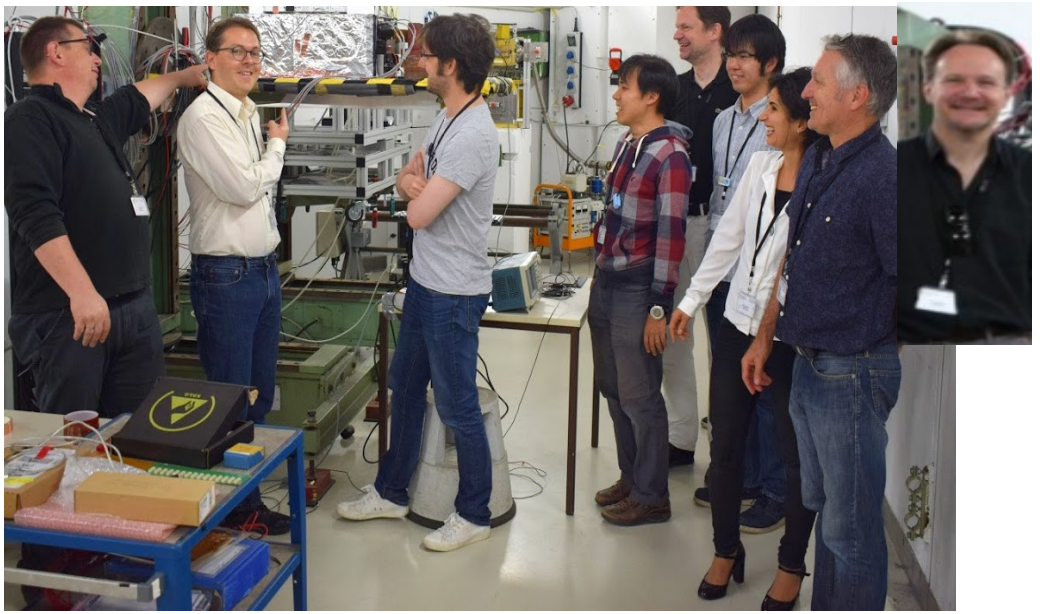




Test Beam 2019

- Two weeks of Beam Test at TB24. From 24th June to 7th July.
- Presence from





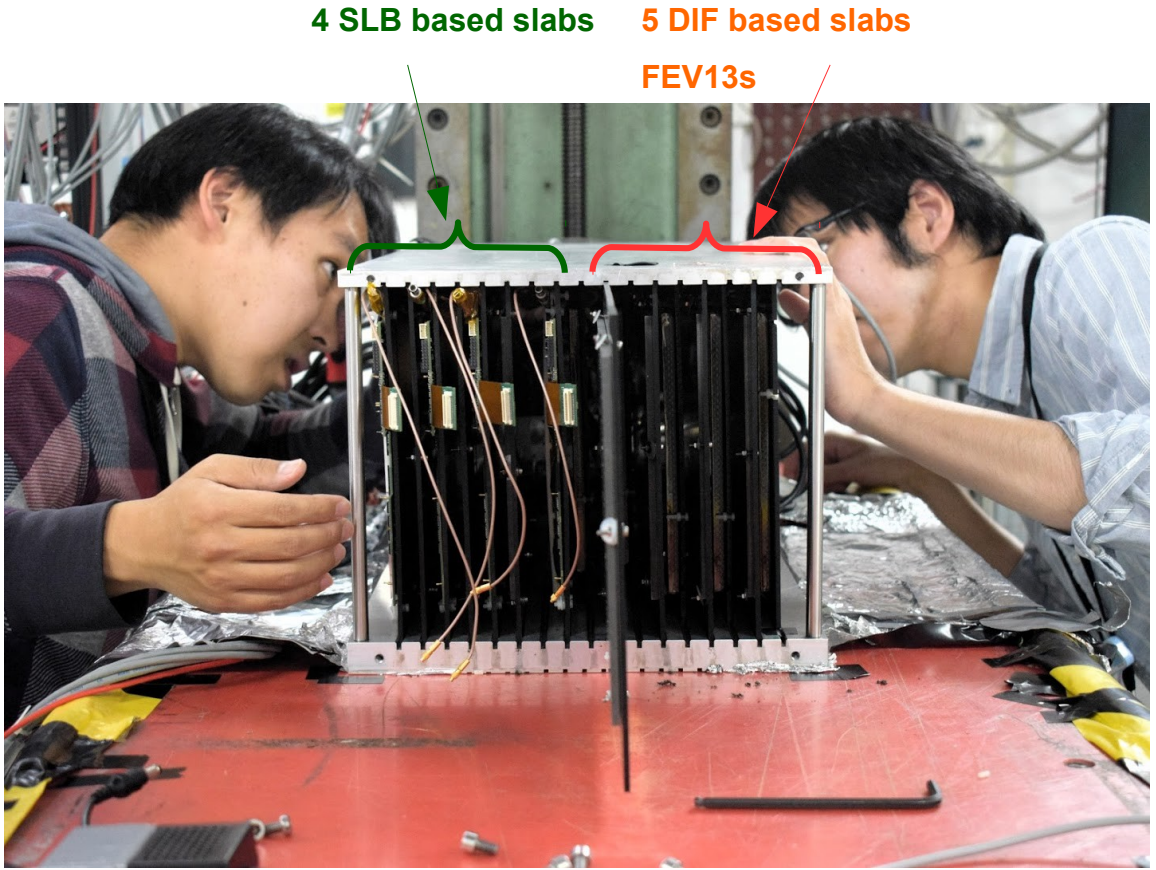
- Plus support & hardware from

"The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)".

HELMHOLTZ
SPITZENFORSCHUNG FÜR
GROSSE HERAUSFORDERUNGEN

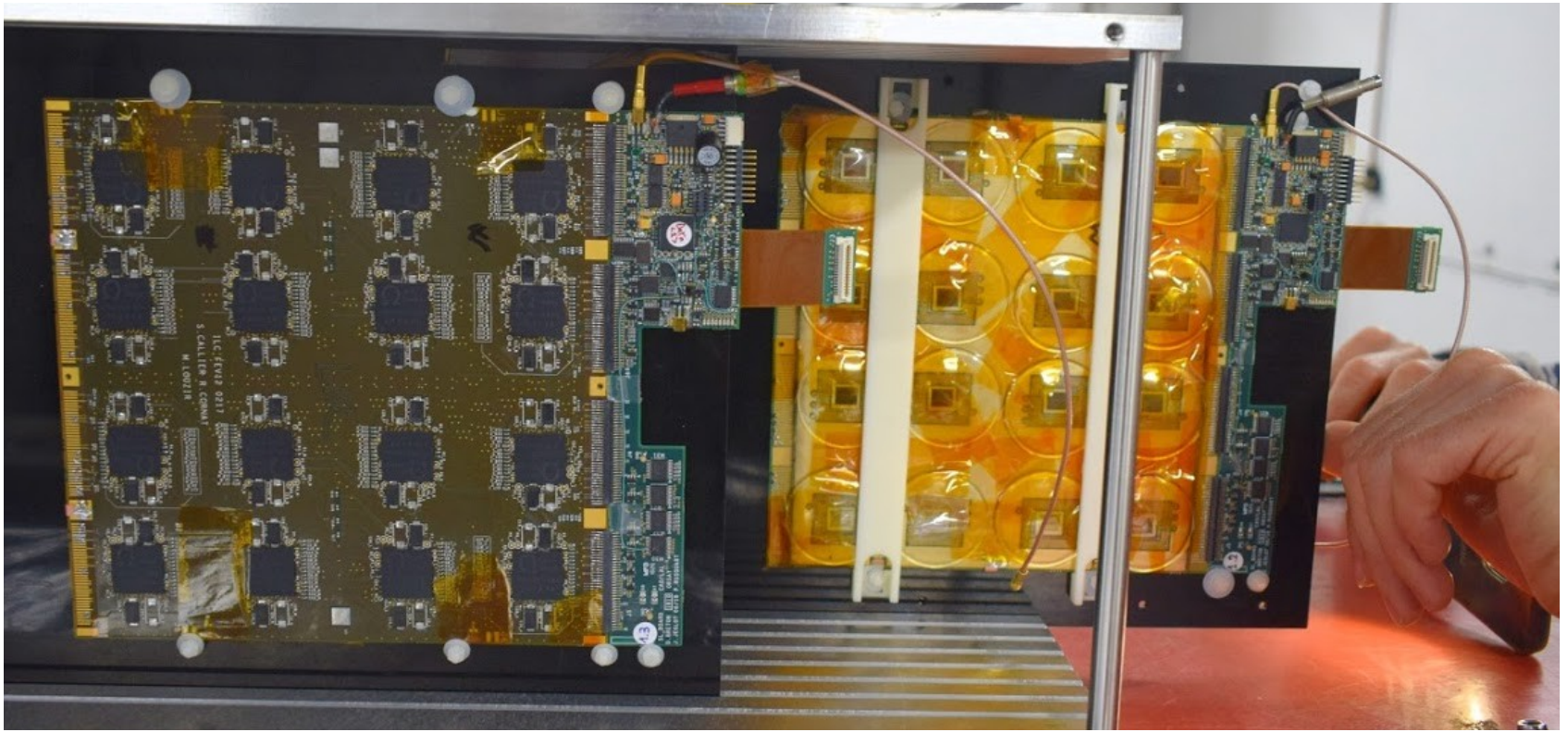
TB setup

- Devices under test:
  - **5 FEV13Jp** fully equipped with 4 Si wafers each. All of 650um except one slab with 320um. **Interfaced with the "old" front end.**
  - **2 COB (called a and c)** boards with one wafer each (500um) and the new **SL-Board**
  - **2 FEV12** boards with one wafer each (500um) and the new **SL-Board**
  - All boards equipped with **skiroc2a ASICs**
- First week: 5 FEV13Jp and 1 COB and 1 FEV12.
- Second week: full setup with 9 slabs.



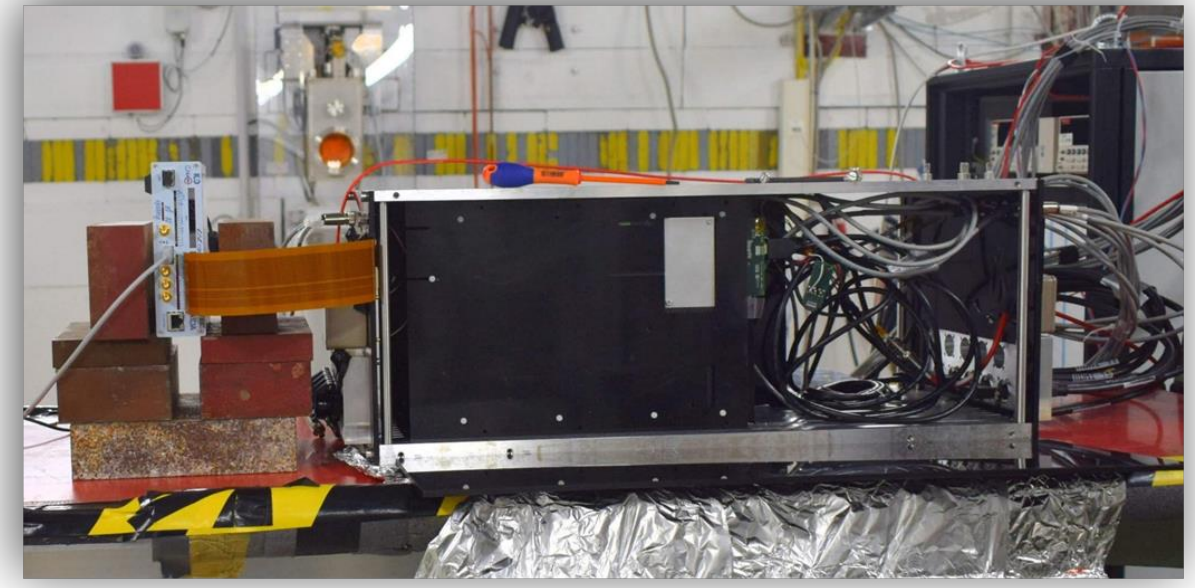
- FEV13's ASICs are operated in Power Pulsing, COB and FEV12's still in Continuous Mode.

TB setup



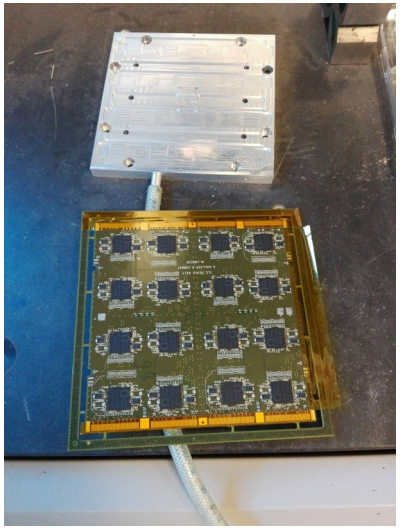
TB setup

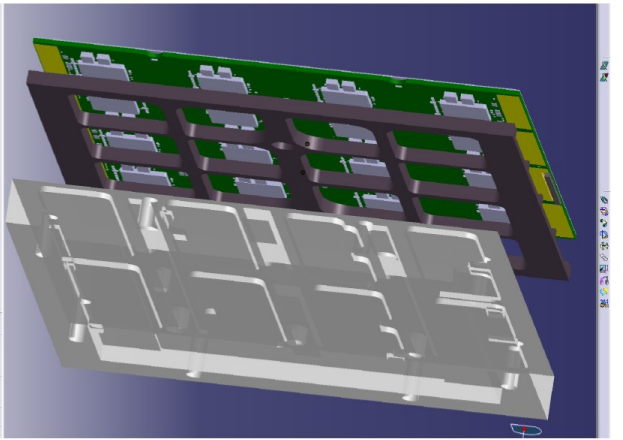
- Flexible prototype stack able to hold the 9 slabs + 8 W plates of different thicknesses. All mounted in plastic plates. The box have two frontal panels (one for DIF and one for SL-Board)
  - One with 4 short HV cables + 4 short LV cables for SLB and the kapton PCB for DAQ.
  - One with 5 HV cables + 5 SMBV5 LV cables + 5 DIF LV cables + 5 HDMI cables for DAQ.



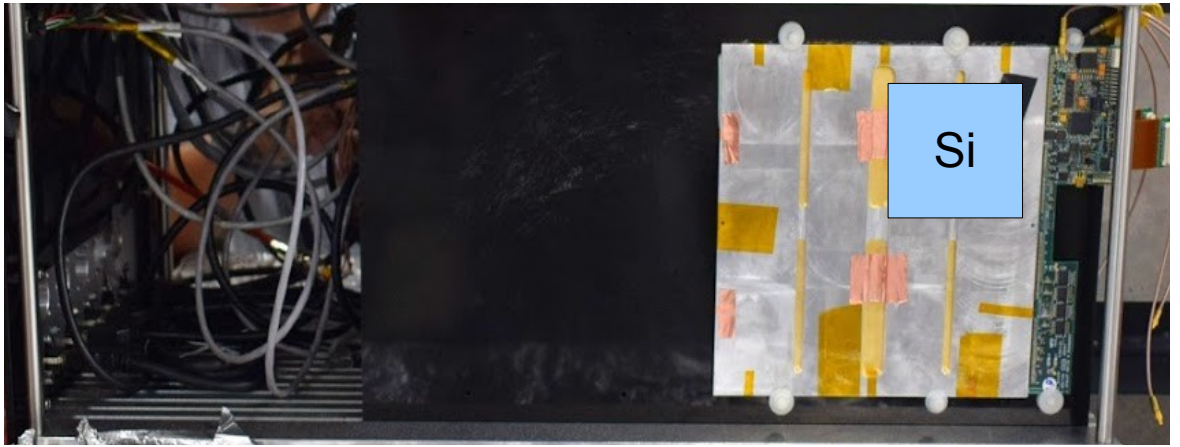
SLB based slabs: gluing

- Wafer gluing made at LPNHE.
  - One wafer per PCB.
- Last glued board received during the beam test.



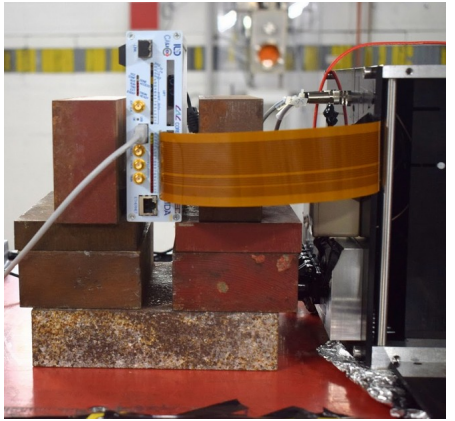


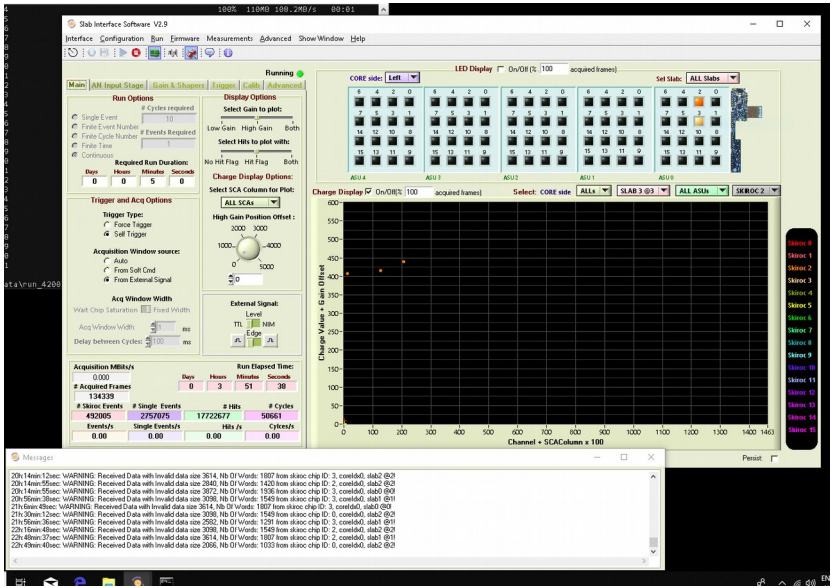
- Current aspiration setup of the gluing robot and the current COB version are not fully compatible
  - in fact, the FEV12 also needs some manual work before starting the the process
- This was fixed by fabricating a simple aluminum (or even a 3D printed) mask to transport the vacuum from the pipes to the COB.
  - Very useful input for the next COB generation.



SLB based DAQ

- **Impressive and very intuitive debugging + on site commissioning capabilities.**
  - Online monitoring for all channels and SCAs.
  - Easy and human friendly environment: quick masking of channels, change of thresholds etc.
  - Automatic commissioning procedure possible (already there at the beam test but not extensively tested)
- At LAL, the boards were extensively tested before gluing the sensor.
- But the boards with glued sensors where **commissioned** to a working level just on site… in less than **30 minutes** !!! (i.e. masking of channels, setting of thresholds etc).



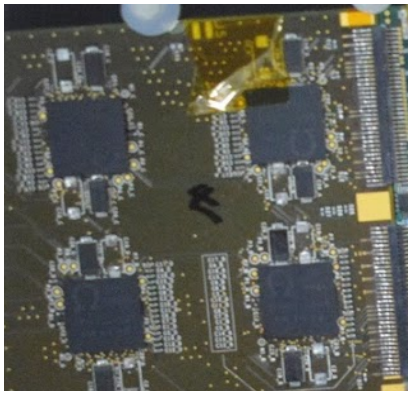


COB performance

General beam test results described in Y. Kato’s talk.

COB-a: with and without extra capacitances

- The COBs are equipped with zero extra components (i.e. no decoupling capacitances).
- FEV experience show that adding decoupling cap. between GND and the analogue power supply of the chip are mandatory to control the noise.



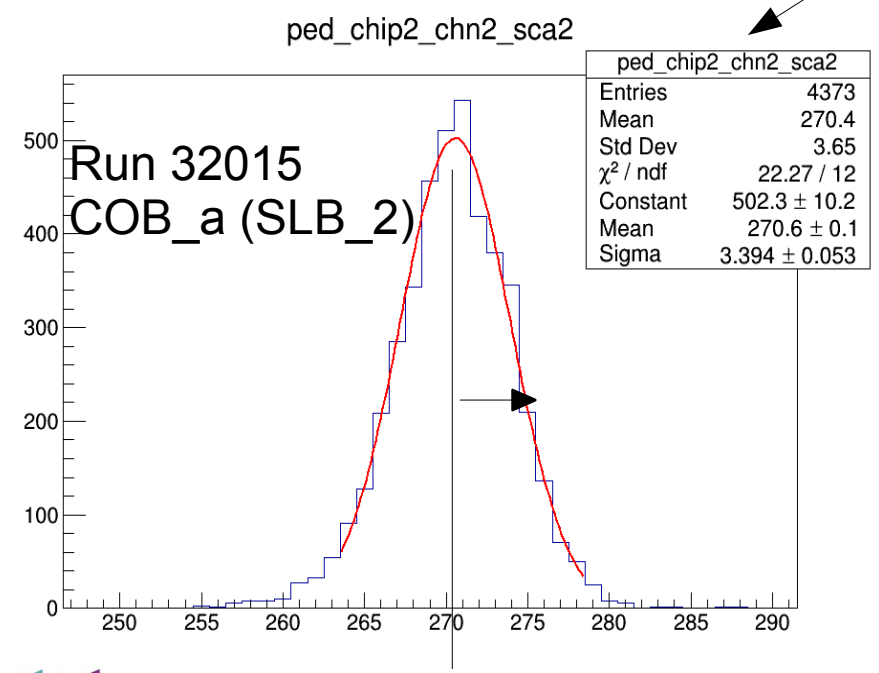
FEV 8-13 At least two cap (120 and 150uF) per chip

- We compare the performance of one of the COBs w/ and w/o.
- Run 21003: COB_a “naked”
  - 3.6pF gain, DAC=300 and with same acq window (2ms, 10Hz)
- Run 21010: Cob_a with 4x150uF cap. Between AVDD and GND.
  - 3.6pF gain, DAC=300 and with same acq window (2ms, 10Hz)

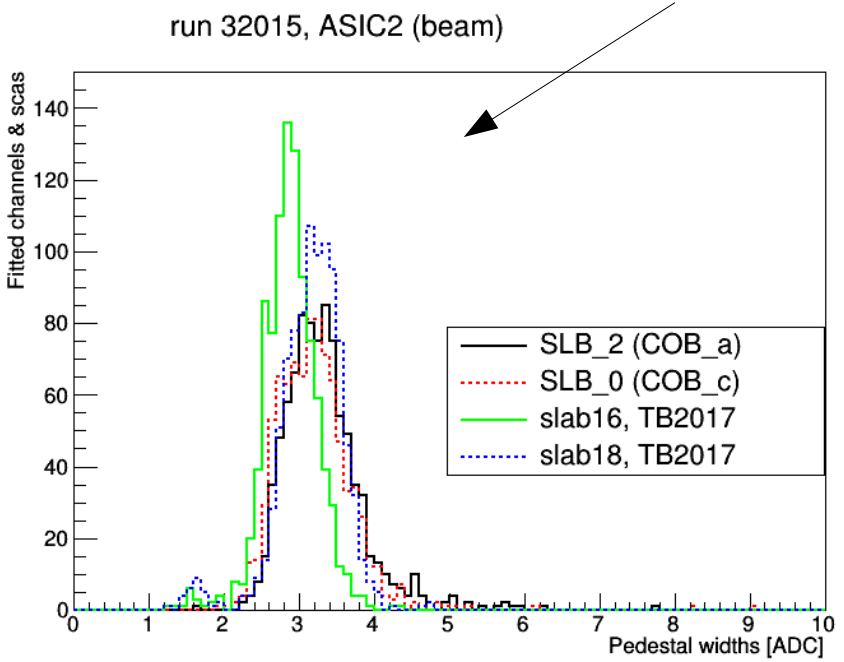
Pedestal calculation

- Analysis done after event filtering of fake signals.
- Check the charge (HG) of non triggered cells.
- Pedestal = Mean (gauss fit)
- Width = Sigma (gauss fit)

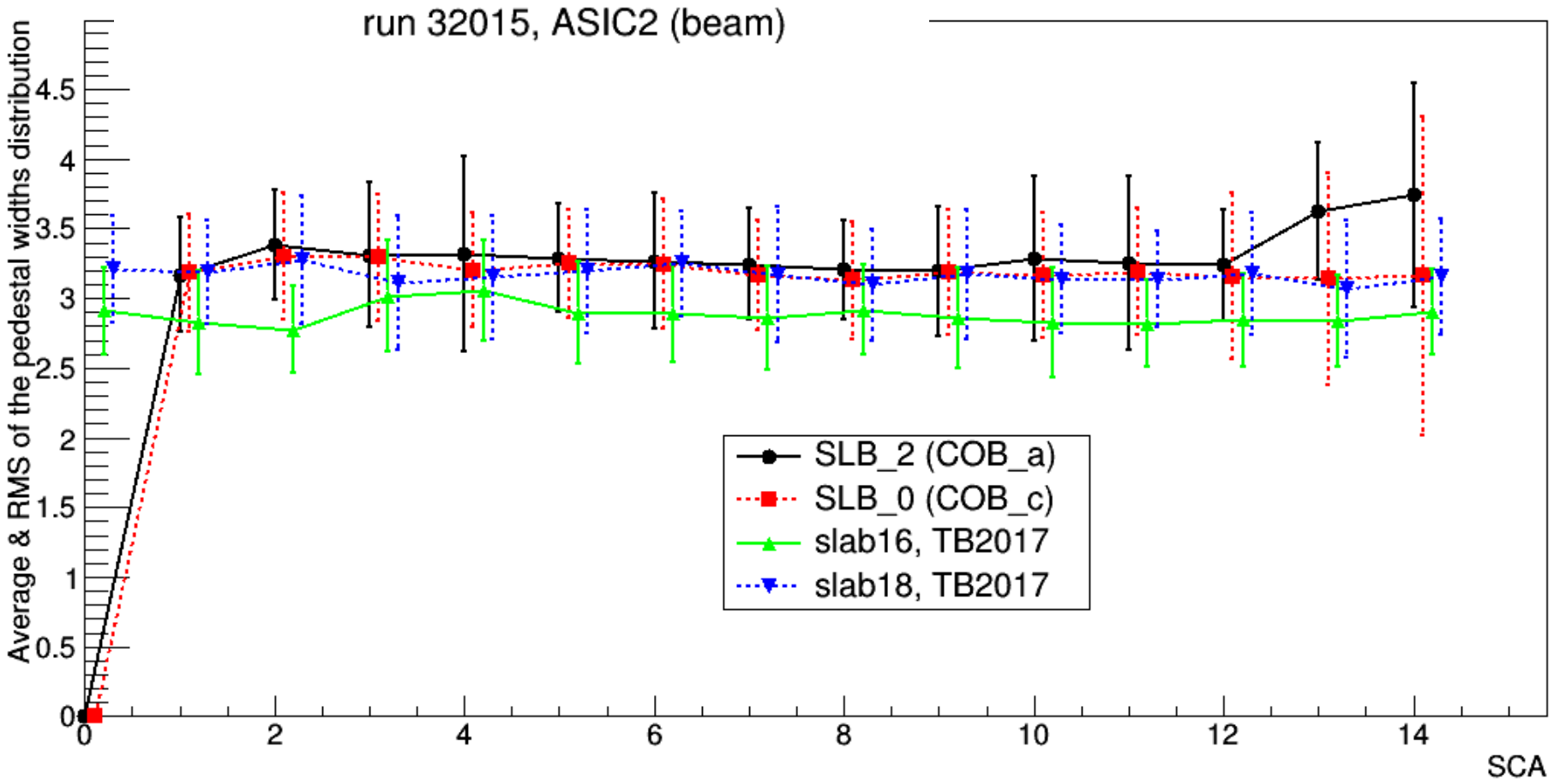
pedestal distribution
example (one chn, one sca)



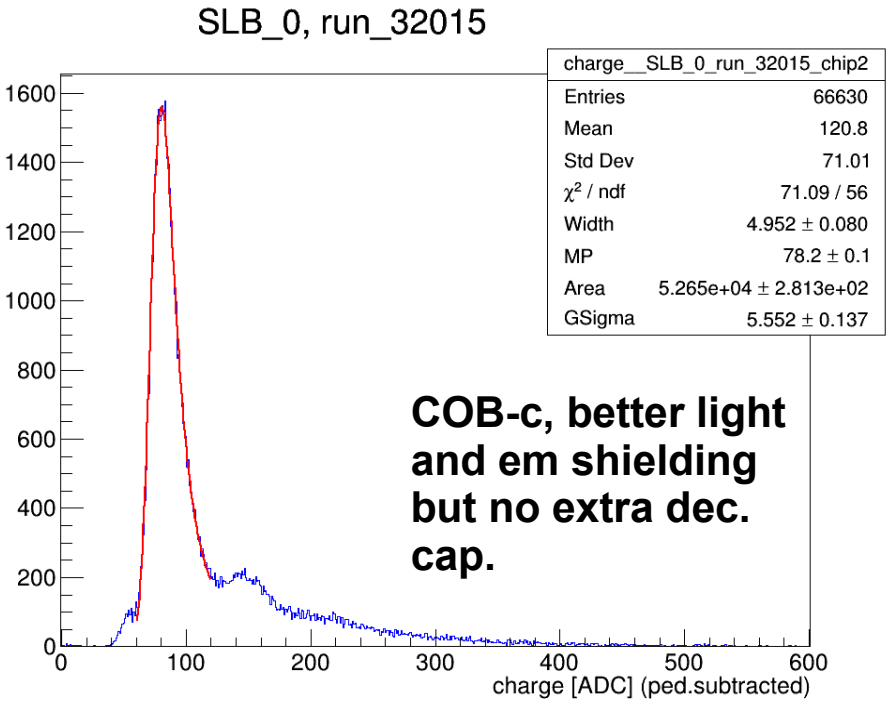
Distribution of all calculated
pedestal widths

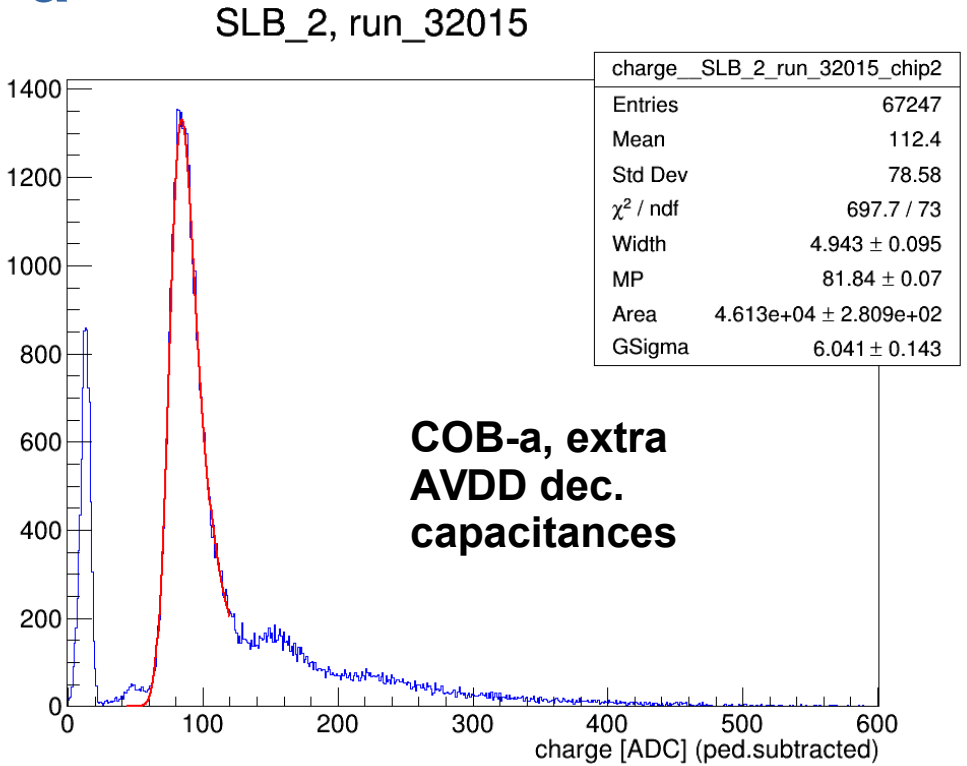


Pedestal calculation: width



MIP calibration COB-c vs COB-a





- Comparable spectrums for both boards
- **MIP spectrum integrating all cells** in ASIC 2 (SLB systems) or ASIC 13 (FEV13 systems)
- Few noisy channels in the COB-a (peak at 0)
  - Improvable by optimizing the thresholds.

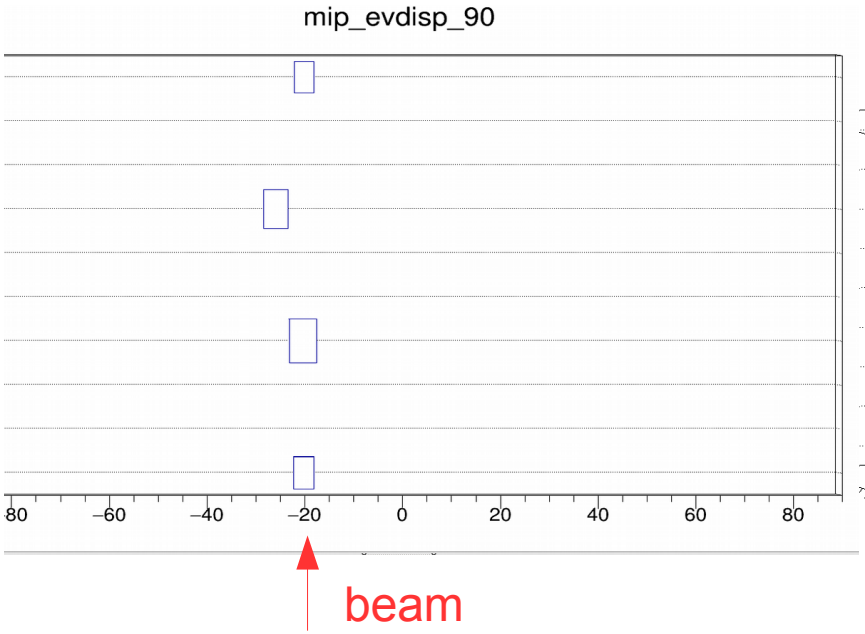
COB summary

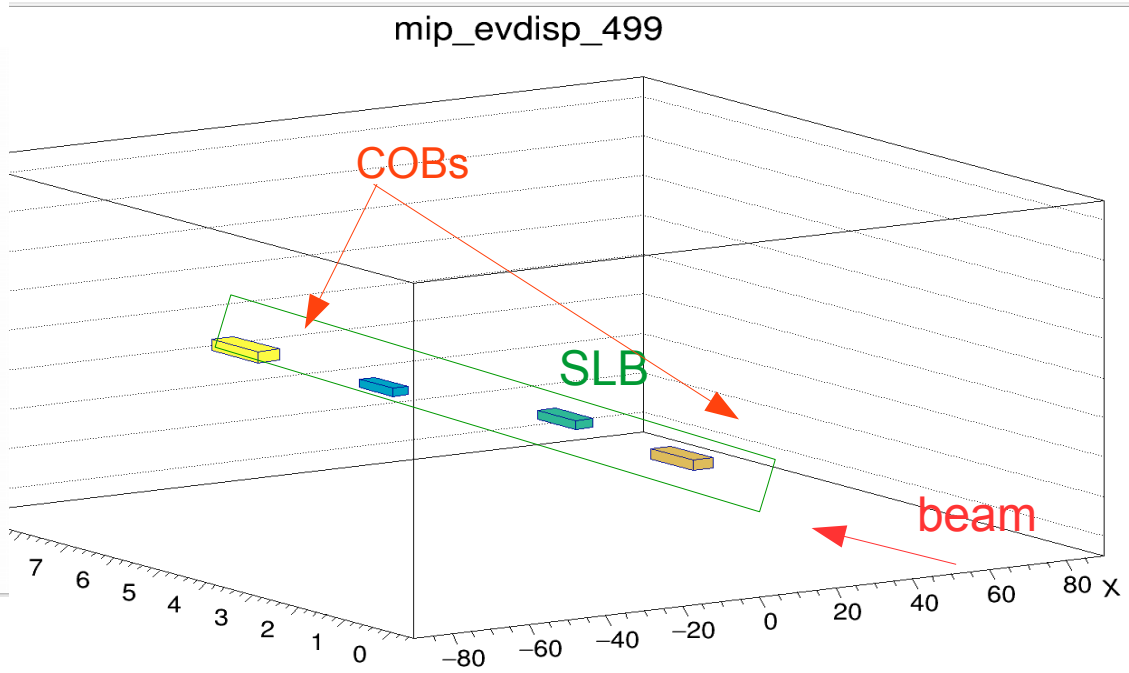
- Gluing wafers is possible in a automatized way:
  - Good planarity of the boards !
- Different Skiroc2a configurations tested with both COBs (gain, thresholds, etc)
  - Dedicated commissioning of the boards and of the new DAQ.
- Competitive results with BGA, after adding few decoupling capacitances
  - Similar number of masked channels.
  - Similar S/N
- Next TB in March 2020
- Lots of inputs for the next generation:
  - Adding space for decoupling capacitances in the PCB
  - Adapting the board to the automatic gluing robot.

ECAL events reconstruction

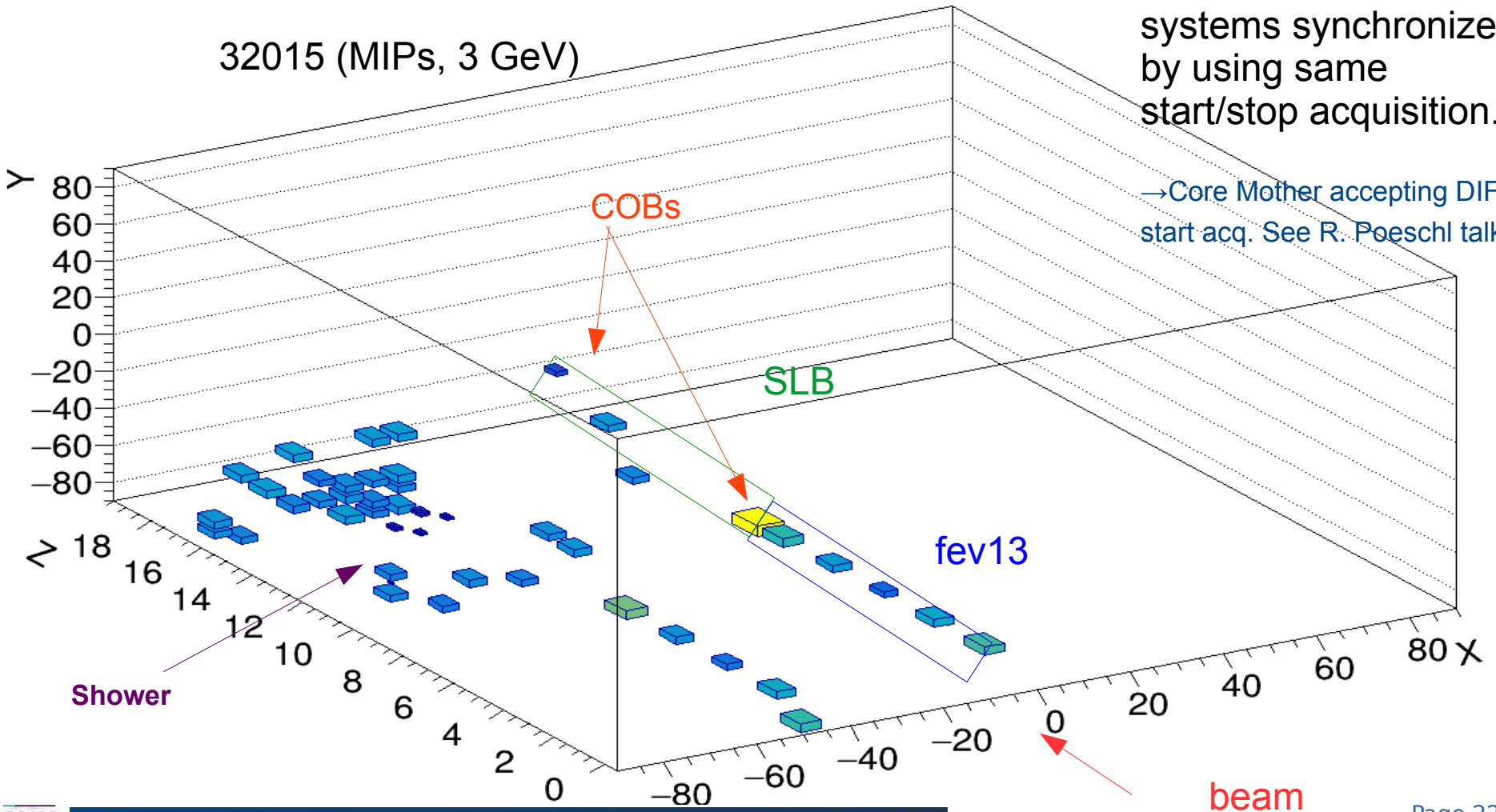
Some built events (preliminary)

32014 (MIPs, 3 GeV, only SLB in the reconstruction)





Some built events (preliminary)



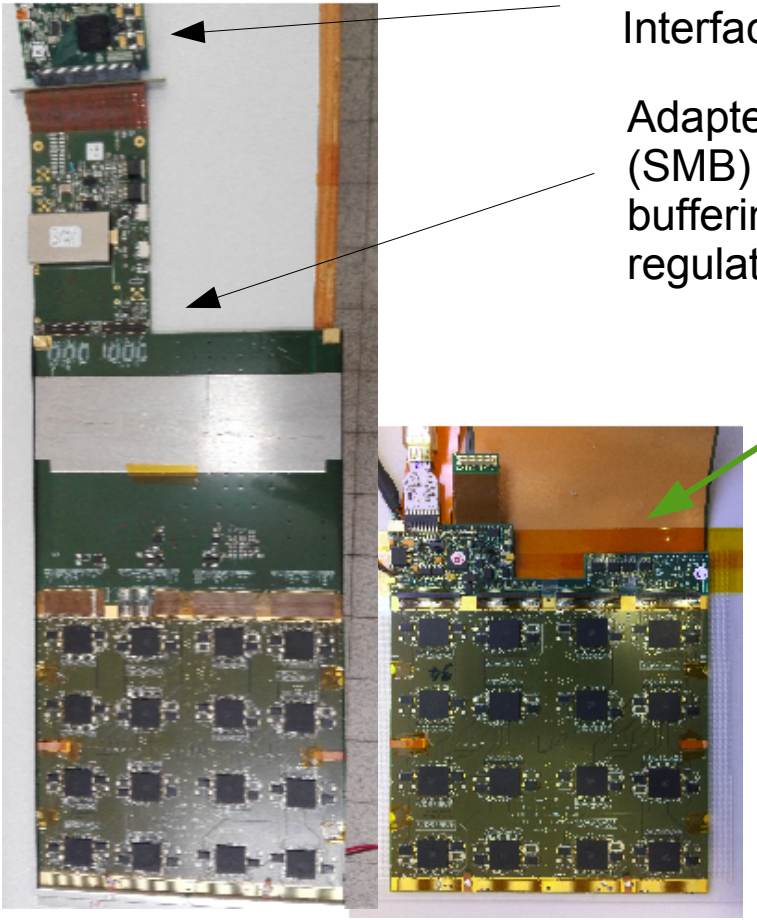
DIF + SL-Board systems synchronized by using same start/stop acquisition.

→Core Mother accepting DIF start acq. See R. Poeschl talk.

Outlook:
TB March 2020

Reminder: BGA based PCB

- 4 versions currently being operated: FEV10, 11, 12, 13.
- 7(+2) FEV10-11 used in 2017-2018 beam test campaign.
  - Using the previous front-end generation (SMB+DIF).
  - Being exported to the new ultra compact front-end electronics SL-Board (see R. Poeschl's talk)
- 2 FEV12 (minor changes w.r.t. FEV11) used in TB2019 with the new SL-Board system.



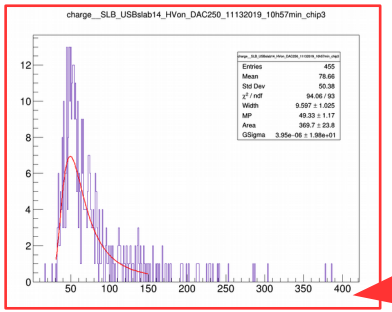
Detector Interface (DIF)

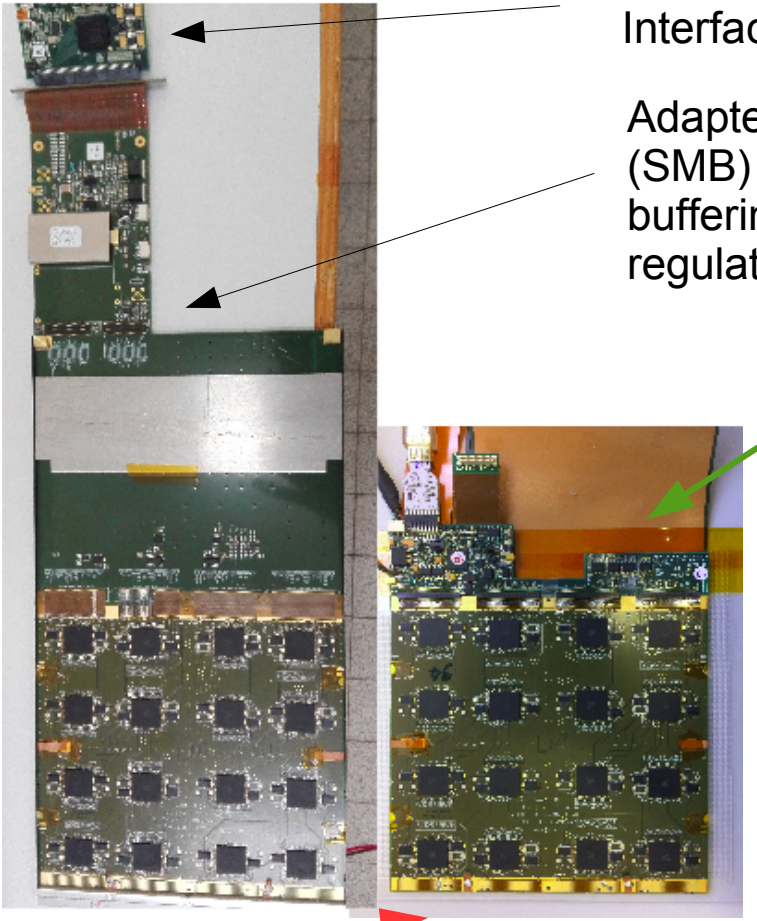
Adapter card (SMB) for signal buffering + power regulation.

DIF and SL-Board concepts are completely compatible.

Reminder: BGA based PCB

- 4 versions currently being operated: FEV10, 11, 12, 13.
- 7(+2) FEV10-11 used in 2017-2018 beam test campaign.
  - Using the previous front-end generation (SMB+DIF).
  - Being exported to the new ultra compact front-end electronics SL-Board (see R. Poeschl's talk)
- 2 FEV12 (minor changes w.r.t. FEV11) used in TB2019 with the new SL-Board system.





Detector Interface (DIF)

Adapter card (SMB) for signal buffering + power regulation.

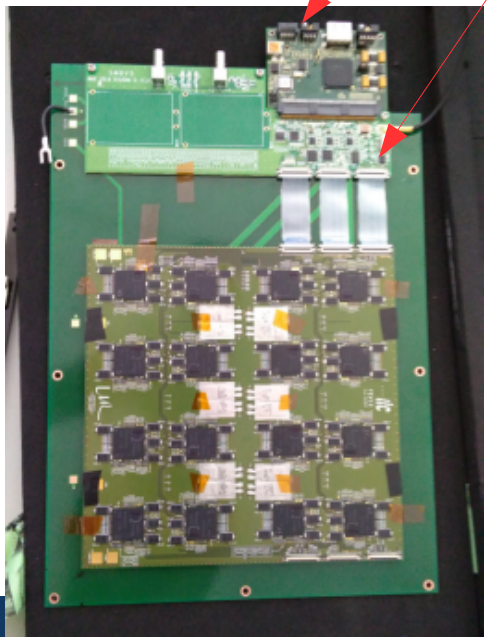
DIF and SL-Board concepts are completely compatible.

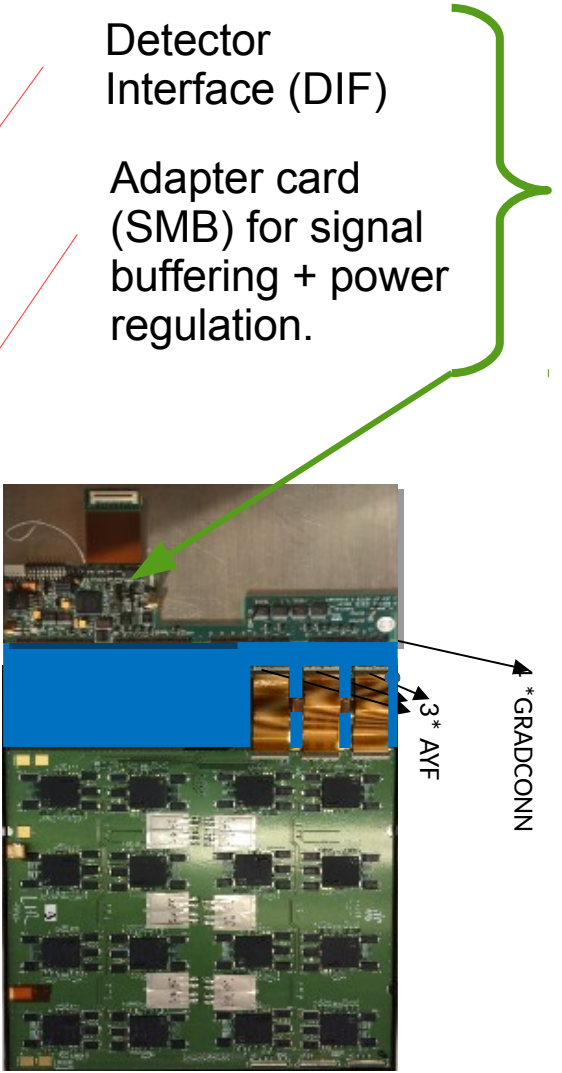
Reminder: BGA based PCB

- 4 versions currently being operated: FEV10, 11, 12, 13.
- Up to 5 FEV13 tested during 2019-2019.
  - Integrated with the old front end but using a new SMB (different connectivity)
  - Separation of analogue and digital PS layers.
  - Not directly compatible with new system…

Interfacing with SL-Board it is an ongoing activity: goal TB March 2020

- Needs some rewriting of FW.
- See R. Poeschl's talk





Plans for the TB March 2020

- **Flexible box** was able to handle up to **9 slabs** (with tungsten) readout by the two generation of front ends:
  - Being modified to host up to **15 slabs + tungsten readout** with the SL-Board.
  - **Front panel design reoptimized** to facilitate cabling.
  - Air ventilation added.
- March 2020 TB: preparing new sets of modules using the new SL-Board.
  - 2 FEV12 already interfaced with SL-Board (+ 2 more?)
  - 2 COB already interfaced with SL-Board (+ 2 more?)
  - Up to 9 FEV11 that are (8 of them) currently interfaced to the “old” front end.
  - Up to 5 FEV13.
  - **Between 15000 – 20000 calorimetric cells !**
- Upgraded SL-Board.

Excellent COB performance: competitive with the BGA boards but with minimal extra components !!

- Great step forward in the COB R&D with lots of inputs for the next COB generation design.

Very successful test of the new ultra compact DAQ based on the **SL-Board.**

Stay tuned for more developments & results soon.

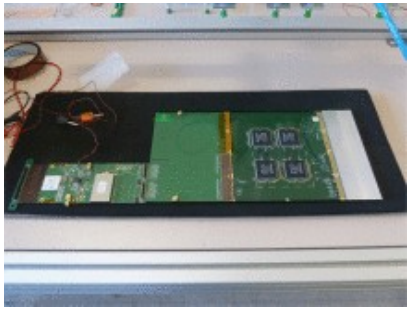
Summary

Back-up slides

Technological prototype

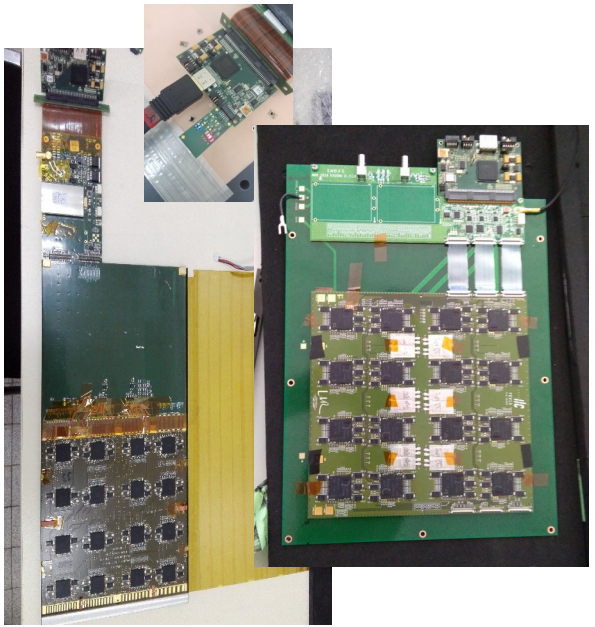
- Front end and VFE compactification with self-trigger ASIC (SKIROC2/2a) operated in power pulsing, higher granularity (5x5mm), compact modules

2010-2015



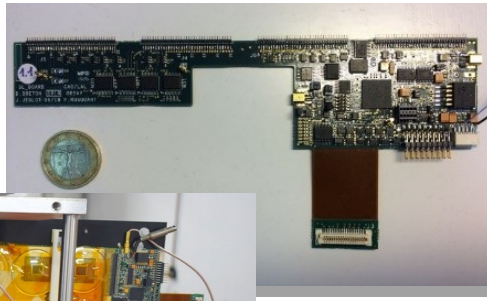
- Version 0 of techn. Prototype
- 256 channels
- 1st power pulsing tests

2015-2018

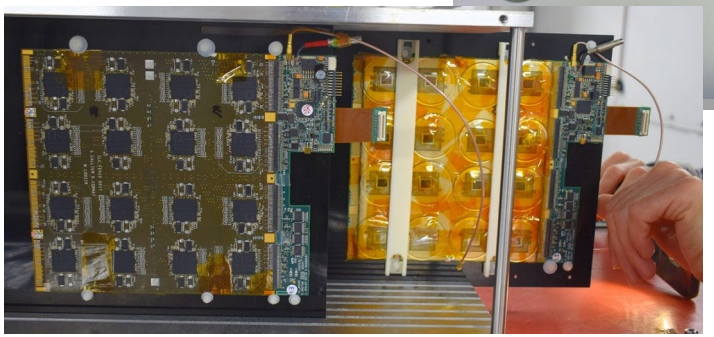


2015-2019

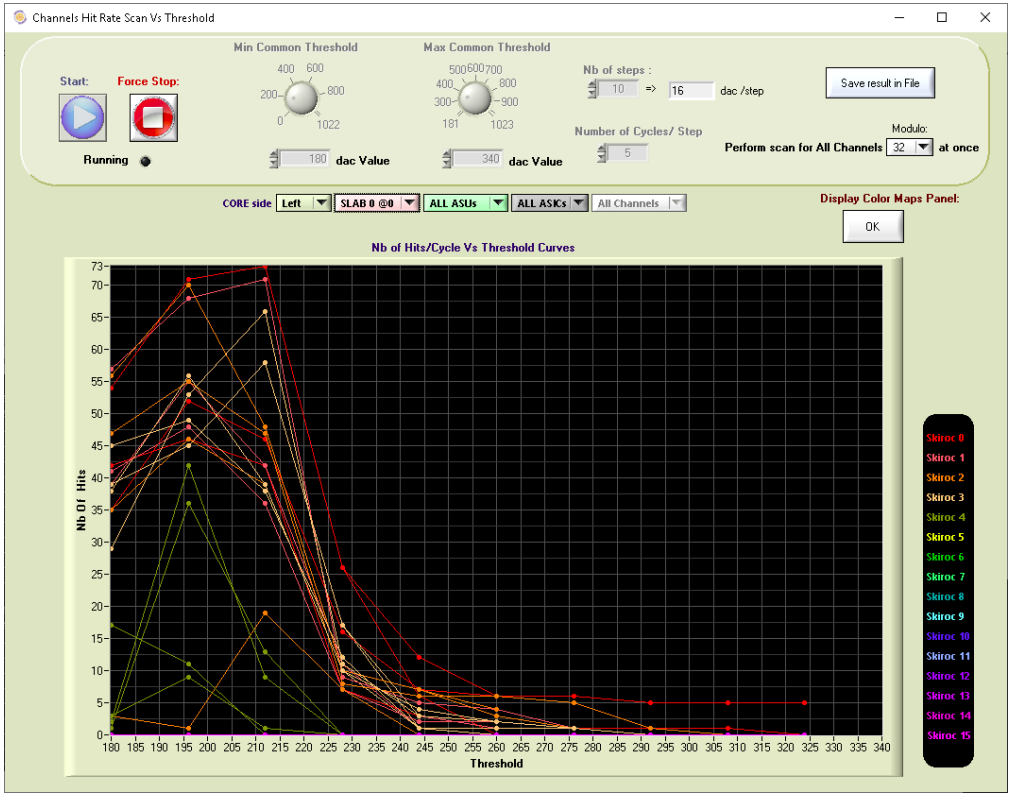
- Ultra thin PCB (COB) with wirebonded ASICs

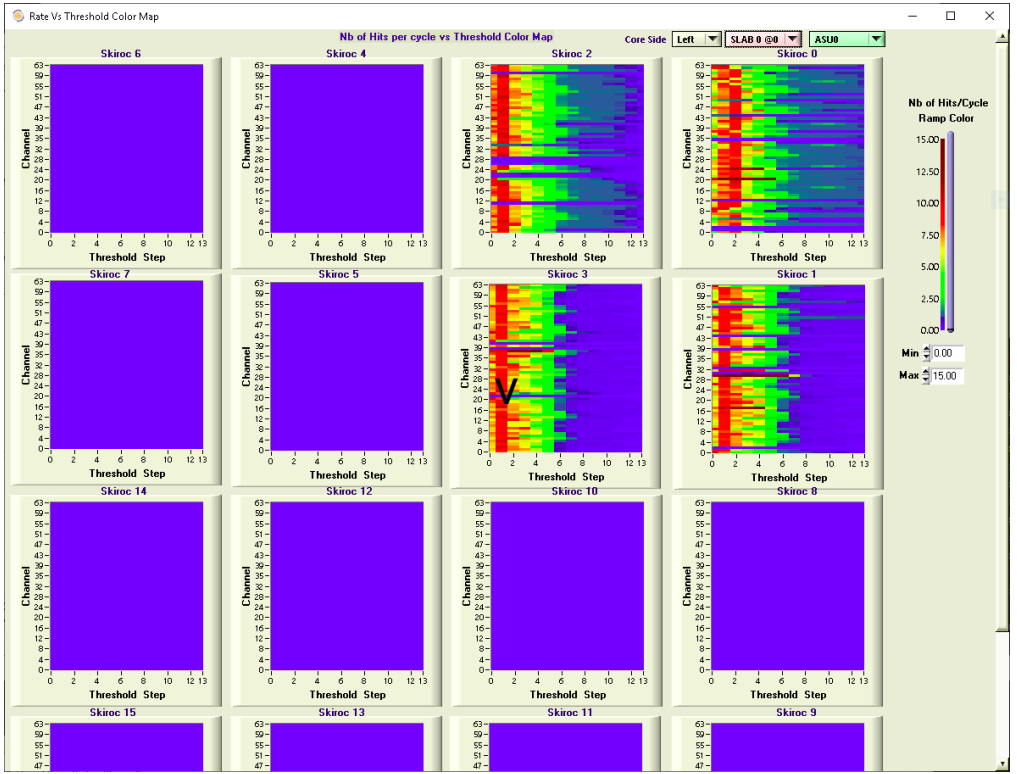


2018-2019



- **1024 chns per module in a 18x18xm surface**
- **Ultra compact DAQ and PCBs**


Channels Hit Rate Scan Vs Threshold
Min Common Threshold
Max Common Threshold
Start:
Force Stop:
Running
180 dac Value
340 dac Value
Nb of steps :
10 => 16 dac /step
Save result in File
Number of Cycles/ Step
5
Modulo:
Perform scan for All Channels 32 at once
CORE side Left SLAB 0 @0 ALL ASUs ALL ASICs All Channels
Display Color Maps Panel:
OK
Nb of Hits/Cycle Vs Threshold Curves
Nb Of Hits
Threshold
Skiroc 0
Skiroc 1
Skiroc 2
Skiroc 3
Skiroc 4
Skiroc 5
Skiroc 6
Skiroc 7
Skiroc 8
Skiroc 9
Skiroc 10
Skiroc 11
Skiroc 12
Skiroc 13
Skiroc 14
Skiroc 15


Rate Vs Threshold Color Map
Nb of Hits per cycle vs Threshold Color Map
Core Side Left SLAB 0 @0 ASU0
Skiroc 6
Skiroc 4
Skiroc 2
Skiroc 0
Skiroc 7
Skiroc 5
Skiroc 3
Skiroc 1
Skiroc 14
Skiroc 12
Skiroc 10
Skiroc 8
Skiroc 15
Skiroc 13
Skiroc 11
Skiroc 9
Channel
Threshold Step
Nb of Hits/Cycle Ramp Color
Min 0.00
Max 15.00

ID	Date	Author
2162	Sat Jul 6 14:55:53 2019	Taikan, Yu, Ludovic, Vincent, Adrian

End of the beam test, at 14.30. Start dismounting.

Run numbering:

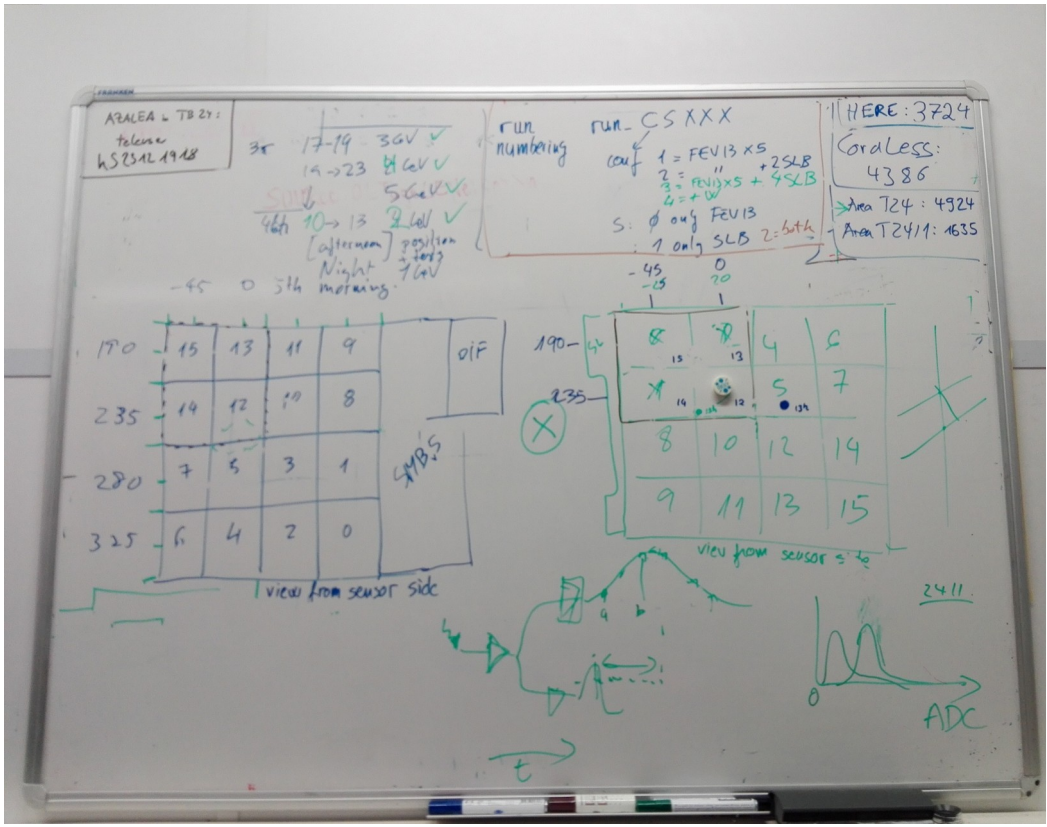
run_CSXXX

- C= configuration
  - 1: only 5 FEV13 in the box
  - 2: 5 FEV13 + 2 SLB (0 and 3) in the box
  - 3: 5 FEV13 + 4 SLB in the box
  - 4: 5 FEV13 + 4 SLB in the box + tungsten plates
- S= system in the DAQ
  - 0= only FEV13
  - 1= only SLBs
  - 2= all

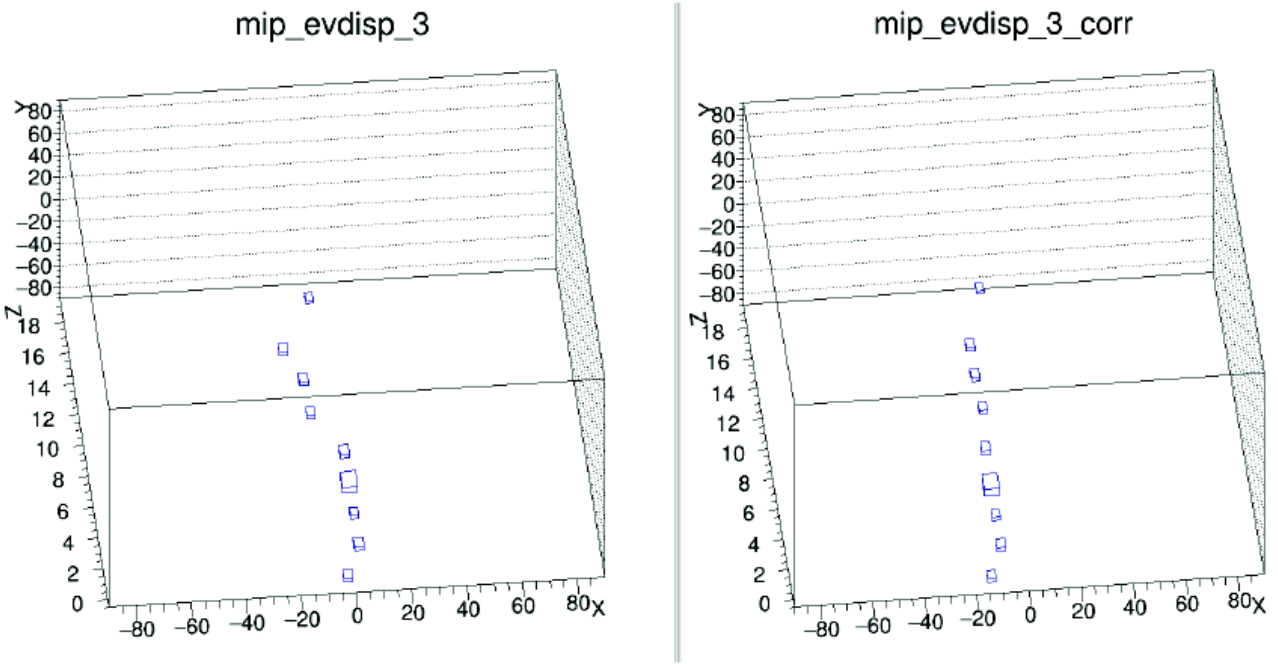
Data location. In the EOS (CERN)

/eos/project/s/siw-ecal/TB2019-06/

Root files with built events for the common runs are to be prepared.



Some results: using tracks to align the modules



- Julien Marchioro (Work in progress)