Development of the ATLAS Liquid Argon (LAr) Calorimeter Readout Electronics for the HL-LHC

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Why new readout for HL-LHC?

- **Main reason:**
  - Incompatibility with the HL-LHC ATLAS Trigger/DAQ scheme (L1 @ 100kHz max => L0 @ 1-4 MHz)
  - Aging: current electronics would be >30 years old by end of the HL-LHC
  - Radiation tolerance: most of current front-end electronics rated up to 1000 fb^{-1}, would like electronics qualified for 4000 fb^{-1}

- **Other reasons:**
  - Improve readout performance: implement two gain system to avoid gain switching at energies relevant for $H \to \gamma\gamma$ photon calibration

- **Requirement:** Free running at 40 MHz, 2 gains, all data sent off detector
  - Wide dynamic range: 16 bits over 2 gains
  - Electronic noise lower than MIP signal (~50 MeV in middle layer)
  - Linearity better than per-mil level in precision measurement region
  - Data transmission: ~300Tbps (200Gbps x 1500 boards)
LAr electronics in HL-LHC

Phase I upgrade:
in progress now,
10x fewer
Boards & easier
analog
requirements
LAr Front-End Board (FEB2)

- Purpose: Provide input line termination, amplification, shaping, digitization and data transmission to the off-detector electronics
- Radiation-tolerant to 180 kRad
- Inspired by current FEB design
- 1524 FEB2 boards, 128 channels each
- Key ASICs:
  - PreAmplifier/shaper (PA/S)
  - ADC
  - Serializer
Key functionality/specifications include:

- Handle 4 calorimeter channels per PA/S ASIC
- Provide two linear overlapping gain scales (HG/LG = 22±5), with CR-(RC)^2 shaping
- Dynamic range: Up to 16-bit, with I(max) up to 10 mA
- Tunable Z\textsubscript{in} = 25, 50 Ω
- Analog filtering with configurable shaping time (15±5 ns)
- Provide analog sums for L0 trigger path

Three designs available: LAUROC, ALFE, HPS1

- Getting ready to test 3rd (and final) pre-prototypes for LAUROC and ALFE, implementing different PA designs, 130 nm CMOS from TSMC
- HPS1 Preshaper is for HEC only, first prototype submitted in September
  - For the Hadronic End Cap (HEC), the PA/Shaper ASIC needs to be replaced with a Preshaper as the HEC incorporates GaAs ASICs on detector in cryostats that include inverting amplifiers plus first stage of summing
**FEB2: Analog processing (2)**

- **LAUROC0** test chip used to investigate various PA designs
- **LAUROC1** designed with 4 PA/S channels shows good results
  - Integral non-linearity (INL) < 0.2% for the full range for HG/LG & 25Ω 10mA/ 50Ω 2mA
  - $Z_{in}$ constant within 1Ω up to 10 MHz
  - Equivalent noise current (ENI) ~250nA at 50ns for the 10mA PA (req. is 300nA)
  - Successfully passed total ionizing dose (TID) tests (1-5MRad)
- Next version (submitted in September) includes full functionality, incl. I2C slow control, trigger sum, ...

- **ALFE** aims to achieve lower noise via a fully differential architecture
- **ALFE0** was 2-channel test chip, implementing 25Ω, 10 mA configuration
  - Measured INL < 0.2%
  - ENI ~150 nA
- **ALFE1** includes full density (4 channels) and full functionality, including trigger sum configurable $Z_{in}$, ...
  - Recently submitted for fabrication
FEB2: ADC

Key functionality/specifications include:

- Digitize both gains of 4 calorimeter channels (i.e. 8 ADC/ASIC)
- Digitize each bunch crossing (i.e. 40 MSPS)
- 14-bit dynamic range, with > 11 bit precision
- Provide output digital data streams (plus BCID) at 640 Mbps

Baseline approach is 65 nm CMOS full-custom development (COLUTA)

- currently on 3rd pre-prototype with full density (8 ADC channels) and full functionality (incl. on-chip bandgap and voltage references, clock distribution, ...)
- 4 channels a Dynamic Range Enhancer (DRE) block with internal 1X/4X gain and 4 channels with a more conventional single-stage MDAC
- 12-bit successive approximation register (SAR) and input stage to resolve upper 2 bits
- simulated performance of effective number of bits (ENOB) > 11.3 for DRE and > 12.2 for MDAC

Given challenging specs, have two alternative options, decision in 2020:

- “IP Block” approach, using 12-bit 160 MSPS analog block in 65 nm CMOS developed for CMS, followed by digital processing to aim for 14-bit at 40 MSPS
- Other possibility is to use COTS ADC (much higher cost)
FEB2 board

- First analog testboard: 4 channels, v2 preprototypes of LAUROC PA/S and COLUTA ADC, plus v1 prototype of lpGBT
- Full readout chain working
- Early performance results are encouraging
  - $\sigma_E/E < 0.04\%$ (req. 0.25\%)
  - $\sigma_t \sim 17\text{ps}$
  - Also studied noise, cross-talk, ...
  - Agreement with requirements
Calibration Board

- Precise calibration of new LAr FE electronics with pulse dynamic range extending up to 7.5 V
- Dynamic range: 16 bits
- Integral non-linearity <0.1%
- Uniformity between channels < 0.25%
- Pulse rise time < 1 ns
- Radiation-tolerant to 180 kRad
- 130 boards with 128 channels each
- Key components:
  - High-frequency (HF) switch
  - DAC
Calibration Board: switch

- Test switch chip in HV-CMOS technology (XFAB 180 nm) produced in 2018
  - Linearity: at high current (injected charge) > 1 mA, INL is small and ~0.2%
  - Maximum of the peak is stable with time
  - Gamma irradiation up to 5MRad (25 x what is needed): no visible degradation observed
Calibration Board ASIC (CLAROC)

CLAROC v2: switch + DAC
- Calibration switch 4 channels
- Up to 320 mA per channel on single channel
- 1 DAC for the 4 channels
- DAC provides 40 mA (13 bit)
- 8x gain with current mirror to provide 320 mA (3 bits)
- Chips arrived last week

In progress:
- CLAROC testboard & its infrastructure
- Tests starting this year:
  - Functionality of the ASIC
  - Irradiation
  - ...
LAr Signal Processor (LASP)

Purpose:
- Receives FEB2 data
- Applies digital filtering
- Buffer/transmits data to TDAQ at 40MHz and to DAQ at 0.6-1MHz
- Computes energy and signal time in each detector cell
- Key components:
  - Main Blade
  - Rear transition module (RTM)
  - 190 boards each
LASP (Main blade + RTM)

Implementation Baseline:
- **ATCA Main Blade** with input optical transceivers and 2 Stratix 10 FPGAs
- **RTM** with 1 Controller FPGA (Zynq+) and output optical transceivers
- Schematics completed & routing started
- Close interaction with INTEL to check the Main Blade design

Input links per processing FPGA: 88 @ 10.24 Gbps

Output links:
- FELIX/TDAQ: ≤ 4 @ 10.24 Gbps
- Global Event Processors: ≤ 4 @ 25.65 Gbps
- fFEX: ≤ 19 @ 25.65 Gbps
- legacy FEXes: ≤ 30 @ 10.24 Gbps

**LASP test goals:** evaluate latest FPGA technologies Stratix 10 with System-on-Chip (SX) and large and fast memory (MX)

**Important challenges:** power consumption and cooling

Detailed simulation performed
- power distribution (Sigirity)
- thermal effects on the board (Ansys Icepack)
LASP Firmware

- Phase I experience shows that firmware complexity is often underestimated

- Current status
  - framework set up based on Phase-I with improvements
  - coding guidelines, work flow done
  - continuous integration, automated simulation, unit tests and compilation
  - working on interface definitions between modules, again profiting from Phase-I experience

- Several technical projects started
  - lpGBT protocol and interface
  - 25 Gbps link tests (firefly transceivers)
  - New firmware algorithms for signal processing with improved pileup reduction
LAr Timing System (LATS)

Purpose: clock distribution, control and monitoring of the FEB2 and calibration boards
~20 ATCA blades, each with 16 time+control FPGAs and 1 main FPGA

- low/mid-range FPGA models are being considered (Cyclone 10)


Tests with FPGA development kit (Intel/Altera Cyclone 10) ongoing

- optical link protocol (lpGBT), TTC clock extraction, data synchronization, etc.
Summary

• Readout electronics for ATLAS LAr calorimeter needs to be replaced for HL-LHC
• New readout architecture based on free-running scheme where all data are sent to digital off-detector system
  – TDR published in 2018
• Status and ongoing developments of critical components presented
• The project is progressing well

https://cds.cern.ch/record/2302626
Backups
ATLAS Liquid Argon Calorimeters

- Fine-grained sampling calorimeter
  - EM: LAr-lead
  - HEC: LAr-copper
  - FCal: LAr-copper and LAr-tungsten

- Granularity
  - \( d\eta \times d\Phi = 0.003 \times 0.1 \) in EM first layer
  - \( d\eta \times d\Phi = 0.025 \times 0.025 \) in EM second layer (shower max)

- 182,468 channels

From B. Vachon CHEF2017
FEB2: Optical links

Key functionality/specifications include:

- Links implemented using CERN lpGBT ASICs and VersatileLink+ (VTRx+) components
- 22 up-links per FEB2 at 10.24 Gbps (incl. 8.96 Gbps of user data) used for transmission of calorimeter readout data to LASP
- 2 bi-directional links per FEB2 used for clock and control distribution and monitoring
  - Exploring ideas of how to implement these links to provide redundancy

Built optical link demo system to allow detailed testing and characterization

Optical eye diagram at 10.24 Gbps
FEB2 board

Key functionality/specifications include:

- Integrate several custom components, including PA/S + ADC + Optical links
- Achieve low coherent noise (< 5% of total noise per channel)
- Provide low-jitter clock distribution, and integrate required control, configuration and monitoring functions
- Size and connectors compatible with installation in existing FE crates
- Power budget of 80 – 100 W
- Radiation-tolerant to LAr HL-LHC specifications
### Custom ADC

- Dynamic Range Enhancer followed by 12-bit SAR.
  - DRE block similar to 4x amplifier. It determines most significant two bits of the 14-bit digital code.
  - Two-stage SAR architecture providing 12-bit.

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**Dynamic Range Enhancer (DRE)**

**Pipeline SAR**
FEB2: ADC alternative options

IP Block approach
- Try using 12-bit 160 MSPS analog IP block in 65 nm CMOS developed for CMS, followed by digital processing to aim for 14-bit at 40 MSPS
  - CMS spec is 10.6 ENOB @ 160 MHz
  - Earlier studies with commercial ADC suggest filtering could yield additional ~0.5-1 bit @ 40 MSPS
- First CMS test chip delivered in June, but issue with I2C configuration causing low effective yield
  - CMS tests so far reaching ~10.1 ENOB @ 40 MSPS (for f_IN = 500 kHz)
  - ATLAS tests to start once some chips received

COTS ADC
- Candidate radiation tolerant COTS ADC (TI ADS5294) identified during R&D for Phase-I
  - Survives total dose, but demonstrates SEEs (incl. some that require reset and reconfiguration of ADC chip to recover)
- Complications include much higher CORE cost, requirement of development of digital chip to interface to lpGBT, need for system-level management of SEEs
CLAROC test board configurations

Standard tests using CLAROC DAC

Switch test using external commercial DAC

Irradiation tests

Test IpGBT → Custom SC
LASP: Draft Component placement on PCB
LASP Main Board Temperature studies

- DC/DC - 60°C
  Good temperature for a component without a heat sink

- HotSwap - 50°C
  Increased temperature due to DC/DC but still reasonable

- PCB
  Average temperature PCB = 42°C

Simulation – Temperature Influence on PCB

4 Fan – 25CFM