The Phase-I Trigger Readout Electronics Upgrade of the ATLAS Liquid Argon Calorimeters

CHEF 2019

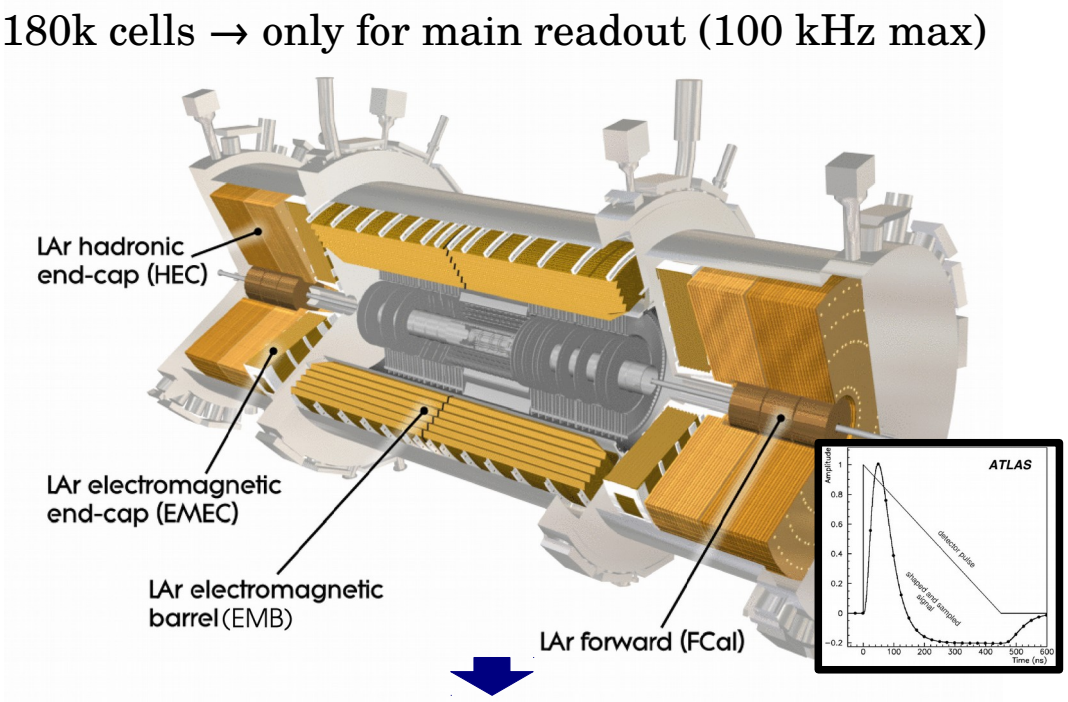
Alexis Vallier (CERN)

On behalf of the ATLAS Liquid Argon calorimeters group

Liquid Argon Calorimeter (LAr)

Pb(Cu,W)/LAr sampling calorimeter

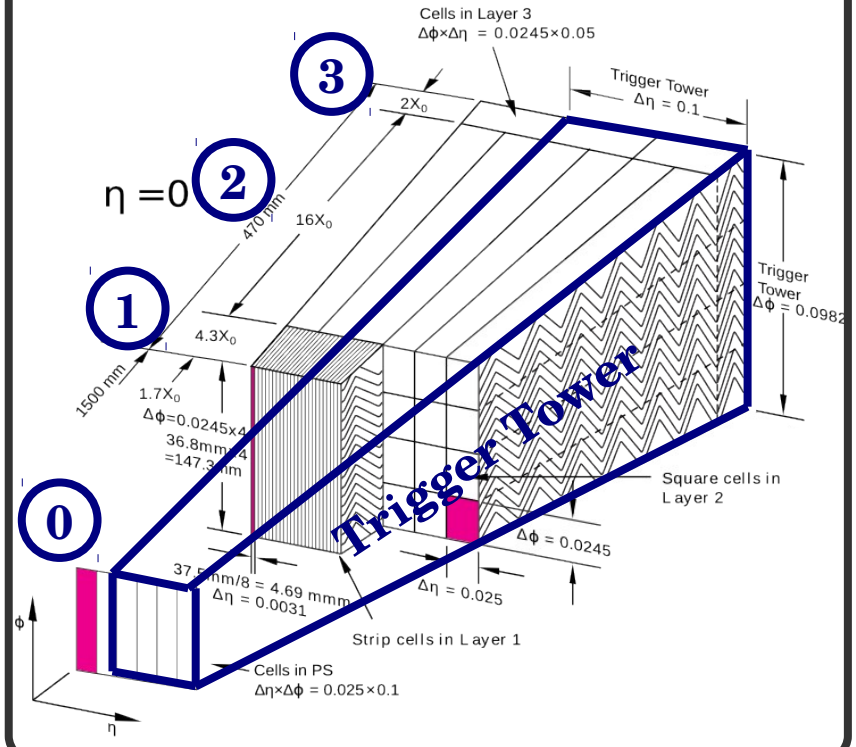
- 180k cells → only for main readout (100 kHz max)



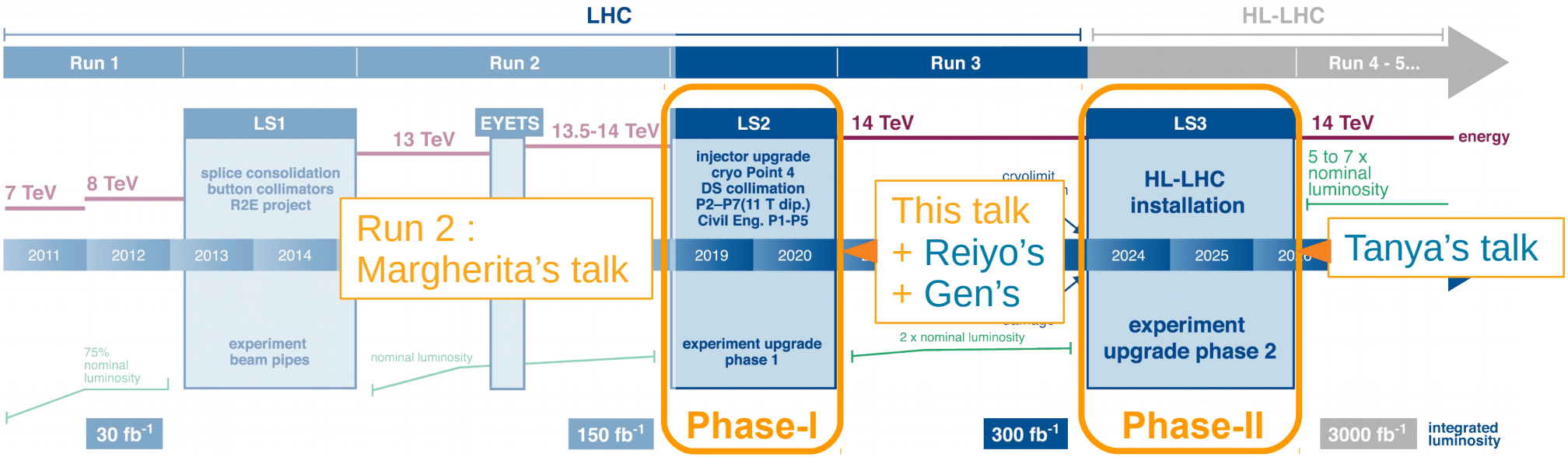
γ, e±, jets, MET from ionisation pulse

Run 1 & 2 : Trigger Tower (TT) (6k)

- Cell clusters in (η,φ) for trigger



LHC / HL-LHC Plan

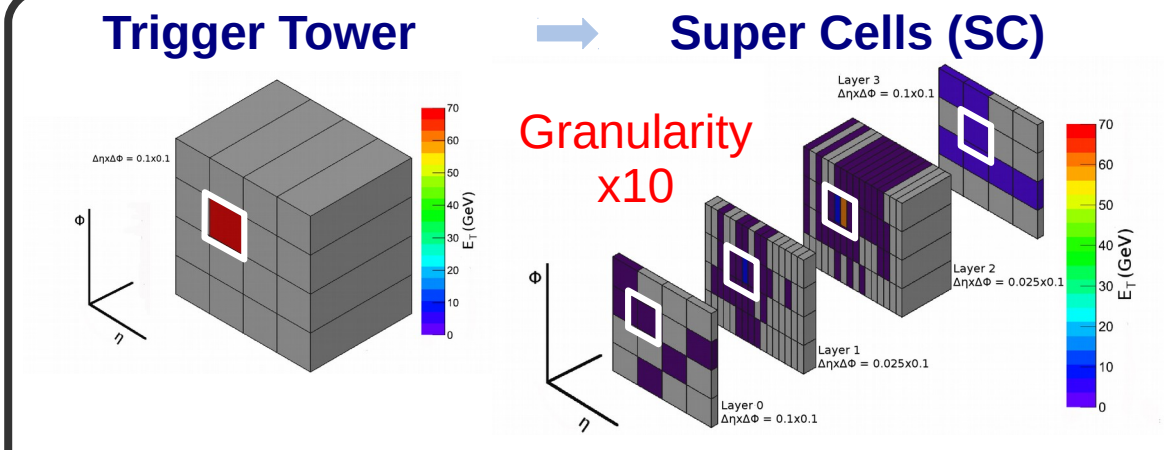


- **In 2018 ATLAS ran with** $\mathcal{L}_{max} = 2.1 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$, $< \mu >= 36.1$ ← Average number of pp collision per bunch crossing
- **LAr Upgrade Phase-I (Now) : trigger readout upgrade** $\mathcal{L} \sim 3 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$, $< \mu > \sim 80$
- **LAr Phase-II (2024-2026) : main readout upgrade** $\mathcal{L} \sim 7 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$, $< \mu > \sim 200$

LAr Phase-1 Upgrade

LHC Run-3 :

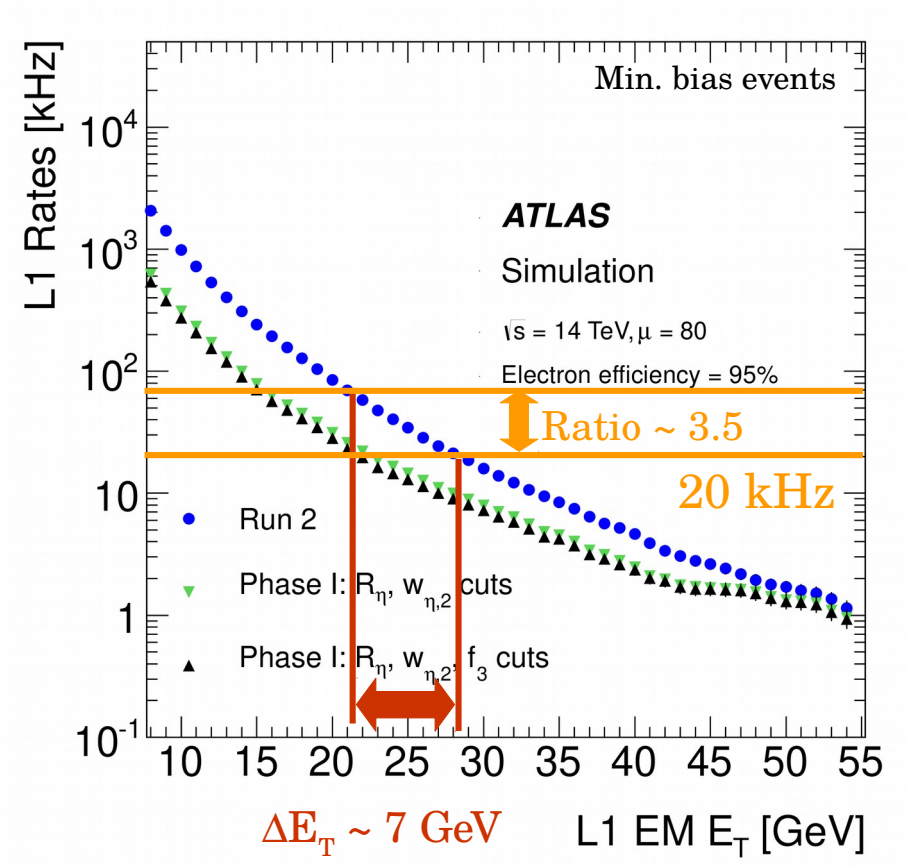
- L1 trigger bandwidth stays at 100 kHz (~20kHz for e±)
- Avoid raise of p_T thresholds → **improve background rejection → Upgrade trigger readout**



70 GeV electron simulation

- **10-fold increase in granularity**
  - longitudinal+lateral segmentation
- **Better digitization precision**
  - 1 GeV → 125 MeV in Layer 2, 32 MeV elsewhere

Trigger Performance Enhancement



- **Shower Shape Discrimination**
  - Better $e^{\pm}$, γ and τ identification @ L1
- **Improved e/γ, jet and missing-E_T efficiency turn-on**
- **Example of performance for electron :**
  - Keeping same bandwitdh (20 kHz), use E_T threshold 7 GeV lower

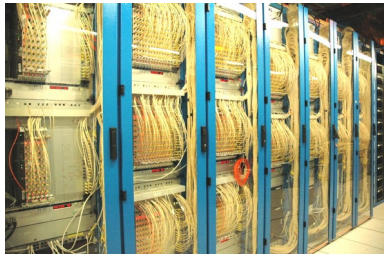
● Run-2 like trigger

▲▼ + Shower Topolog. Cuts

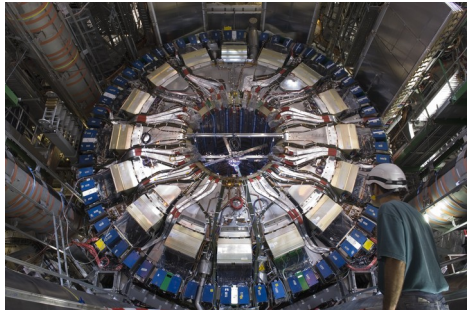
LAr Readout Electronics

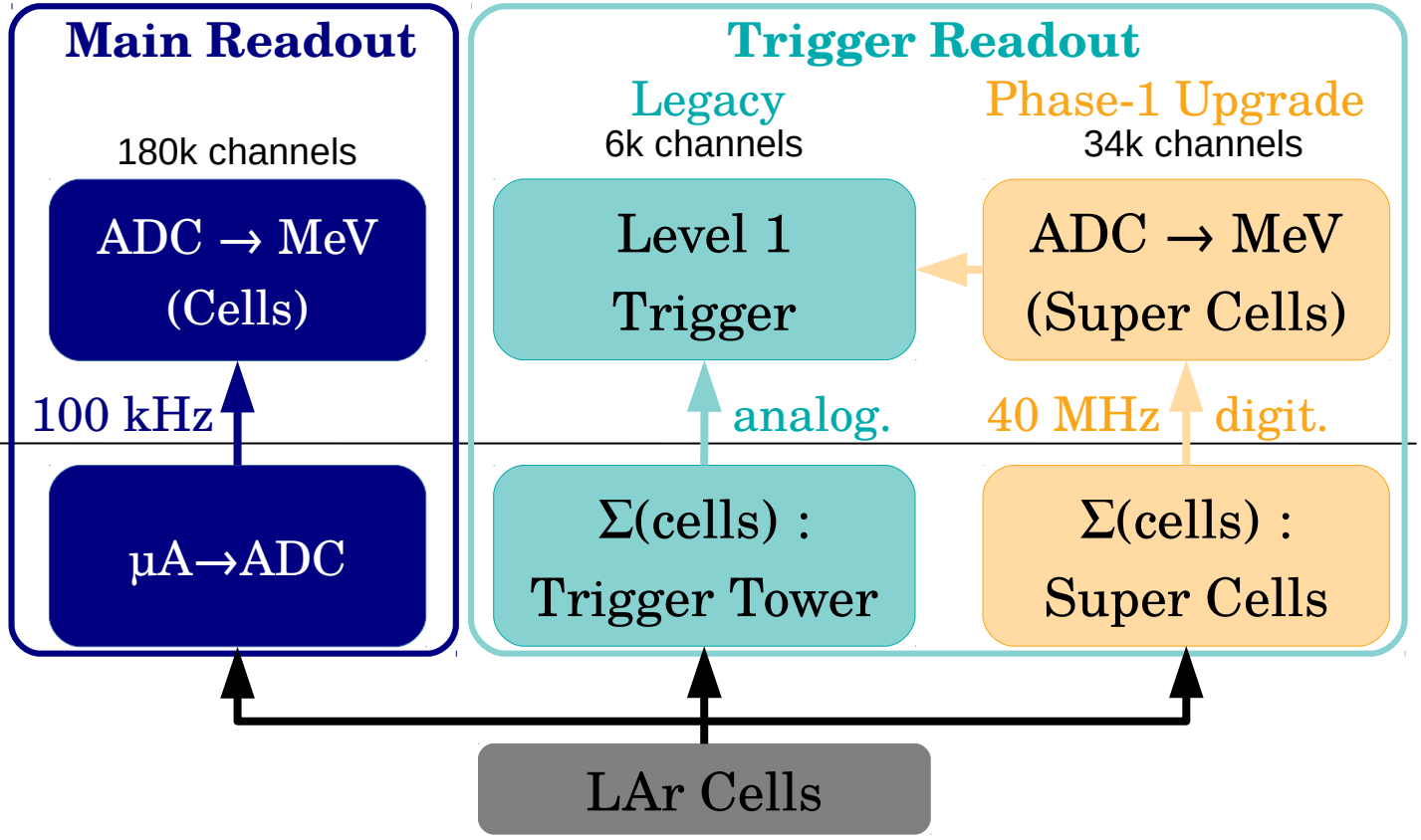
Back-End

(Counting room)



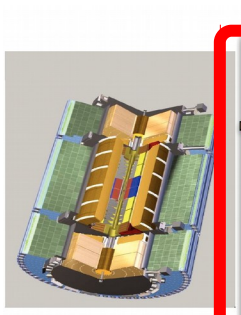
Front-End (On detector)



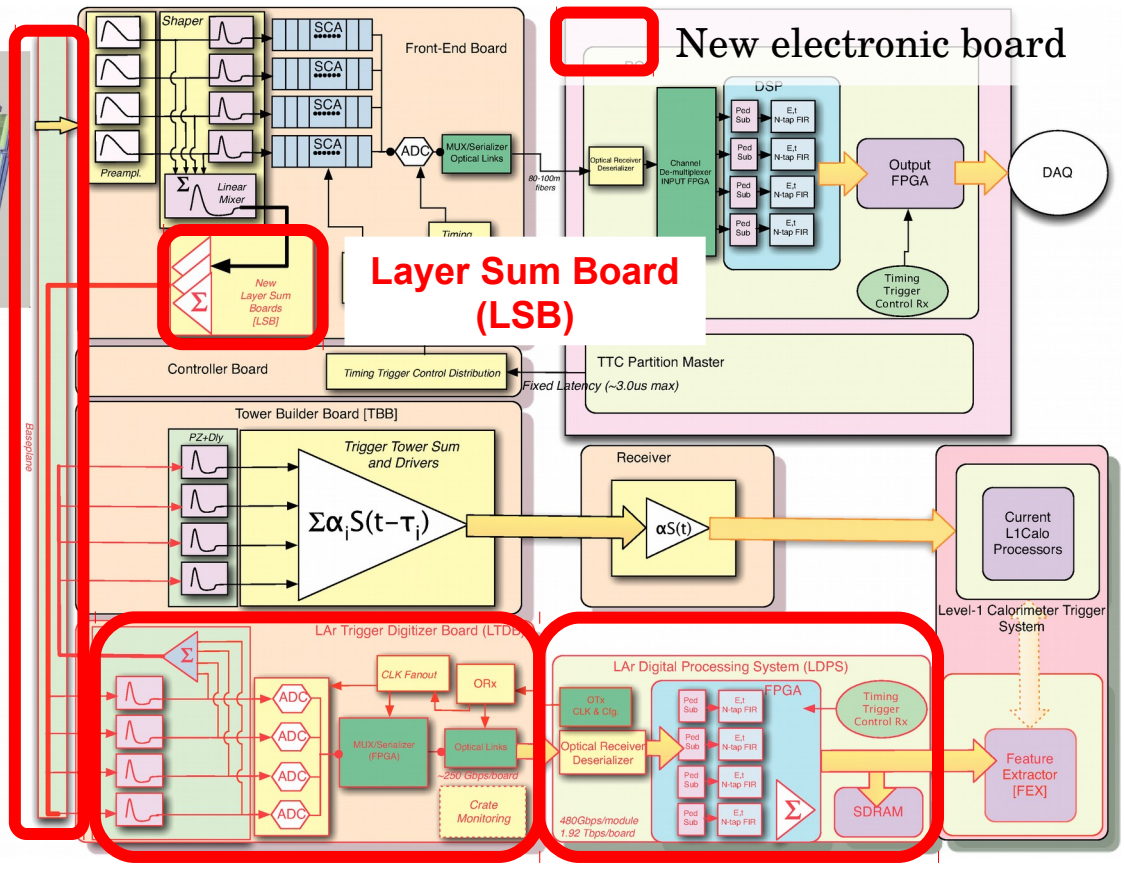


New Electronics : Front End

- **Layer Sum Board**
  - Higher granularity
- **Baseplane**
  - #channels x 10
- **LTDB**
  - Digitizes Super Cell Signals @ 40 MHz, 12b precision
  - Send ADC to Back End
  - Send old layer sums to legacy trigger system (backup)



Baseplane

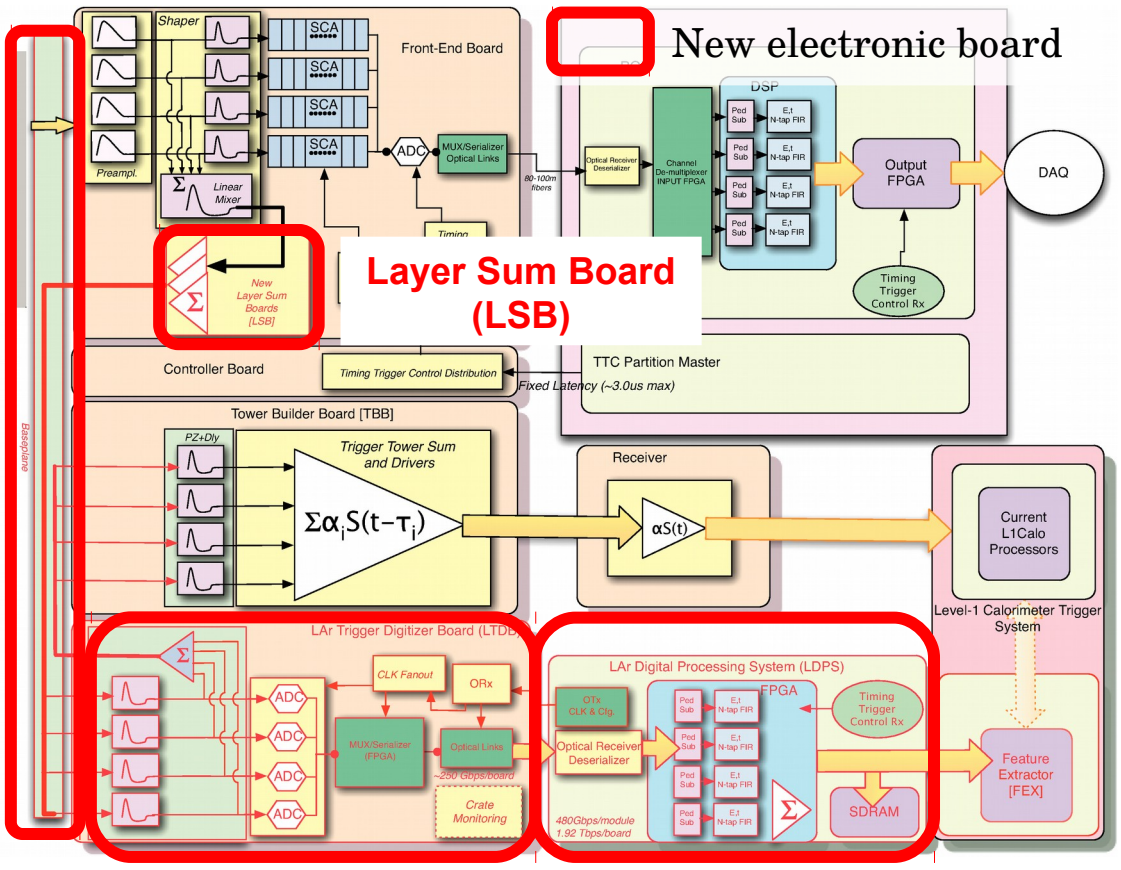


LAr Trigger Digitizer Board (LTDB)

LAr Digital Processing System (LDPS)

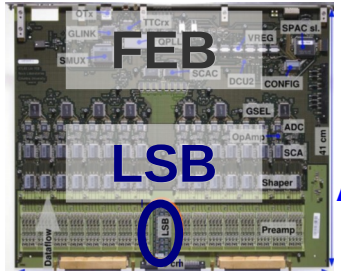
New Electronics : Back End

- **LDPS**
  - Read Super Cell ADC @ 40 MHz
  - Compute Super Cell E_T
  - Identify Bunch Crossing ID of the Super Cell signal
  - Send data to L1 Trigger (41 Tbps) + Monitoring
  - Main board : Lar Digital Processing Blade (LDPB=LArC+LATOME)
- **System with fixed latency**
  - Smaller than 1.625 µs

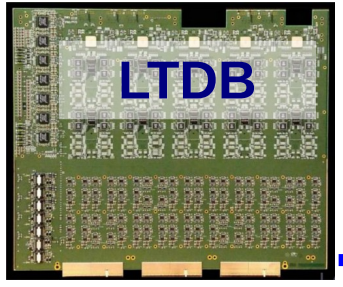


New LAr Electronics

- **LTDB : 124 boards**
  - Custom ASICs : radiation-hard
- **LArC : 30 boards**
  - ATCA carrier
- **LATOME : 116 boards**
  - ATCA advanced mezzanine

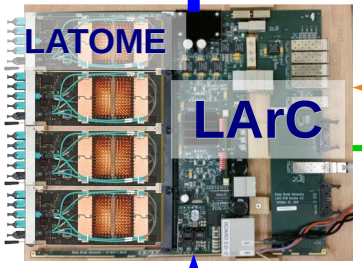


New Analog Σ (SC)



Legacy Analog Σ (TT)

ADC @ 40MHz



ATLAS DAQ

Local DAQ

E_T @ 40 MHz

L1 Trigger

Σ(cells) : Super Cells

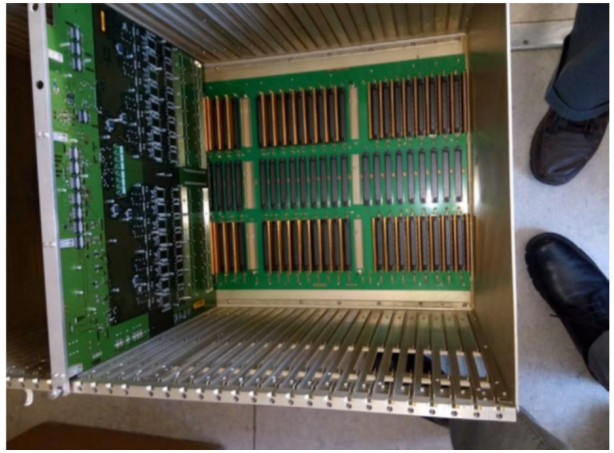
ADC → MeV (Super Cells)

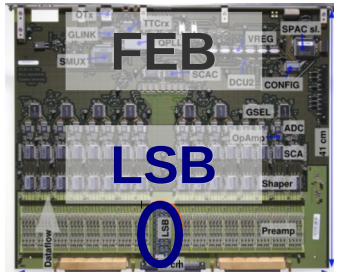
Level 1 Trigger

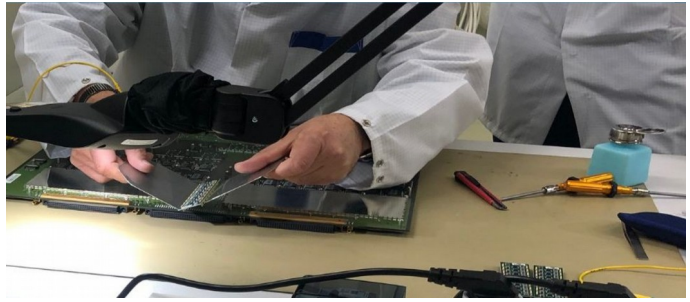
Upgrade Phase-1

Baseplanes & Layer Sum Boards

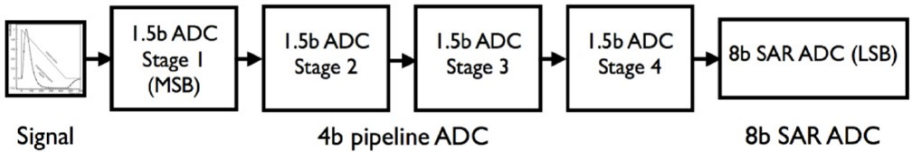
- **Baseplanes : 6 different topologies (Barrel, End-Cap …)**
  - Nominal production done (spares production ongoing)
  - 75 out of 114 installed (~70%)
- **Layer Sum boards (LSB)**
  - Production completed (2456), delivered to CERN
  - 868 FrontEnd Boards re-installed out of 1524 (~60%)

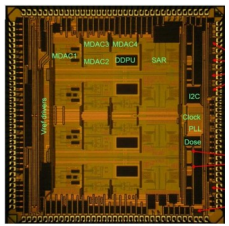


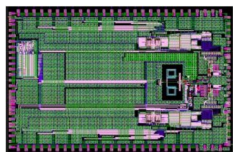


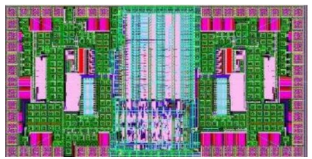


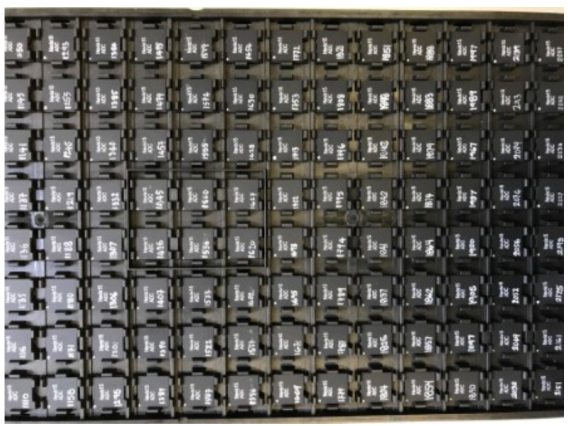
Custom ASICs





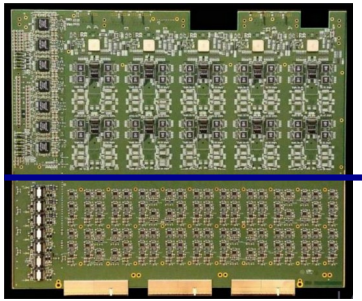






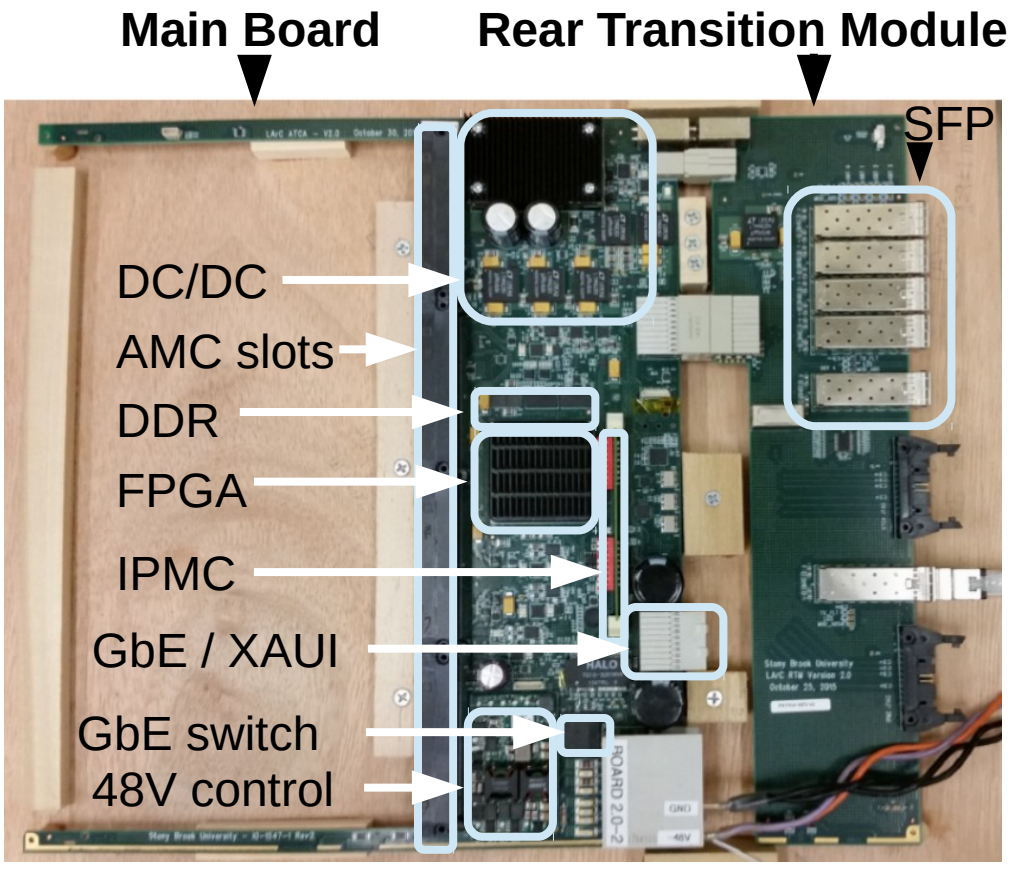
- **ADC: 12b, 4 channels (80 / LTDB)**
  - Tolerance established up to 10 MRad
  - 12.8k chips qualified for LTDB production
  - Tests continue to cover shelf spares
- **Serializer : LOCx2 (20 / LTDB)**
  - 3.2k chips qualified for LTDB production
- **Optical modules: MTx/MTRx (40 / LTDB)**
  - 3.2k Mtx qualified for LTDB production
  - 800 MTRx qualified for LTDB production
  - Few spares production ongoing

Front End – Lar Trigger Digitizer Board



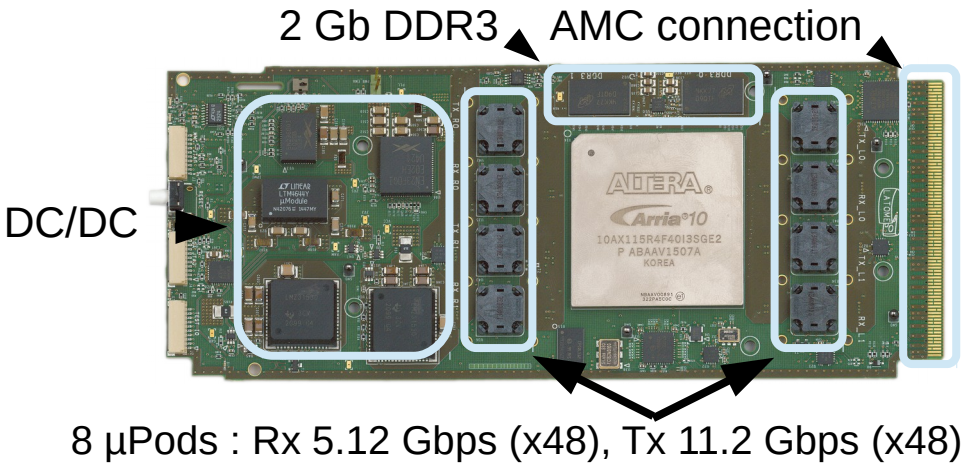
- **A total of 124 LTDB to be installed**
  - 150 PCB produced
  - 70 Barrel LTDB produced and tested
  - 2 End Cap LTDB produced and tested
  - Production & Test of remaining LTDB ongoing
  - **11 LTDB already installed, commissioning ongoing**
  - Totality expected at CERN in Spring 2020

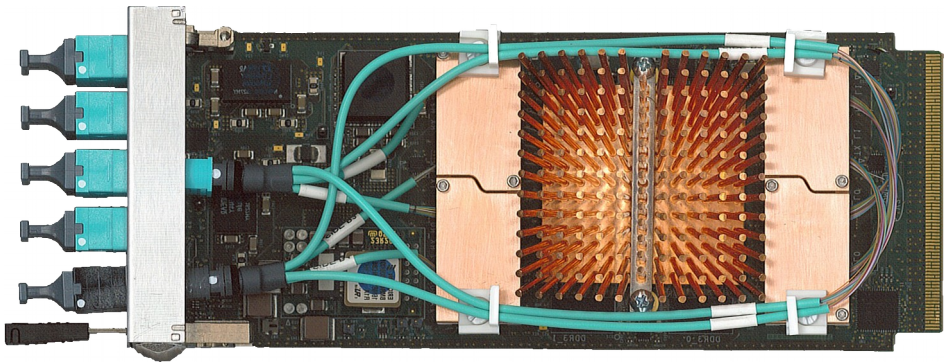
Back End – LAr Carrier



- **Carrier : ATCA back end motherboard**
  - Hosts 4 Advanced Mezzanine Card (AMC) : LATOME
  - Drives Control and Monitoring Data communications
- **34 boards produced and tested (4 spares)**
- **Power management with dedicated card & firmware: IPMC**

Back End – LATOME

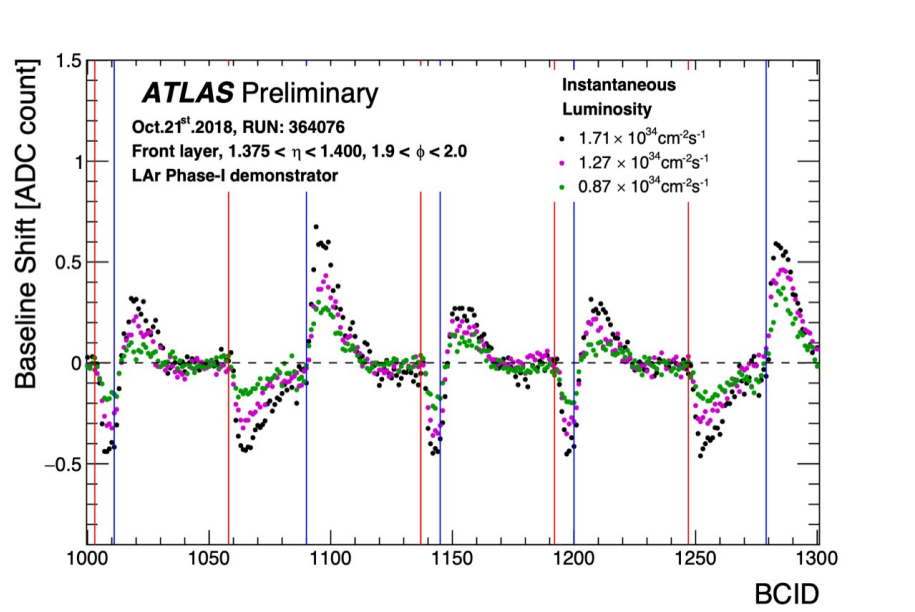




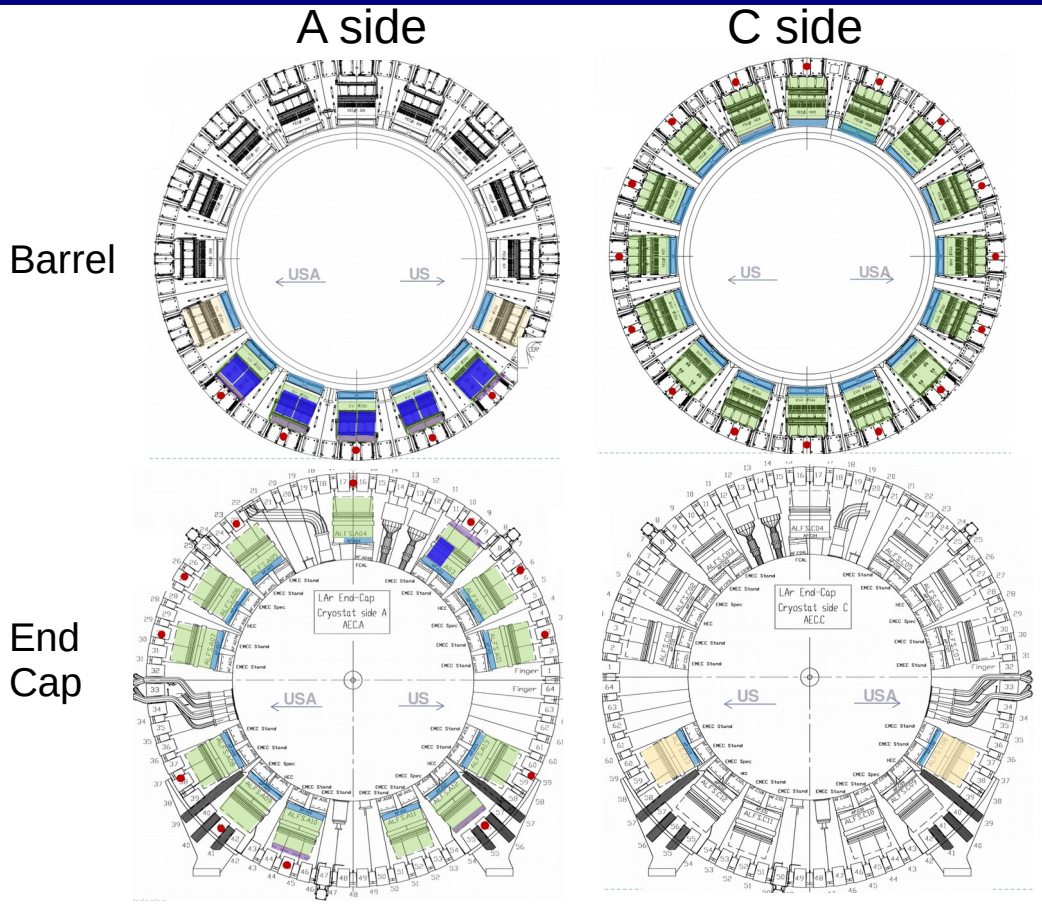
- **LATOME : computes Super Cells E_T and Bunch Crossing ID from ADC, corrects baseline**
  - All 150 boards produced (34 spares), 143 already qualified
  - Blades validation tests LArC+LATOME ongoing
  - Firmware under validation (see Reiyo's talk)
  - Integration tests and commissioning on the real system has started (see Gen' s talk)

Demonstrator

- **Demonstrator installed in 2014 on 1/32 of Barrel**
  - Prototype boards up to spring 2018
  - Pre-production boards aftwerwards
- **Took collisions data parasitically during LHC runs**
- **Valuable inputs for full Phase-I system**
  - Check expected performances
  - Real data → improve simulation
  - Identified bugs in firmware



Installation Status



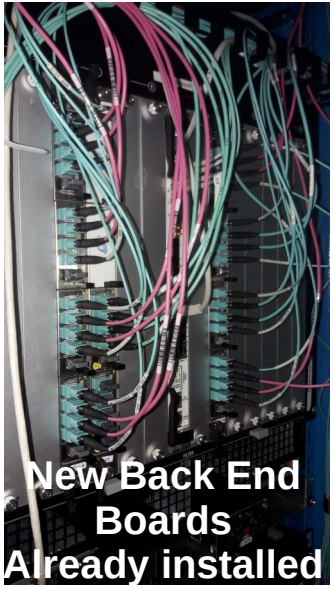
- Baseplane exchanged
- Re-cabled for commissioning
- FEB Boards reinserted
- LTDB installed, in commissioning
- cooling refurbished

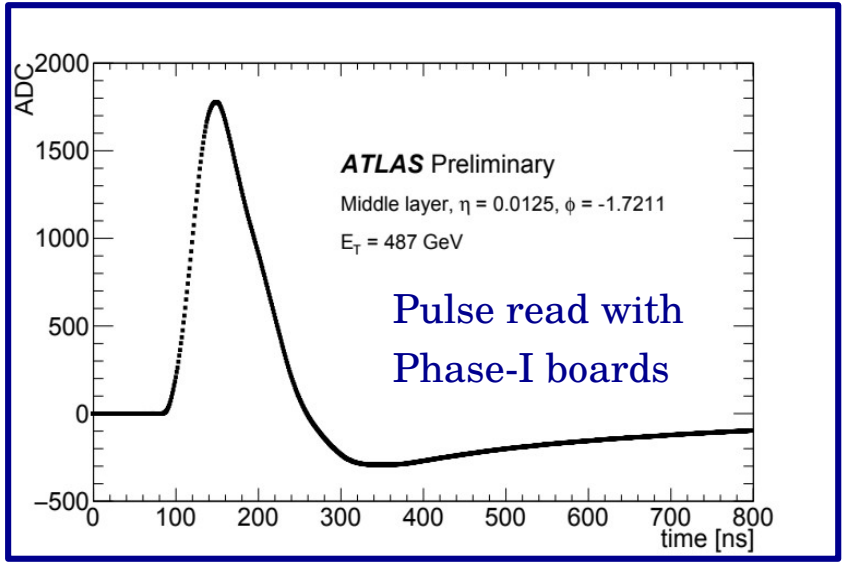
- **Installation started in winter 2019**
- **End : 2nd half of 2020**
- **Access depending on the detector opening**

- **70 % of Baseplanes installed**
- **60 % of FEB reinserted with new LSB**
- **11 LTDB installed**
- **Also refurbish cooling system**

Commissioning

- **Commissioning has started, seperated in 3 steps :**
  - **Main readout :** check refurbished FEB with new LSB are OK
  - **Legacy Trigger readout :** check LTDB provide correct analog sums to legacy system
  - **New Trigger readout :** check new digital sums ⇒ tools to automatised procedures





- **Up to now no issues found on main & legacy trigger readouts !**
- **Currently finalizing tools to check new trigger readout**

Conclusion

- **In 2021, the Run-3 of LHC will start with an increase instantaneous luminosity**
- **The calorimeters are not changed, only the electronics**
  - keep providing excellent performances if readout is sufficient
  - True also for the HL-LHC !
- **Phase-I (now) : electronics is upgraded for the trigger readout**
  - Improve background rejection capabilites + Energy resolution at first level of trigger
- **Production of all the boards has started and will complete in Spring 2020**
- **Installation & Commissioning has started → no major issues, we are on track !**