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LHC-ATLAS Phase-1 upgrade: Firmware validation for real time digital processing for new trigger readout system of the Liquid Argon calorimeter.

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LHC ATLAS Run3 experiment will start from 2021 with higher instantaneous luminosity. ATLAS experiment uses two staged trigger system, the first trigger system is based on hardware, and the second is performed with PC farm. With two staged trigger system, trigger rate can be suppressed to 1KHz from bunch crossing rate of 40MHz. In order to improve trigger performance under high luminosity and high energy condition, we will readout 10 times more finely segment, so-called supercell, with new trigger readout system. This new system requires high performance ATCA mezzanine card, so-called LATOME board, with Intel Arria-10 FPGA. LATOME firmware has several blocks. User Code block, one of main block, calculates deposited energy from 40 MHz sampling 12 bits ADC by using DSP blocks which multiply 14 bits coefficients with a latency of 125 ns. User Code has some modules. About half of them connect to IP bus controller, and which can be read out register contents from FPGA directly. Other modules are connected to a monitoring readout path, which can extract data contents in conjunction with trigger signals. User Code firmware has beed constructed and currently it is under detailed validation. Simulation base User Code verification scheme has been built up based on Universal VHDL/Verilog Verification Methodology (UVVM), which can set up an automatic validation procedure. Also, on-board validation scheme is under development with appropriate readout system. In the presentation, we summarize simulation based firmware verification, and result of on-board validation.

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