Analysis of SiW-ECAL technological prototype beam test with electron beam

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Table of Contents

- R&D of SiW-ECAL technological prototype
  - FEV13-Jp Status
- Beam Test 2019
- Procedure for Energy Measurement
- Analysis
  - Slab commissioning
    - Trigger adjustment
    - Masked channels
    - Pedestal uniformity / stability
  - MIP calibration
  - Shower
  - TDC
The International Large Detector (ILD) is a concept for a detector at the International Linear Collider (ILC). In a slightly modified version, it has also been proposed for the CLIC linear collider.

The ILD detector concept has been optimised with a clear view on precision. In recent years the concept of particle flow has been shown to deliver the best possible overall event reconstruction. Particle flow implies that all particles in an event, charged and neutral, are individually reconstructed. This requirement has a large impact on the design of the detector, and has played a central role in the optimisation of the system. Superb tracking capabilities and outstanding detection of secondary vertices are other important aspects. Care has been taken to design a hermetic detector, both in terms of solid-angle coverage, but also in terms of avoiding cracks and non-uniformities in response.

The overall detector system has undergone a vigorous optimisation procedure based on extensive simulation studies both of the performance of the subsystems, and on studies of the physics reach of the detector. Simulations are accompanied by an extensive testing program of components and prototypes in laboratory and test-beam experiments.

Figure III-1.1 View of the ILD detector concept.

The ILD detector concept has been described in a number of documents in the past. Most recently the letter of intent gave a fairly in depth description of the ILD concept. The ILD concept is based on the earlier GLD and LDC detector concepts. Since the publication of the letter of intent, major progress has been made in the maturity of the technologies proposed for ILD, and their integration into a coherent detector concept.
R&D of SiW-ECAL technological prototypes

Major changes in FEV11 → 13 and SMBv4 → v5

- ASIC: SKIROC2 → 2A
  - Individual threshold control
  - Improvements on TDC
- Smaller SMB footprint
- Connection by 0.4mm-pitch flex cables
  - Two candidates, footprint compatible
- Capacitor for Power Pulsing
  - 0.4 mm thickness, 40 mF x 6
Analogue core: SKIROC2A

- Outputs
  - ADC mode: Charge High($\times$10) & Low($\times$1)
  - TDC mode: Timing & Charge (High or Low)

[Diagram of the analogue core with various components and labels]

arXiv:1801.02024
FEV13-Jp Status

**ASIC:** SKIROC2A

*Si thickness:* 320 μm & **650 μm** New!
- 256 ch/sensor × 4 sensor/slab

**FEV-SMB Connection:** Flexible cable or Micro-coaxial cable

**EM shielding:** w/ Carbon frame and cover

**Operation:** Power Pulsing

---

**Total 5 slabs in Kyushu U., Japan**

<table>
<thead>
<tr>
<th>slab ID</th>
<th>P1</th>
<th>P2</th>
<th>P3</th>
<th>K1</th>
<th>K2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si thickness</td>
<td>650 μm</td>
<td>650 μm</td>
<td>320 μm</td>
<td>650 μm</td>
<td>650 μm</td>
</tr>
<tr>
<td>Board production</td>
<td>in Kyushu U.</td>
<td>in Kyushu U.</td>
<td>in Kyushu U.</td>
<td>in LLR</td>
<td>in Kyushu U.</td>
</tr>
</tbody>
</table>

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Beam Test 2019 @ DESY

● Beam time:
  ◦ 24th June - 7th July at DESY test beam facility
  ◦ e⁻ beam: 1 - 5 GeV
● Presence from:

● Support & Hardware from:
Beam Test 2019 @ DESY

- **Beam time:**
  - 24th June - 7th July at DESY test beam facility
  - e⁻ beam: 1 - 5 GeV

- **Objectives:**
  - Comparison of ASU based on BGA and based on Chip-On-Board (COB)
  - Test of new SL-Boards (SLB)
  - **Validation of FEV13-Jp** ← Target of this talk

- **Programs:**
  - **MIP program (w/o Tungsten):**
    - Position scan for MIP calibration
    - TDC test
    - Angled beam: 25 deg.
    - Retriggering / double pedestal
  - **Shower program (w/ Tungsten):**
    - **Energy measurement**
    - Response from large signal
    - TDC / auto gain
    - Edge effect
Setup for Beam Test

- **Devices:** 2 types of readouts
  - DIF based slabs: FEV13-Jp $\times$ 5
  - SLB based slabs:
    - COB $\times$ 2
    - FEV12 $\times$ 2

- **Absorber:** Tungsten
  - $X_0 = 3.5$ mm, $R_M = 9$ mm, $\lambda_0 = 96$ mm

![Diagram of the setup with SLB slabs, DIF slabs, and Tungsten absorber.](image)
Procedure for Energy Measurement

**Single Slab Analysis**
1. Trigger adjustment & Masking of noisy channels
2. Pedestal calibration
   - 16 chips × 64 channels × 15 memories
3. Gain calibration using MIP
   - 16 chips × 64 channels

**Multi Slab Analysis**
1. Timing coincidence
   - using bunch crossing ID (BCID): $\Delta t = 0.2 \, \mu s$
2. Event Building
Trigger Adjustment (@ Kyushu)

- Threshold scan is performed for estimation of $S/N_{\text{Trig}}$ and trigger adjustment. *(previous TB: 11.6)*
  \[
  S/N_{\text{Trig}} \equiv \frac{\mu_{2\text{MIP}} - \mu_{1\text{MIP}}}{\sigma_{1\text{MIP}}}
  \]
- Test pulse of {4.2, 8.4} fC is injected.
  - 4.2 fC: 1 MIP for 320 μm
- S-curve is fitted by Err-function.
  \[
  f(x) = A \times \text{Errfc}\left(\frac{x - \mu}{\sqrt{2}\sigma}\right) + \text{const}.
  \]

<table>
<thead>
<tr>
<th>Injection [fC]</th>
<th>4.2</th>
<th>8.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>mean [DAC]</td>
<td>265.4</td>
<td>340.4</td>
</tr>
<tr>
<td>sigma [DAC]</td>
<td>12.0</td>
<td>12.5</td>
</tr>
<tr>
<td>$S/N_{\text{Trig}}$</td>
<td>6.4 ± 0.8</td>
<td></td>
</tr>
</tbody>
</table>

- Trigger is set as 0.5 MIP of 320 μm slab: ~ 230 DAC.

$S/N_{\text{Trig}}$ is worse because of noisy pedestals at Kyushu.
But it should probably have stabilized in BT.
Pedestal Uniformity: Mean

- Mean of Gaussian by which non-triggered ADC output is fitted.
- Result of only 1st Memory (Memory-cell dependence is referred later.)

Although there are differences between chips, mean of pedestals looks generally uniform within the same chip.
Pedestal Uniformity: Width

- Sigma of Gaussian
- Result of only 1st Memory (Memory-cell dependence is referred later.)

P3-chip0 looks strange. This chip may be broken.

 chipset & Channel ID (front)

- Width of pedestal is almost uniform (3~4) throughout.
Pedestal Stability

- Pedestal stability is confirmed in this beam time.
MIP event

MIP program is performed for mainly energy calibration of all the pixels.
- Hit map: Sum of the triggered events
- Event display: ADC output of single event after event building

Electron energy: 3 GeV
MIP spectrum

- Typical MIP spectrums of each slabs are shown.
- Pedestal is subtracted.
- Fitted by Lan-Gaus function.
  - Convolution of Landau × Gaussian
- MPV: Most Probable Value
- Definition of $S/N_{ADC}$:
  $$S/N_{ADC} \equiv \frac{MPV_{1MIP}}{Width_{pedestal}}$$

<table>
<thead>
<tr>
<th>slab</th>
<th>P1</th>
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<th>P3</th>
<th>K1</th>
<th>K2</th>
</tr>
</thead>
<tbody>
<tr>
<td>thickness</td>
<td>650µm</td>
<td>650µm</td>
<td>320µm</td>
<td>650µm</td>
<td>650µm</td>
</tr>
<tr>
<td>MPV</td>
<td>146.5</td>
<td>144.9</td>
<td>71.3</td>
<td>141.4</td>
<td>146.1</td>
</tr>
<tr>
<td>Ped_width</td>
<td>3.0</td>
<td>3.0</td>
<td>3.3</td>
<td>2.8</td>
<td>3.1</td>
</tr>
<tr>
<td>S/N</td>
<td>49.0</td>
<td>48.9</td>
<td>21.7</td>
<td>50.2</td>
<td>47.5</td>
</tr>
</tbody>
</table>
MIP calibration: MPV maps

Problems

Higher statistics
Shower event

- Event building have been achieved using the preceding results.
  - BCID offsets between SLB-based and DIF-based are corrected.

- A typical event is checked with event display.
  - In this picture, color scale is not converted to energy, still ADC output.

Event display of shower event
Shower Analysis: Hit Energy

- Hit energy after MIP calibration (run_42003)

Single cell hit energy in 3 GeV e⁻ beam

from noise?
Simulation

- We performed detector simulation for this beam test.
- Simulator: DDSim in iLCSoft
- Structure of FEV13-Jp:
  - Carbon: 0.6 mm
  - Electronics(Air)
  - PCB: K1: 1.6 mm, others: 1.8 mm
  - Glue(Air): 0.08 mm
  - Si: 320 / 650 μm
  - Glue(Air): 0.08 mm
  - Cu: 0.06 mm
  - Carbon: 0.6 mm
  - Plastic: 5 mm
- SLB (FEV12 & COB):
  - Electronics(Air)
  - PCB: 1.6 mm
  - Glue(Air): 0.08 mm
  - Si: 500 μm
  - Glue(Air): 0.08 mm
  - Cu: 0.06 mm
  - Plastic: 5 mm
Comparison of Measured and Simulated.

- Simulated results are converted to MIP units and compared to measured ones.
- Work in progress.
TDC Analysis

- TDC mode operation test
- SKIROC2/2A has the ramp wave as one of the internal clocks
  - I measured this ramp waveform for calculating from TDC to real time factor
- The ramp wave can be measured with
  - synchronization of internal and external clock (injection signal)
  - change the phase of injection signal

![Diagram showing internal clock and ramp wave](image)
TDC Calibration

- TDC is calibrated by injection signal synchronized and delayed against ramp wave.
- Problems:
  - saturation
  - phase should be shifted

- TDC to real time calibration factors:
  - 0.127 ns / TDC count (up)
  - 0.066 ns / TDC count (down)
TDC Correlation with MIP

- Correlation of TDC between slab P1 and P2
- Select 1 ch (at the center of the beam), 450 < ADC < 500 (to avoid time-walk)
- ~10 / 1 ns at the normal slope: timing resolution ~ a few ns?
- TDC calibration in progress.
Correction of Time Walk

- Time Walk: TDC dependence on ADC
- TDC-interval vs ADC are fitted by Log function.
- Width of TDC-interval is improved: 117 $\rightarrow$ 52.

Timing resolution: $5.2 \pm 1.6 \text{ ns}$
Summary

- FEV13-Jp: 5 slabs from Kyushu University
- BT 2019 DESY: **All the slabs worked consistently.**
- Pedestal study
  - Uniformity and Stability is verified.
- MIP calibration
  - MIP calibration is almost completed.
  - S/N is obtained for 5 slabs:

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<td><strong>S/N(_{ADC})</strong></td>
<td>49.0</td>
<td>48.9</td>
<td>21.7</td>
<td>50.2</td>
<td>47.5</td>
</tr>
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- Shower analysis
  - Event building has done and shower event is reconstructed in event display.
  - Hit energy distribution looks consistent with simulation result.
  - Work in progress.
- TDC test
  - Time walk is corrected, but very preliminary.
  - Timing resolution is obtained, however we need more detail study using injection.
backup
Simulation Results

- MIP calibration

**Hit Energy conf0_e_3GeV**

- w/o Tungsten

**Hit Energy conf1_e_3GeV**

- w/ Tungsten

Entries: 10663
Mean: 0.2532
Std Dev: 0.1383

Entries: 10087
Mean: 0.2513
Std Dev: 0.1267
Simulation Results

- Very preliminary

Energy deposit on Si in each slab ($E_{\text{slab}}$)

Sampling ratio

$$\frac{E_{\text{slab}}}{(E_{\text{W}}+E_{\text{slab}})}$$

[MIP/MeV]
Remaining Issues
Double pedestal / Retrigger

- run 32015, slab P1

Retrigger event: BCID is consecutive.

Double pedestal by retrigger
Pedestal difference between ADC/TDC mode

- We found the difference of pedestals between ADC/TDC mode.
- Memory-cell dependence is not same.
- In the first memory cell, the difference of typical Ped_mean is ~15.
Pedestal difference between ADC/TDC mode

- We found the difference of pedestals between ADC/TDC mode.
- Memory-cell dependence is not same.
- In TDC mode, SCA~2 is worse.
Pedestal difference between ADC/TDC mode

- We found the difference of pedestals between ADC/TDC mode.
- Memory-cell dependence is not same.
- In TDC mode, SCA~2 is worse.

- There are double pedestal even after bcid selection in TDC mode.
- The criteria for identification of double pedestal is not optimized.

Work in progress.
Hardware update

- Previous problems
  - Carbon frame was not optimized for FEV13.
  - HV connection between SMB and flex was fragile.

- Update: New carbon frame
Hardware update

- Previous problems
  - Carbon frame was not optimized for FEV13.
  - HV connection between SMB and flex was fragile.

- Update: Conductive adhesion
Masking of Noisy channels

- A few channels are noisy after trigger adjustment and masked: 1 - 2 %.
- Individual threshold control was not used because it wasn't ready. → Next TB
Pedestal Analysis

- Non-triggered ADC output (around ~300 [ADC])
- Fitted by Gaussian
MIP calibration

- slab: P1

Chip0 is broken?

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MIP calibration

- slab: P2

**MPV**

**Error of MPV**

**$\chi^2$/ndf**

Low-statistics because DIF was broken in position scan
MIP calibration

- slab: P3

Chip 0 is broken?
MIP calibration

- slab: K1

HV connection is bad?

MPV

Error of MPV

$\chi^2$/ndf

entries

MIP entries dif_1_1_4

MIP mpv dif_1_1_4

MIP empv dif_1_1_4

MIP chi2ndf dif_1_1_4

MPV

Histogram and distribution of MPV:
- Entries: 482
- Mean: 141.4
- Std Dev: 27.79
MIP calibration

- slab: K2

**MPV**

**Error of MPV**

**$\chi^2$/ndf**

**Good!**
R&D of SiW-ECAL technological prototypes

**ASU: 12 years of R&D**

- Most complex element: electro-mechanical integration
  - Distrib / Collect signals from VFE (ASICs), Analog & Digital with dyn. range ≥ 7500
  - Mechanical placer & holder for Wafers → precision
  - Thickness constraints

<table>
<thead>
<tr>
<th>Milestone</th>
<th>Date</th>
<th>Object</th>
<th>Details</th>
<th>REM</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st ASIC proto</td>
<td>2007</td>
<td>SK1 on FEV4</td>
<td>36 ch, 5 SCA proto, lim @ 2000 mips</td>
<td></td>
</tr>
<tr>
<td>1st ASIC</td>
<td>2009</td>
<td>SK2</td>
<td>64ch, 15 SCA</td>
<td>3000 mips</td>
</tr>
<tr>
<td>1st prototype of a PCB</td>
<td>2010</td>
<td>FEV7</td>
<td>8 SK2</td>
<td>COB</td>
</tr>
<tr>
<td>1st working PCB</td>
<td>2011</td>
<td>FEV8</td>
<td>16 SK2 (1024 ch)</td>
<td>CIP (QGFP)</td>
</tr>
<tr>
<td>1st working ASU in BT</td>
<td>2012</td>
<td>FEV8</td>
<td>4 SK2 readout (256ch)</td>
<td>best S/N ~ 14 (HG), no PP retrigger 50–75%</td>
</tr>
<tr>
<td>1st run in PP</td>
<td>2013</td>
<td>FEV8-CIP</td>
<td></td>
<td>BGA, PP</td>
</tr>
<tr>
<td>1st full ASU</td>
<td>2015</td>
<td>FEV10</td>
<td>4 units on test board 1024 channel</td>
<td>S/N ~ 17–18 (High Gain) retrigger ~ 50%</td>
</tr>
<tr>
<td>1st SLABs pre-calo</td>
<td>2016</td>
<td>FEV11</td>
<td>7 units</td>
<td></td>
</tr>
<tr>
<td>1st technological ECAL</td>
<td>2018</td>
<td>SLABvFEV11 &amp; FEV13 SK2a+ Compact stack</td>
<td>SK2 &amp; SK2a (timing)</td>
<td>Improved S/N Timing...</td>
</tr>
</tbody>
</table>

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